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A Novel Circuit for Pulse Code Modulation - to - Digital Pulse Position Modulation Conversion

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Abstract*— Digital pulse position modulation (DPPM) is a good choice for transmission of data over optical fibre links. The data is often found in pulse code modulation (PCM) form and therefore needs to be converted into DPPM. A novel and low-cost circuit for Pulse Code Modulation (PCM) to Digital Pulse Position Modulation (DPPM) conversion is proposed in this paper. A simple circuit for DPPM-to-PCM conversion is also presented. The proposed circuits have been tested in hardware and the experimental results are quite satisfactory. These circuits have been implemented using purely digital logic design and can therefore be found suitable for IC implementation.

***Keywords*— PCM, DPPM, Optical Fiber**

I. INTRODUCTION

An optical fiber is increasingly becoming popular to free space channel, as large number of signals are being transmitted simultaneously through the fiber by using various modulation techniques. Several organizations have installed optical fiber links for various inland and under-sea systems. With advanced single-mode fibers like dispersion shifted and dispersion flattened fibers coming in the market and with the popularity of the optical fiber amplifiers, intensity modulated direct detection (IMDD) systems are becoming quite popular [1]. The best monomode optical fiber links have bandwidths of the magnitude greater than that of the information currently transmitted over them. This excess of bandwidth can be exploited using digital pulse position modulation (DPPM) instead of commonly used PCM. This is because DPPM offers much better performance characteristics and increased receiver sensitivity [2,3,4]. As predicted by Ian et al [3], receiver sensitivity below 100 photons per binary bit has been achieved with direct detection even at high data rates by exploiting the bandwidth offered by monomode fiber near minimum dispersion wavelength. Pulse position modulation and its comparison with other pulse time modulation techniques has been discussed in literature in detail [5,6]. In DPPM, n bits of PCM are coded into a single pulse that occupies one of 2^n time slots. Thus instead of transmitting n bits of data a single pulse is transmitted that carries the same information. At the receiving end, the pulse is decoded into PCM data by using a digital PPM to PCM converter. Circuits, reported in the literature, for the same are complex [3,7]. Since most of the modems for digital communication have been designed for PCM, a PCM-to-DPPM converter is required if DPPM is to be used for data transmission. Similarly, DPPM-to-PCM converter will be needed at the receiver end as most of the destination units operate on PCM data. In light of the above discussion, a novel and simple technique for PCM-to-DPPM conversion is proposed in this paper. A parallel PCM data is directly converted into the corresponding DPPM signal, using the proposed circuit. Receiver circuit for DPPM-to-PCM conversion is also presented.

II. PROPOSED CIRCUIT

The circuit diagram for proposed PCM-to-DPPM converter is shown in Fig. 1. For the simplicity of experimental work the word length of PCM data is taken as three bits only. This 3- bit parallel PCM data, to be converted into digital PPM signal, is generated by a 3-bit word generator.

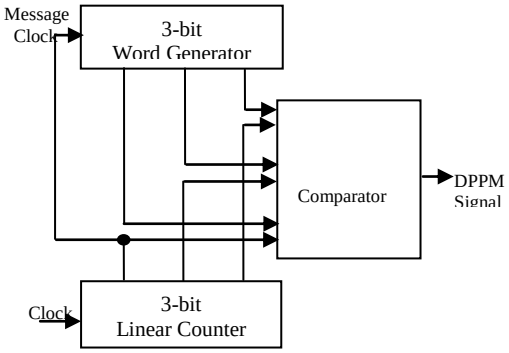

Fig. 1 Proposed PCM-to-DPPM Converter

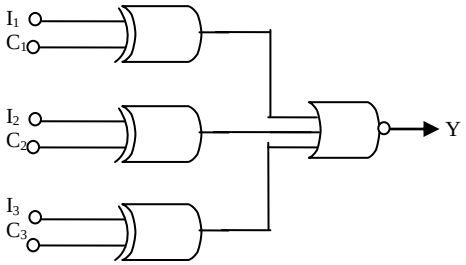

Fig. 2 Circuit diagram of comparator

The PCM data is applied to the comparator circuit as shown in Fig. 1. Each bit of the PCM data is individually compared with a corresponding bit of a 3-bit words generated by a 3- bit linear counter. The comparator circuit is implemented using XOR gates and a NOR gate as shown in Fig. 2, wherein the PCM bits are applied at I_1, I_2 and I_3 and linear counter is connected at C_1, C_2 and C_3. The comparator output is given by

$$Y = \overline{(I_1 \oplus C_1) + (I_2 \oplus C_2) + (I_3 \oplus C_3)} \quad \ldots \quad (1)$$

The clock signal for the PCM word generator (message) is taken from the most significant bit of the linear counter as shown. Therefore the clock frequency of the linear counter is eight times the message clock. Thus during a particular message available at the output of the PCM generator, the linear counter generates all the eight possible 3-bit words. Each time the linear counter reads '000', the PCM word generator receives a high-to-low pulse and generates a new message word. Now each time a new word is generated from the PCM word generator, it is continuously compared with all the states of the linear counter by the comparator circuit. When the counter generates the same 3-bit word as the PCM word, the comparator output goes to a high state. However, when the counter generates a different 3-bit word, the comparator output will remain low. It is evident that the PCM word will be exactly equal to one out of the eight possible 3-bit words generated by the linear counter in one message interval. Since the PCM word being different from the rest of the seven 3-bit words generated by the counter, the output of the comparator thus remains low during this time. This arrangement divides the message bit interval into eight different sub-intervals and outputs a high pulse on one of the sub-intervals during a message word interval. The position of the pulse depends upon PCM word. This high pulse is then transmitted as a DPPM signal. To clarify the operation, let us consider that the PCM word is '101' and the counter has started from '000'. After the counter receives five clock pulses, the counter reads '101'. When it is compared with the PCM data being already '101', the output of the comparator circuit goes high. For rest of the three states viz. 110, 111 and 000, the comparator output remains in '0' state. Thus a high pulse is transmitted for each message word. Hence the output signal is a DPPM signal.

III. RECEIVER CIRCUIT

The circuit diagram for digital PPM to PCM converter is shown in Fig. 3. The received DPPM signal is applied to one input of an AND gate. The other input of the AND gate is excited by the clock signal, synchronized with the clock signal used at the transmitter. The output of the AND gate generates sampling pulses for the latch circuit. The latch transfers the data to the output on receiving a low to high pulse.

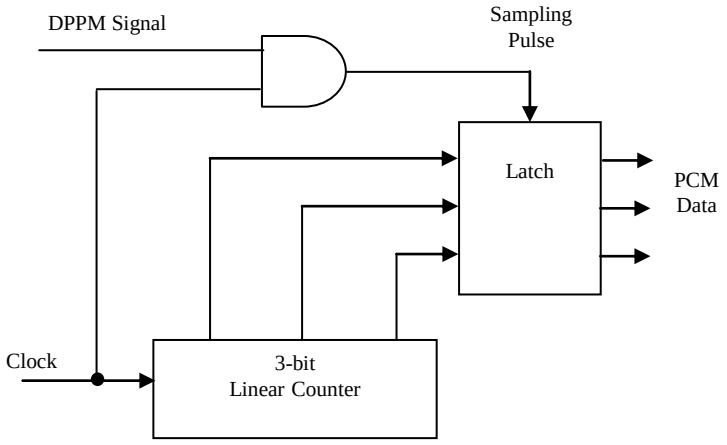

Fig. 3: Circuit layout of DPPM-to-PCM Conversion

The inputs of the chip are driven by the 3-bit linear counter. This counter is synchronized with the counter used at the transmitter i.e., the two counters read the same data at any instant of time. When the latch senses a low-to-high signal at its clock input, the data available at the output of the counter is transferred and latched at the output. Since a low-to-high pulse is generated at PCM-to-DPPM converter, when the counter output and the PCM data generator are same at the transmitter, therefore at the receiver, the same counter state is latched at the output on arrival of the corresponding DPPM pulse. Hence the DPPM signal is converted back into corresponding 3-bit PCM data.

IV. EXPERIMENTAL RESULTS

The proposed circuit has been implemented in hardware for performance evaluation. IC7493 was used as linear counter and IC74LS374 was used as latch. The word generator used in the system was implemented using JK flip-flops. The clock signal required by the circuit was given externally. Further, the clock signals used by the transmitter as well as the receiver were assumed synchronous with each other as the same clock was applied to both the systems for experimental purpose. Both linear as well as random data was used for the investigation. The results of experimental investigation conducted over the proposed scheme are shown in Fig. 4.

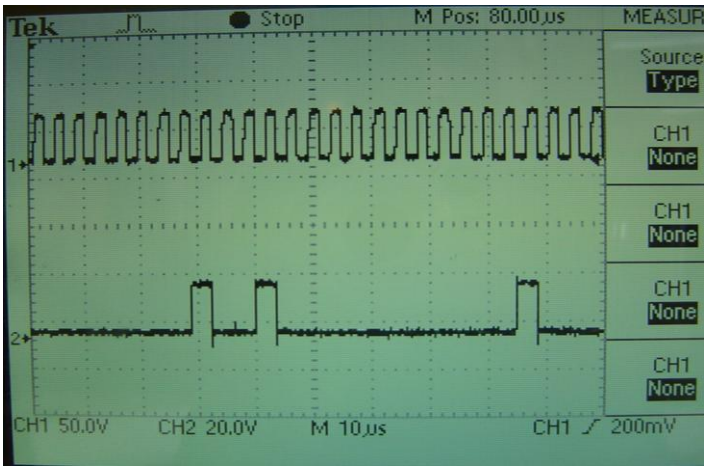

Fig. 4: (Upper: Clock signal)
(Lower: DPPM signal)

V. CONCLUSION

The tremendous bandwidth available with optical fibers (mono-mode) is not exploited by existing PCM systems. This excess of bandwidth can be exploited by DPPM, because DPPM offers much better performance and increased receiver sensitivity than PCM. A novel technique for PCM-to-DPPM conversion has been proposed in this paper. The proposed circuits were implemented in hardware and the results carried out over experimental investigation were satisfactory. Since the proposed scheme is implemented using purely digital circuits it can be suitable for IC implementation.

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