



Analytical Study of Sense Amplifier

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Abstract: The increased device variations, lower supply voltages have compelled the usage of sense amplifier circuit in Complementary Metal Oxide Semiconductor Random Access Memory (CMOS RAM). Voltage mode sense amplifier during read has been found one of the most promising solutions to reduce the power dissipation and increase the speed. Latch type voltage mode sense amplifier is presented. The presented latch type voltage mode sense amplifier technique can be used to reduce the power dissipation and delay. Analytical study and simulation results like dynamic power dissipation, leakage or static power dissipation, rise time effect on offset voltage, delay and effect of temperature on leakage have proposed.

Keywords: SAEN (sense enable signal), BB (bit-bar), BL (bit-line), SOC (system on chip)

I. INTRODUCTION

From the past few decades, the growth of the semiconductor industry is very fast and also the use of integrated circuits in various fields of electronics is increasing very fast. In today's world the number of device on the chip is increasing and the sizes are reducing. Also compatibility to CMOS logic process and its scalable nature have enabled the usage of embedded SRAM in 100s' of MB in the present day system-on-chip (SOC) applications. Owing to these facts, SRAM are occupying more than 70% of the final SOC area and hence SRAM's area, power, performance and leakage etc. became significant deciding factors in overall budgeting of SOC. With the increase in usage, system level requirements are imposing more constraints on SRAM design for improving key parameters like area, speed, leakage, dynamic power etc. The other important parameter associated with the SRAM design is yield [2]. SRAM cells are optimized to have maximum storage capacity and minimum device dimensions compared to any other device in the design to minimize the area and hence cost of IC. In the semiconductor memory the storage capacity can be increased by increasing the number of transistors to store the increased bits. Also if the number of transistors in a memory increased, the size of bit lines increased, due to this the time required to read/write the information from/to the memory increases as it depends on the time required to discharge/charge the bit lines. Hence by increasing the no. of transistors in memory, capacity increases but the memory access time increases. To achieve these two factors simultaneously, an accessory circuit called sense amplifier is used in SRAM. The use of sense amplifier in SRAM reduces the required time to access the memory. Also, the power dissipation is low. In this work latch type voltage mode sense amplifier is introduced. The latch type voltage sense amplifier is connected to the SRAM through bit lines as shown in figure1. Initially both bit lines BT and BB pre-charged to V_{dd} . Due to transistor action both the bit lines start to discharge. As pass transistor R1 and R2 are ON during this time, the value at bit lines (BT and BB) passes to the latch at node Sa0 and Sab0 respectively. When there is a sufficient voltage difference (which is above the offset voltage) the sense amplifier is activated by the sense enable signal. When the sense enable signal is provided by the control unit [4], the pass transistor R1, R2 turn OFF and latch is isolated from the bit lines. This transistor N3 provides the discharging path to the sense amplifier. Consider that node Sa0 has voltage $V_{dd}-\Delta$ (where ' Δ ' is small fraction of V_{dd}) and Sab0 has voltage V_{dd} . The two transistors N1 and N2 are symmetric. The N2 have more gate over drive voltage as compared to the N1 ($V_{dd}-\Delta < V_{dd}$), due to which the current flow through the N2 is more than the N1. Hence the value $V_{dd}-\Delta$ discharges more rapidly as compared to the V_{dd} .

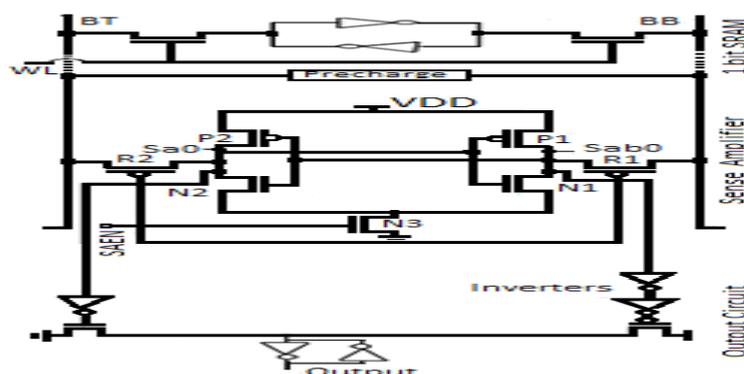


Figure1: Latch type sense amplifier with output circuit.

Initially, both the nodes Sa0 having voltage $V_{dd}-\Delta$ and Sab0 having voltage V_{dd} starts discharging, but as the node Sa0 discharge more rapidly the value $V_{dd}-\Delta$ approaches to zero rapidly. Due to this zero approaching value the transistor P1 turns ON and the node Sab0 again charge to V_{dd} . The output circuit (shown in figure1) is used with sense amplifier to store the value for external use. The number of sense amplifier used in memory is depends upon column multiplexer option.

II. SIMULATION RESULTS

The analytical study of the parameters like leakage, dynamic power, offset voltage variation, rise time effect on offset voltage, delay and effect of temperature on leakage was performed for SRAM cell.

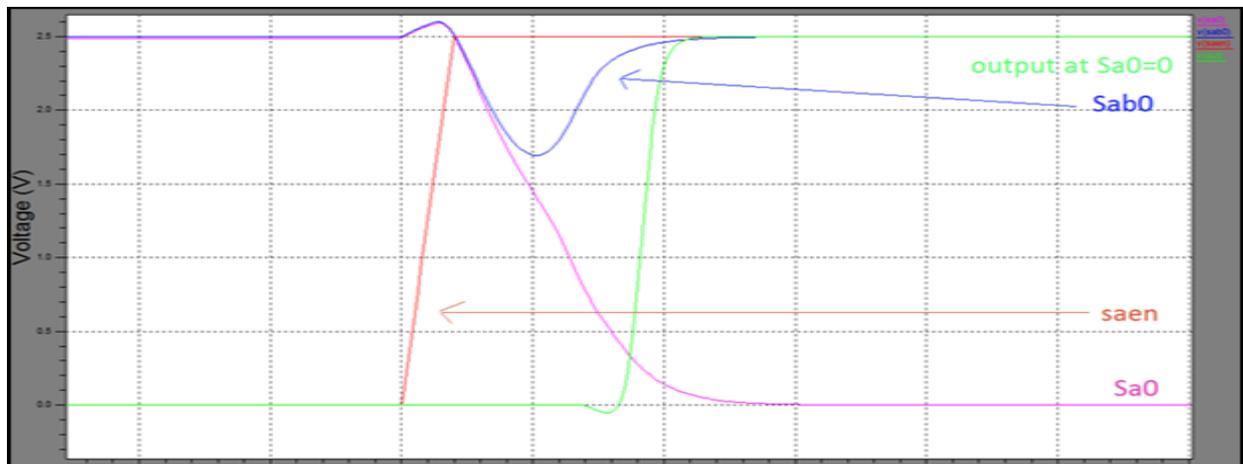


Figure2: Operation performed by sense amplifier

A. Offset

Offset is the minimum differential voltage between bit lines BT and BB which is required to operate the device in correct state. The offset of the sense amplifier can be varied or increased due to the mismatch in the transistor N1 and N2, pass transistor R1 and R2 [3]. The offset can also be reduced by reducing the size of tail transistor (N3) or by increasing the rise time of the sense enable signal. The offset is of two types namely intrinsic and extrinsic offset [3]. The offset contribution due to transistors N1 and N2 is termed as intrinsic offset. Suppose that N2 is weak transistor and N1 is strong transistor. When BT goes low, N1 will have larger gate voltage than N2, but smaller drain voltage than N2. When the difference between BT and BB is less than threshold voltage, both the transistors N1 and N2 are in saturation mode. The N2 can have more drain current, even if N2 is weak and N1 is strong, provided BT is suitably lower than BB. Because of higher drain current of N2, Sa0 will discharge more rapidly and sense amplifier will latch into the correct state. The difference in drain currents of two transistors N1 and N2 resulting from V_{th} and β variations causes the intrinsic latch offset. These variations can be due to process variations such as random dopant number fluctuations, interface-state density fluctuations etc [7, 8]. The intrinsic offset of the sense amplifier increase with the increase in the mismatch between transistors N1 and N2. The offset contribution due to the pass transistors R1 and R2 is termed as the extrinsic offset. The extrinsic offset in the sense amplifier can be considered or can be neglected, depending upon driving signal of the three transistors R1, R2 and N3.

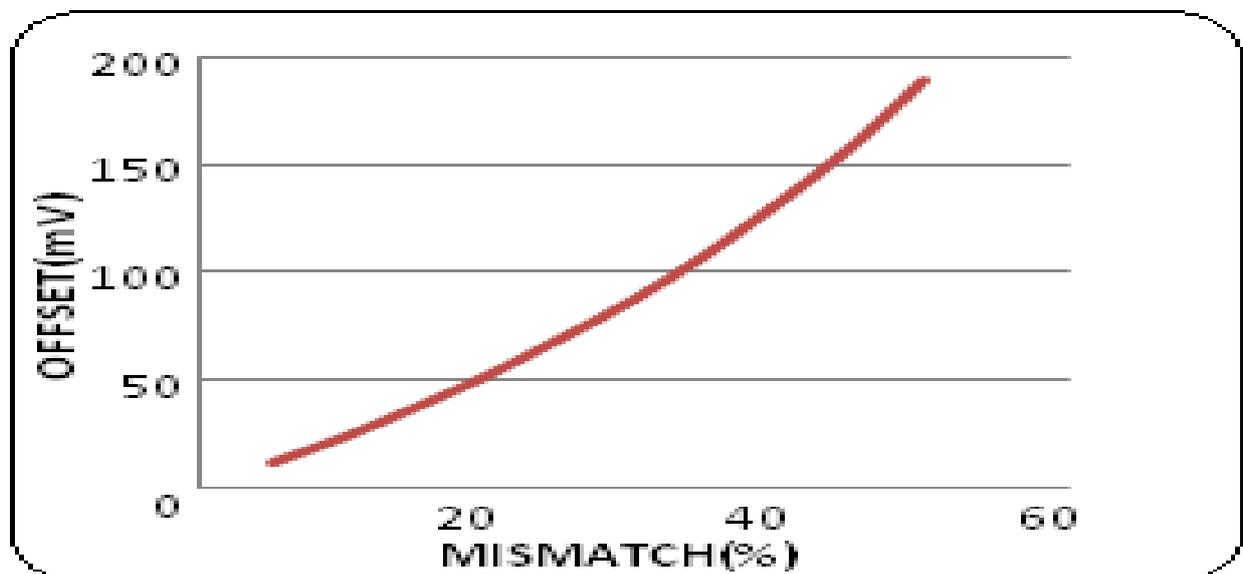


Figure3: Effect of mismatch on the offset

The driving signals of N3 and pass transistors R1, R2 can be given separately by the control unit. The pass transistors should turn OFF before or at the same time, when transistor N3 turns ON. If there is some delay in the turning OFF the pass transistors, the extrinsic offset will contribute in the total offset of the sense amplifier. The driving signals of transistors N3, R1 and R2 in the sense amplifier which is designed here are given at the same time by the control unit. Therefore, the extrinsic offset is neglected in this work, because the pass transistors R1, R2 are in OFF state, when the transistor N3 is activated. The total sense amplifier offset is the sum of these two offsets.

B. Effect of rise time and size of tail transistor on offset

The offset of sense amplifier can be compensated in the two ways. Firstly by disturbing the slope of rise time of the sense enable signal. The slope is disturbed to increasing the rise time of sense enable signal due to which the tail transistor (N3) becomes weak. By increases the rise time of sense enable signal the offset of the sense amplifier decreases. Secondly, the offset of sense amplifier can be decreases with decrease in size of tail transistor (N3).

It is clear that by reducing the size of tail transistor offset can be reduced, but by reducing the size, the discharging path weakens.

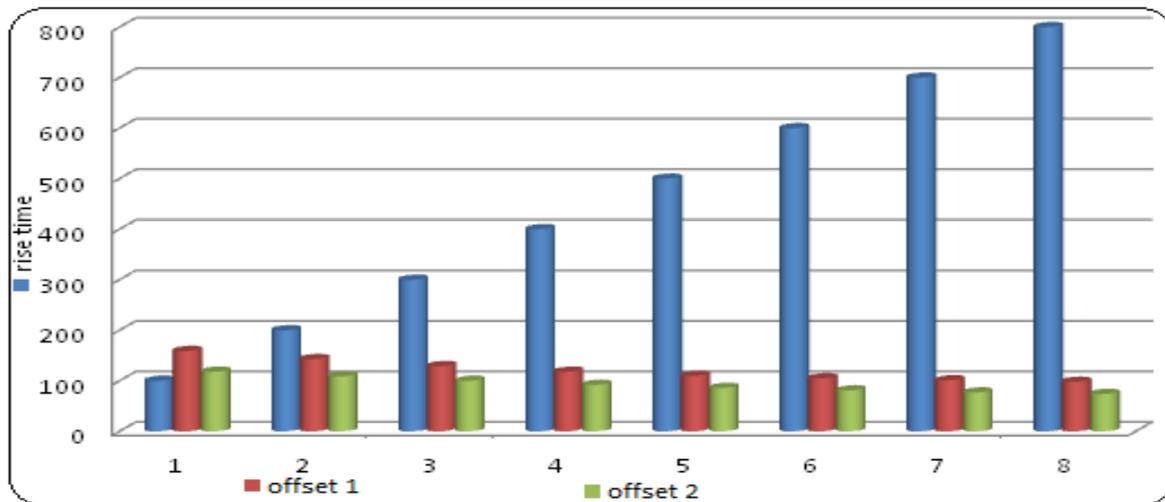


Figure4: Offset versus Rise time plot for different sizes of tail transistor

Hence for discharging the value through N1 and N3 or N2 and N3, time consumed will be more. Therefore the size of tail transistor is selected in accordance with the application, whether the fast discharging or the lower offset is required.

C. Delay Analyses

The propagation delay time (τ_p) determines the input to output signal delay during the high to low and low to high transitions of the output. By definition, τ_{PHL} is the time delay between the $V_{50\%}$ transition of the rising input voltage and the $V_{50\%}$ transition of the falling output voltage. Similarly, τ_{PLH} is defined as the time delay between the $V_{50\%}$ transition of the falling input voltage and the $V_{50\%}$ transition of the rising output voltage. The average propagation delay (τ_p) of the inverter characterizes the average time required for the input signal to propagate through the inverter. Simply, the delay is the time difference between input and output that is after how much time the output is obtained corresponding to particular input. The time consumed between input and output can be due to the time required to overcome the offset voltages. By increasing the differential input between the bits lines BT and BB the delay can be reduced.

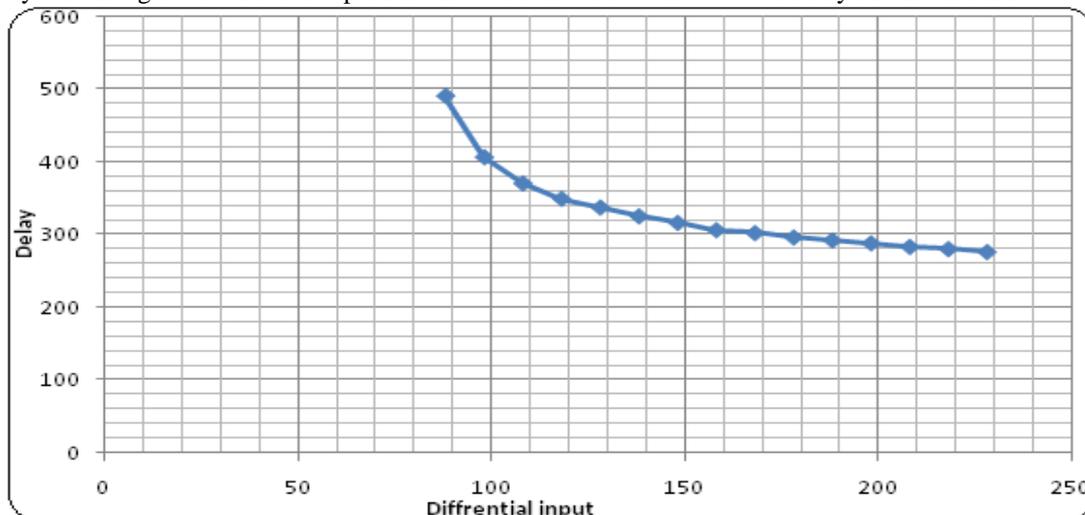


Figure5: Effect of differential input on delay

D. Analyze Static power or Leakage power

The static power is the power required by the device in the ideal state that is in non working stage. It is also termed as leakage[1]. The NMOS and PMOS transistors used in the CMOS logic gate generally have nonzero sub-threshold currents. The sub threshold is the leakage current which flows in weak inversion region. Ideally, when gate source voltage is below the threshold voltage, no current flows between source and drain. But, in reality, little current flows due to minority carriers in that region. In a CMOS VLSI chip containing a very large number of transistor, these currents can contribute to the overall power dissipation even when the transistor are not undergoing any switching events. Leakage or static power is directly proportional to the leakage current and operating voltage.

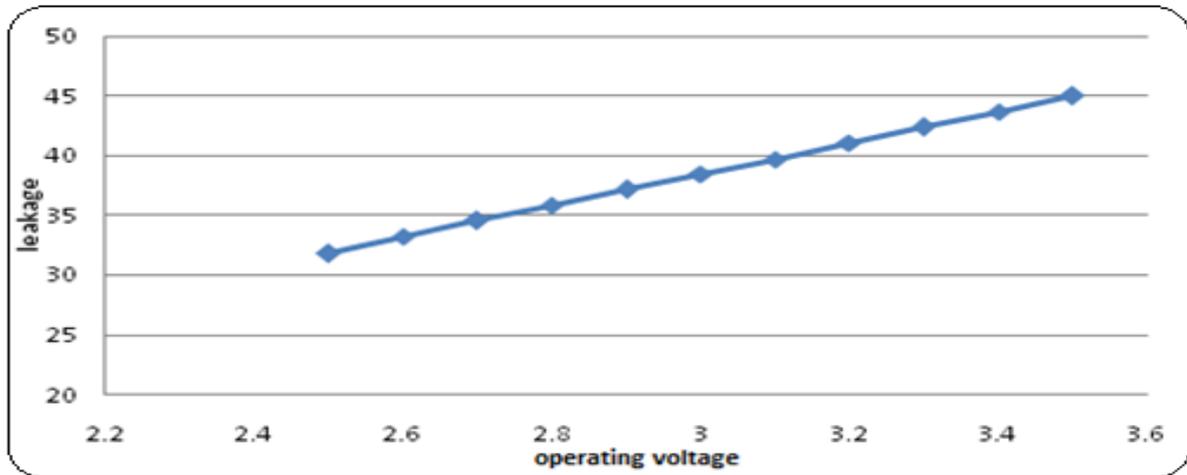


Figure6: Leakage versus operating voltage.

As operating voltage increases, the leakage also increases. The current flow, when the sense enable signal is low, is the leakage current. The leakage in the transistors can be resulted due to body effect, DIBL effect or narrow width effect [1].

E. Analyses of Dynamic power

The dynamic power of a device increases with the increase in the operating voltage. In digital CMOS circuits, switching power is dissipated when energy is drawn from the power supply to charge up the output node capacitance. During this charge-up phase, the output node voltage typically makes a full transition from 0 to V_{dd} and one-half of the energy drawn from the power supply is dissipated as heat in the conducting PMOS transistors. Note that no energy is drawn from the power supply during the charge-down phase, yet the energy stored in the output capacitance during charge-up is dissipated as heat in the conducting NMOS transistors, as the output voltage drops from V_{dd} to 0.

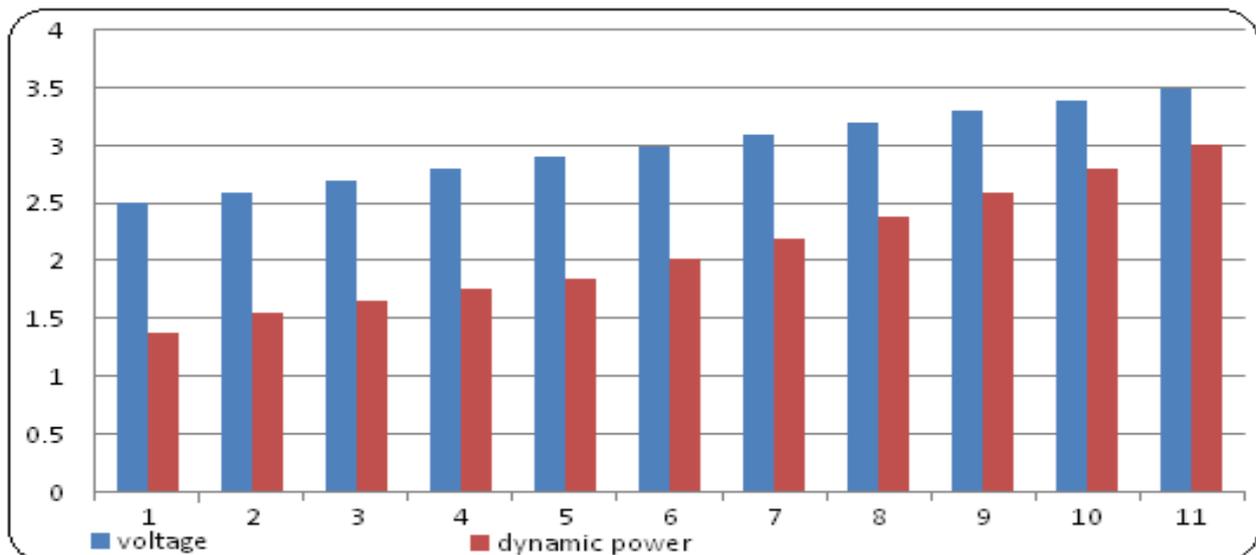


Figure7: Operating voltage versus dynamic power

F. Effect of temperature on leakage

Temperature dependence of the sub-threshold leakage current is important, since very large scale integration (VLSI) circuits usually operate at elevated temperatures due to the power dissipation (heat generation) of the circuit. The sub-threshold leakage increases exponentially with rise in temperature as threshold voltage decreases linearly with rise in temperature [1].

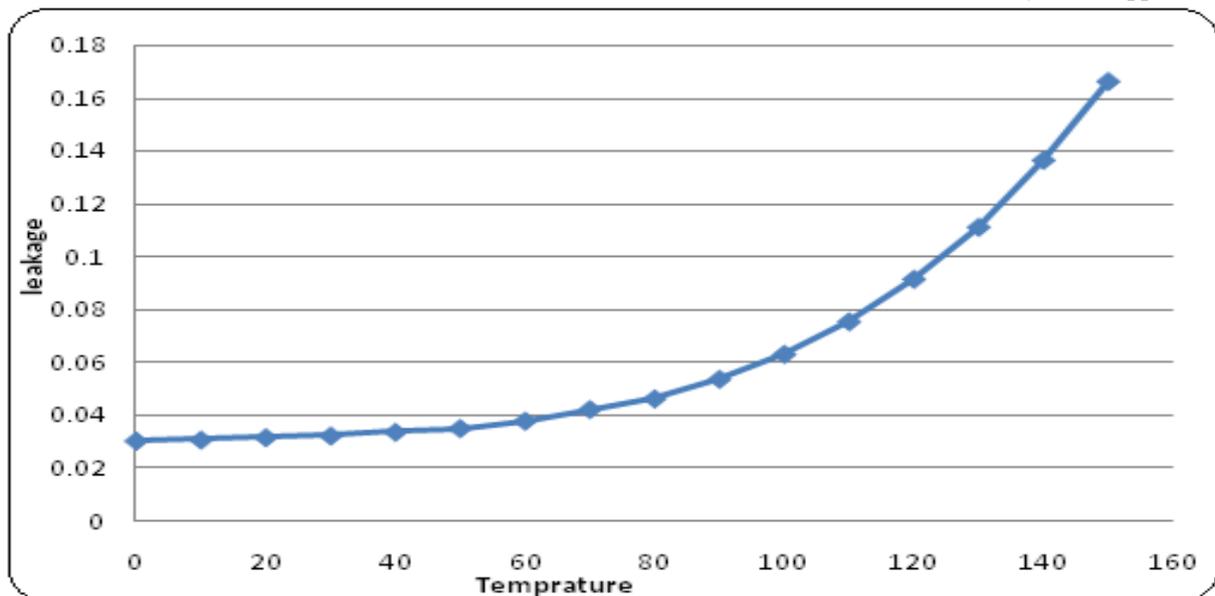


Figure8: Effect of temperature on the leakage

When the temperature is less, the leakage across the sense amplifier is small. The leakage increases as the temperature rises.

III. CONCLUSION AND FUTURE WORK

The sense amplifier design and analysis were presented. The schematics were designed and simulated. In the simulation part, the effect of mismatch on the offset was studied. An offset compensation through the slope control of sense-amp enabling signal was studied and analyzed. It is found that for higher SRAMs, the slower SAEN signal can result in low power dissipation as well as high speed operation. The effect of differential input on the delay, effect of operating voltage on the leakage, effect of operating voltage on the dynamic power, effect of temperature on the leakage was studied through SPICE simulations. This work was primarily on Sense-amplifier design for SRAM applications. Because of their small sizes, SRAM use voltage sense-amplifiers and current sense-amplifier is normally not used in SRAMs [5, 9]. However there are other flavors of memory like DRAM, flash memories whose bit-lines are very-very large and current amplifier shows benefit over voltage sense-amplifiers [6, 10]. A study similar to presented in this work may be performed on current sense-amplifiers for those applications.

REFERENCES

- [1]. Kaushik Roy, fellow, IEEE, Saibal Mukhopadhyay, student member, IEEE, and Hamid Mahmoodi-Meimand, student member, IEEE "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Sub micrometer CMOS Circuits" Proceeding of the IEEE, VOL. 91, NO. 2, February 2003.
- [2]. B. Wicht, Thomas Marsche, Doris Schmitt-Landsiedel, "A Yield-Optimized Latch type SRAM Sense Amplifier"
- [3]. Ravpreet Singh, and Navakanta Bhat, Senior Member IEEE "An Offset Compensation Technique for Latch Type Sense Amplifiers in High Speed Low Power SRAMs" TVLSI-0073-2002.R3.
- [4]. Jaume Segura Charles F. Hawkins, CMOS Electronics, IEEE Press, 2004.
- [5]. Igor Arsovski, "High-Speed Low-Power Sense Amplifier Design", 2001.
- [6]. Birinderjit Singh Kalyan, Amit Verma, Inderpreet Kaur, Iqbaldeep Kaur, "Low power high speed current sense amplifier", IJCST, September 2010
- [7]. K. A. Bowman, X. Tang, J.C.Eble, J.D.Meindl, "Impact of extrinsic and intrinsic parameter fluctuations on CMOS circuit performance", IEEE J,Solid-State Circuits, vol. 35, August 2000.
- [8]. P.A. Stolk and D.M. Klaassen, "The effect of statistical dopant fluctuation on MOS device performance", IEDM Dig. Tech. Papers, 1996.
- [9]. L. F. Rahman, MBI. Reaz, M.A.M. Ali, M. Marufuzzaman "Implementation of sense amplifier in 0.18 μ m CMOS process" ISSN 1392-1215.
- [10]. M Sinha, S Hsu, S Bookar "High performance and low voltage sense amplifier techniques for sub 90nm SRAM".