Volume 4, Issue 4, April 2014 ISSN: 2277 128X
International Journal of Advanced Research in Computer Science and Software Engineering
Research Paper
Available online at: www.ijarcsse.com

Low Power Active Noise Cancellation System using an Adaptive Filtering Configurations on Reconfigurable Platform

Dipen B. Patel*
ME Student,
Digital Electronics
Sipna College of Engineering & Technology, Amravati
India

Pritesh R. Gumble
Associate Professor,
Electronics & Telecommunication Department
Sipna College of Engineering & Technology, Amravati
India

Abstract— This paper proposed the implementation of adaptive filters on reconfigurable platform i.e. FPGA with the application of low power active noise cancellation. Adaptive filter is an essentially digital filter with self adjusting characteristics. It adapts, automatically, to change in its input signal. Adaptive filter are central topic in the sub-area of DSP known as adaptive signal processing. An adaptive filter has the property that its frequency response is adjustable or modifiable automatically to improve its performance in accordance with some criterion, of their self adjusting performance and in-built flexibility, adaptive filters have found use in many diverse applications such as telephone echo cancelling, radar signal processing, navigation systems, equalization of communication channels, and biomedical signal enhancement. In this paper we have made an attempt to implement adaptive LMS algorithm in noise cancellation system which is hardware configurable on low power view point.

Keywords— LMS Adaptive Filter; Noise cancellation system; Adaptive filter structure for Noise suppression; LMS algorithm systolic array architecture, Low Power Adaptive Filter

I. INTRODUCTION

Adaptive algorithms are typically algorithms for optimization. In contrast to classic optimization problems, adaptive filter algorithms try to find optima in permanently change in environment. Obtaining the best design usually requires a priori knowledge of certain statistical parameters such as the mean and correlation functions within the useful signal. With this information, an optimal filter can be designed which minimizes the unwanted signals according to some statistical criterion. One popular measure involves the minimization of the mean square of the error signal, where the error is the difference between the desired response and the actual response of the filter. However, it is only optimum when the statistical characteristics of the input data match the priori information from which the filter is designed, and is therefore inadequate when the statistics of the incoming signals are unknown or changing, i.e. in a non stationary environment. For this situation, a time-varying filter is needed to allow for these changes. When the input signals are stationary the algorithm will converge to the optimum solution after a number of iterations, according to the set criterion. If the signals are non-stationary then the algorithm will attempt to track the statistical changes in the input signals, the success of which depends on its inherent convergence rate versus the speed at which statistics of the input signals are changing. Fig.1 shows the Generalized Adaptive Filter structure; an input signal x(n) fed into both the linear filter and also the adaptive algorithm. The output from the adaptive linear filter is y(n), an estimation of the desired signal, d(n).

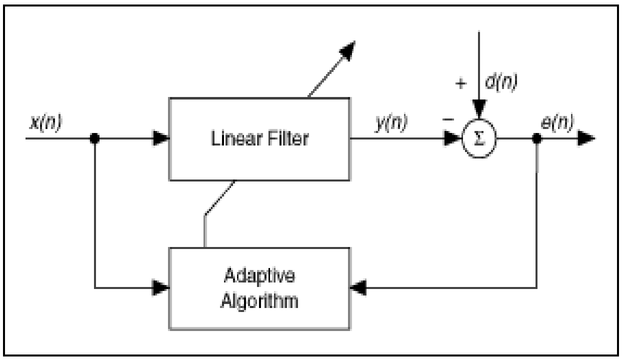

Fig. 1. Adaptive Filter system block

The difference between d*(n)* and y(n) gives an error signal e(n). The adaptive algorithm uses this signal and the input signal x(n) to calculate updates for the filter weights w(n). This generalized adaptive filter structure can be applied to a range of applications. When there is spectral overlap between the signal and noise, if the band occupied by the noise is unknown or varies with time. The use of conventional filters in the above cases would lead to unacceptable distortion of the desired signal [8].

II. ADAPTIVE FILTER STRUCTURE FOR NOISE CANCELLATION

A. Adaptive Filter structure

An optimal filter can be designed which minimizes the unwanted signals according to some statistical criterion. One popular measure involves the minimization of the mean square of the error signal, where the error is the difference between the desired response and the actual response of the filter. In general, any system with a finite number of parameters that affect how y(n) is computed from x(n) could be used for the adaptive filter in Fig. 1. Define the parameter or coefficient vector W(n) as, $W(n)=[W_o(n)\ W_1(n)\ldots\ldots W_{L-1}(n)]^T$. Where, $\{Wi(n)\}, 0 \le i \le L-1$ are the L parameter of the system at time n. The general input output relationship for adaptive filter are,

y(n)= f(w(n), y(n-1), y(n-2), …… y(n-N), x(n), x(n-1), x(n-2),…. x(n-M+1)) where f(.) represents any well defined linear or non linear function and M and N are positive integer. in determining the best linear relationship between the input and desired response signals for many problems. This relationship typically takes the form of a finite-impulse-response (FIR). Fig. 2. shows the structure of a direct-form FIR filter, also known as a tapped-delay-line or transversal filter, where Z^{-1} denotes the unit delay element and each $W_i(n)$ is a multiplicative gain within the system [6]. We can write the output signal y(n) as

$$y(n) = \sum_{i=0}^{L-1} w_i(n)x(n-i) = \mathbf{W}^T(n)\mathbf{X}(n),$$

Where, $x(n)=[\ x(n), x(n-1), x(n-2),\ldots x(n-L+1)]^T$ denotes input signal vector.

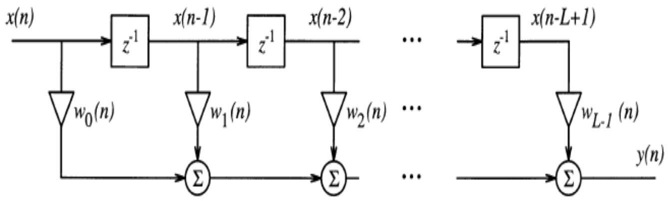

Fig. 2. Structure of an FIR filter

this system requires L multiplies and L − 1 adds to implement, and these computations are easily performed by a processor or circuit so long as L is not too large and the sampling period for the signals is not too short. It also requires a total of 2L memory locations to store the L input signal samples and the L coefficient values, respectively.

B. Adaptive Algorithm

The key aim of the adaptive filter is to minimize the error signal e(n). The success of this minimization will clearly depend on the nature of the input signals, the length of the adaptive filter, and the adaptive algorithm used. The LMS algorithm does not require measurement of correlation and cross correlation function and matrix inversion. [7], [8].

the Least Mean Square algorithm, whose weight updating equations are as

$W_{k+1} = W_k + 2\mu\ e(k)\ x(k)$ where, $e(k) = d(k) - x^T(k)\ w(k)$.

Typically, one iteration of the LMS requires N + 2 multiplications for the filter coefficient updating and N + 1 multiplications for the error generation. The convergence factor or step size, μof the LMS algorithm must be chosen in the range $0 < \mu < (1/\lambda_{max})$, Where, λ_{max} is largest Eigen value of correlation of Input signal.

C. Application of Adaptive Filter - Noise Cancellation

The structure of adaptive noise cancellation is given in Fig. 3. The structure is slightly different. The reference signal in this case is the data x(k) corrupted with a noise signal $n_1(k)$. The input to the adaptive filter is a noise signal $n_2(k)$ that is strongly correlated with the noise $n_1(k)$, but uncorrelated with the desired signal x(k). [9]. A particular example is the removal of the mother's heartbeat from the ECG trace of an unborn child. In this application, the error signal is given by,

$$e(k) = x(k) + n_1(k) - \sum_{l=0}^{N} w_l n_2(k-l) = x(k) + n_1(k) - y(k)$$

where error signal is the expected desired signal. In some applications, it is useful to include a delay of L samples this delay provides a kind of synchronization between the signals involved.

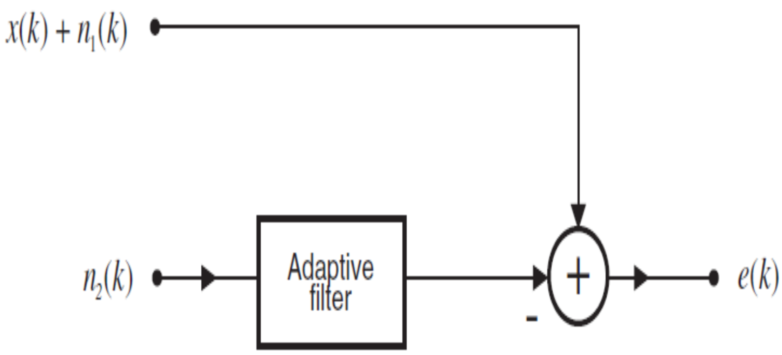

Fig. 3. Noise Cancellation System Block

III. Design & Implementation of Active Noise Cancellation System

Generally signal of interest is linearly mixed with other extraneous noises in the measurement process, and these extraneous noises introduce unacceptable errors in the measurements [3]. However, if a linearly related reference version of any one of the extraneous noises can be cleanly sensed at some other physical location in the system, an adaptive filter can be used to determine the relationship between the noise reference and the component of this noise that is contained in the measured signal. After adaptively subtracting out this component, what remains in is the signal of interest. Fig. 4. Shows the generalized block diagram for the active noise cancellation adaptive filtering system. Where Input Signal to the adaptive filter is the background active noise signal and desired signal is the voice signal from microphone s(k) and its contaminated with the background noise n(k). The output of the adaptive filter is of error out which eliminate the noise signal from the voice signal from microphone and shows the desired output signal. The above stated system is hardware configured on FPGA and also simulate on the Xilinx ISE.

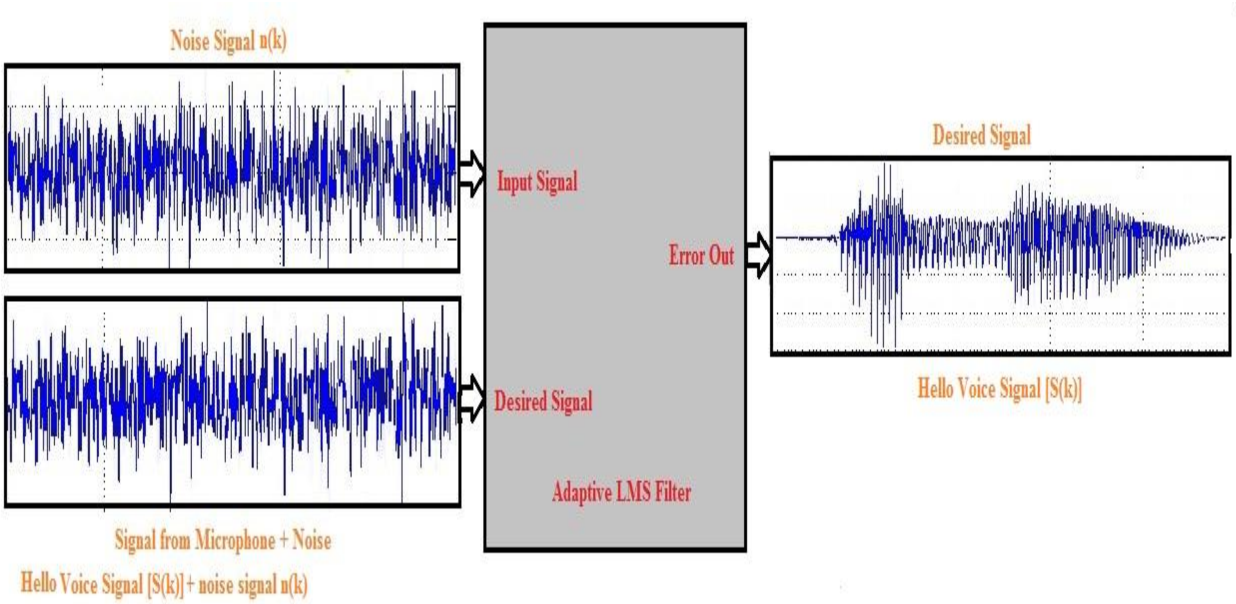

Fig. 4. Adaptive Filter System: Noise Cancellation

This adaptive digital filter for noise canceller can be design on reconfigurable FPGA platform using the 40 tap digital filter which adapts the weight by means of adaptive LMS algorithm which is configured in the systolic array architecture form, which reduce the circuit scale into half without impairing the processing speed [2]. Systolic arrays represent a bottle neck architecture in which the adaptive algorithm calculations are performed in parallel. Implementing such adaptive filter architecture by arranging circuits (cells) that perform individual, calculations in a regular pattern and the data required for the calculation are feed to such cell in a pipelined manner. This parallel approach can improve the processing speed to a large extent and the uniform structure provides excellent expandability. Fig. 5. shows the architecture used for implementing the LMS algorithm using systolic arrays, shows a case with four array elements. x1(i), x2(i), x3(i) and x4(i) represent the ith sample point of the signals of each element and y(i) represents the ith sample point of the reference signal used for identifying the desired signal.

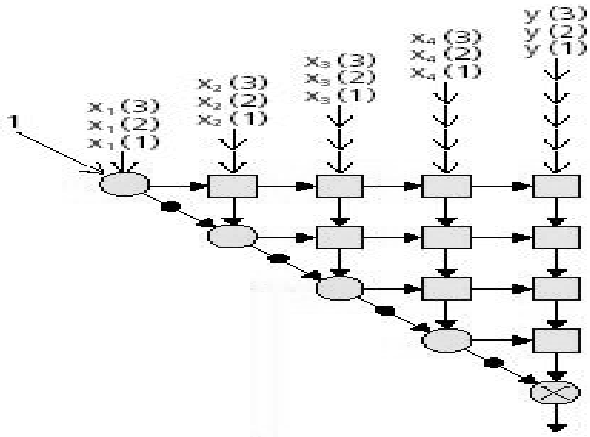

Fig. 5. Systolic array architecture

All cells operate under the control of a single clock, and the data propagates through the cell arrays in synchronization with this clock, each data point addition, and multiplications of numbers are included in the internal cell processing.

IV. CLOCK GATING TECHNIQUE

Low-power techniques are essential in modern VLSI design due to the continuous increase of clock frequency and chip

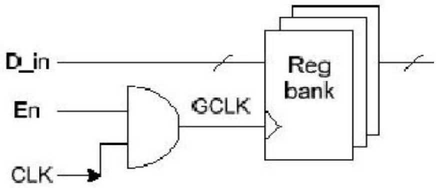

Fig. 6. Clock gating technique

complexity. As a consequence many techniques have been proposed to reduce clock system power dissipation.
Disabling the clock signal (clock gating) in inactive portions of the chip is a useful approach for power dissipation reduction. Clock gating can be applied to different hierarchical levels. Clock gating principle involves in freezing the clock to the portions of a design that are ideal or are not performing useful computations. The Fig. 6 describes the concept of clock gating. Independent blocks when clock gated, it greatly affects power savings because gating larger blocks achieves in higher power savings in 'off' clock cycle.

V. RESULT

The signals used in the verification of the workability of the noise canceller LMS algorithm based adaptive filter are a speech signal acoustical environment. The noise signal is a Gaussian noise with mean 0 and variance of 0.1. A 40 tap direct form structure FIR filter has been used to simulate the unknown noise path in the Acoustic Environment by means of LMS algorithm which is in systolic array architecture form. HDL simulation provided in Xilinx ISE, Hardware Description Language (HDL) simulation result has been setting up shown in Fig. 7.

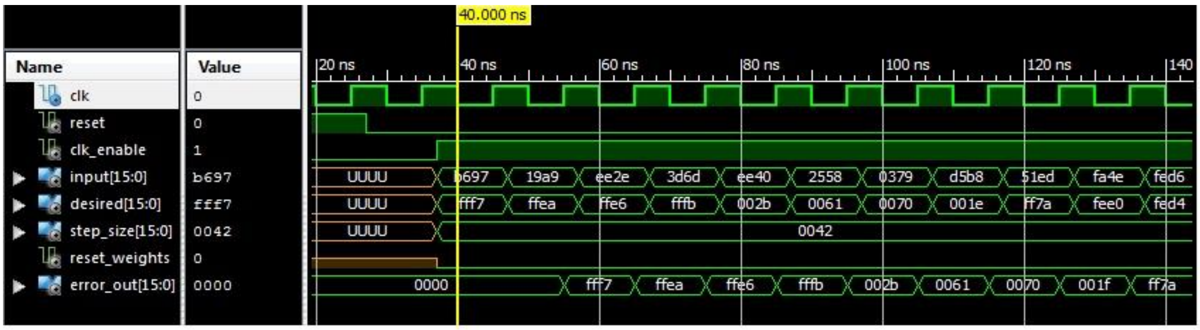

Fig. 7. Xilinx ISE Simulation result of the Noise cancellation system using LMS adaptive filter

The Xilinx ISE simulator has been used to simulate the design at various stages. Xilinx synthesis tool (Xilinx ISE 13.1 version) has been used to synthesize the design for Spartan family FPGA. As the present implemented structures makes use of only VHDL constructs the work also brings out fundamental design goals in FPGA based design with systolic architecture usage.

.

Project File:	lmsorig.xise	**Parser Errors:**	No Errors
Module Name:	lms	**Implementation State:**	Synthesized
Target Device:	xc6slx100-3fgg484	**• Errors:**	No Errors
Product Version:	ISE 13.1	**• Warnings:**	16 Warnings (16 new)
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	1312	126576	1%
Number of Slice LUTs	7106	63288	11%
Number of fully used LUT-FF pairs	662	7756	8%
Number of bonded IOBs	69	326	21%
Number of BUFG/BUFGCTRLs	1	16	6%
Number of DSP48A1s	121	180	67%

Fig. 8 Synthesis Report

Fig. 8 shows the synthesis report for the active noise cancellation system using adaptive LMS algorithm which clarifies the stated design is hardware configurable and optimized power report using Xilinx Xpower tool is shown in Fig. 9. The Clock Gating Technique implemented on design which optimize the dynamic power of the system the detailed

Device		On-Chip	Power (W)	Supply Summary		Total	Dynamic	Quiescent
Family	Spartan6	Clocks	0.028	Source	Voltage	Current (A)	Current (A)	Current (A)
Part	xc6slx100	Logic	0.109	Vccint	1.200	0.385	0.336	0.048
Package	fgg484	Signals	0.146	Vccaux	2.500	0.012	0.001	0.010
Grade	C-Grade	DSPs	0.119	Vcco25	2.500	0.026	0.021	0.005
Process	Typical	IOs	0.058			Total	Dynamic	Quiescent
Speed Grade	-3	Leakage	0.096	Supply Power (W)		0.557	0.460	0.096
		Total	0.557					

Fig. 9 Active Noise Cancellation system Power Report.

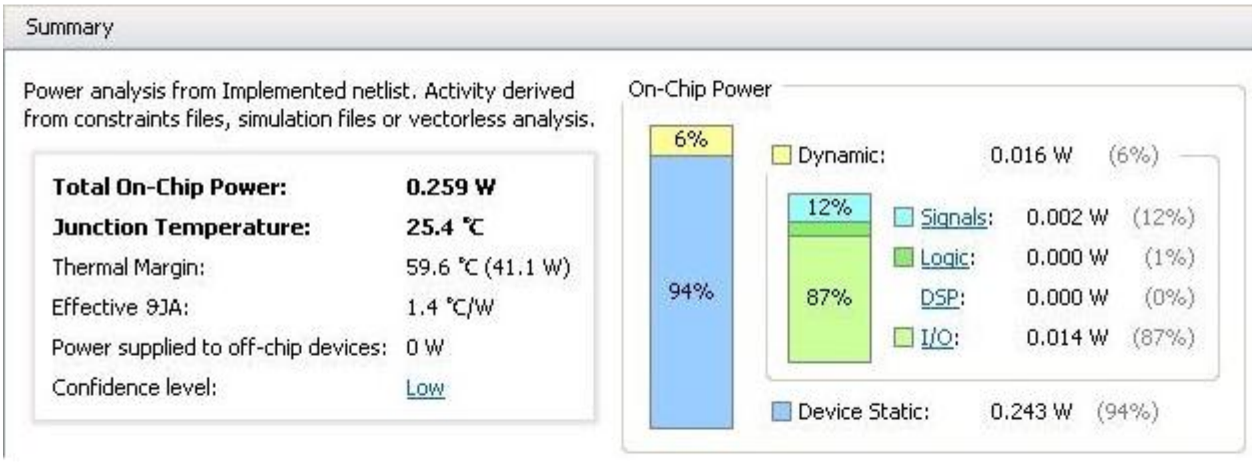

Fig. 10 Power Analysis for Clock Gating Technique

power analysis report using Xilinx Vaivado 13.4 tool is shown in Fig. 9(b). Which shows the low power design of active noise cancellation system on FPGA.

VI. CONCLUSIONS

This article described the implementation and evaluation result of the LMS algorithm in the application of active noise cancellation system using FPGA technology. The adaptive filter system architecture is proposed systolic array architecture can reduce the circuit scale into half without impairing the processing speed with the optimized power by using clock gating technique. In the future, we intend to investigate the applications of adaptive filter configurations in biomedical area with the blind adaptive filter algorithm.

ACKNOWLEDGMENT

We would like to acknowledge the Faculties of Electronics & Telecommunication Department, Sipna College of Engineering & Technology, Amravati for their support. I, Dipen B. Patel specially want to thank my guide Prof. Pritesh R. Gumble for their guidance and constant encouragement towards the work.

REFERENCES

[1] M.S. Sutaoane, M.B. Mali and S.R. Deo, "VLSI Implementation Of Adaptive Filter On Reconfigurable Platform" SPIT-IEEE Colloquium and International Conference.
[2] Lan-Da Van,Wu-Shiung Feng on "An Efficient Systolic Architecture for the DLMS Adaptive Filter and Its Applications"IEEE Transactions On Circuits & Systems.
[3] Lei Wang and Naresh R. Shanbhag, "Low-Power Filtering via Adaptive Error-Cancellation" IEEE Transactions On Signal Processing.
[4] T. Rissa, R. Uusikartano, J. Niittylahti, "Adaptive FIR filter architectures for run-time reconfigurable FPGAs," IEEE International Conference on Field-Programmable Technology.
[5] Ankit Jairath, Sunil Kumar Shah, Amit jain, "Design & implementation of FPGA based digital filters" IJARCET.
[6] Douglas, S.C. "Introduction to adaptive filters", Digital signal processing handbook.
[7] S. Haykin, Adaptive Filter Theory. Upper Saddle River, NJ: Prentice Hall, 1996.
[8] E.C.Ifeachor and B. W. Jervis, Digital Signal Processing, A Practical Approach, Prentice Hall, 2002.
[9] Paulo S. R. Diniz "Adaptive Filtering Algorithms and Practical Implementation" Third Edition Kluwer Academic Publishers.

[10] Ying Heet al. (2008),,,The Applications and Simulation of Adaptive Filter in Noise Cancelling", International Conference on Computer Science and Software Engineering, IEEE, 1-4.
[11] Roger woods, John McAllister, Gaye Lightbody, Ying Yi, "FPGA based Implementation of signal processing system" A John Wileyand sons Ltd., Publication
[12] Vinay K. Ingle, John G. Proakis, "Digital Signal Processing using MATLAB" The PWS publisher.

