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Flash Memory Controller

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Abstract-Flash memory controller is interfaced with flash memory. It handles all signals required by the flash memory. With the required signals different types of commands are also sent through flash memory controller to the flash memory. For each operation such as PROGRAM, READ,ERASE certain type of sequence is need to be generated to perform specific operation on flash memory. When any other system is required toperform read or write operation onto the flash memory, it has to communicate with flash controller.This paperfocuses on design of NOR based Flash Memory Controller in VHDL.

Keywords- NOR flash memory, commandsequence, flash memory controller, command decoder,FIFO

I. INTRODUCTION

There are two types of flash memories are availablei.e. NOR based and NAND based. Different types of series and parallel NOR flash memory chips are available.This paper focuses on design for parallelNOR based flash memory controller. Figure 1 and figure 2 shows the general blocks which are used to in flash memory controller. The program address, program data and operation which is to be performed are sent from the other system to the flash memory controller. It performs command decoding, signal generation and send those to the flash memory [2].

Rest of the paper is organized as, second section introduces different blocks which are used in the designing of flash memory controller. Third section describes the command decoding formats used in the designing. Fourth section contains, the results of implemented blocks followed by conclusion.

II. FLASH MEMORY CONTROLLER

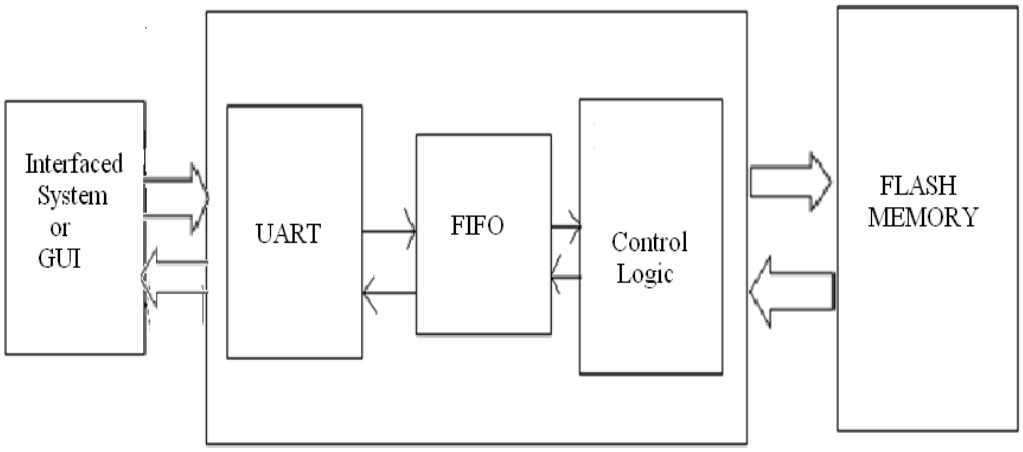

Figure 1: General diagram of Flash memory controller

With reference to figure 1, data, address and operation are the inputs to the flash memory controllerwhich are sent from interfaced system or from GUI. This data bits are transmitted serially to the UART. Then received data, address and operation are stored in FIFO. Control logic generates required signal for flash memory. While read operation is done data read from flash memory is sent to interfaced system or to GUI through control logic, FIFO and UART [4].

Figure 2 shows detailed block diagram of flash memory controller. Working and use of each block is as follows.

A. Interfaced system or GUI :

This system sends the information related to operation, address, data to the flash controller. Interfaced system and GUI send this information serially. While read operation is there data sent from flash memory is passed to interface system or to GUI through flash memory controller.

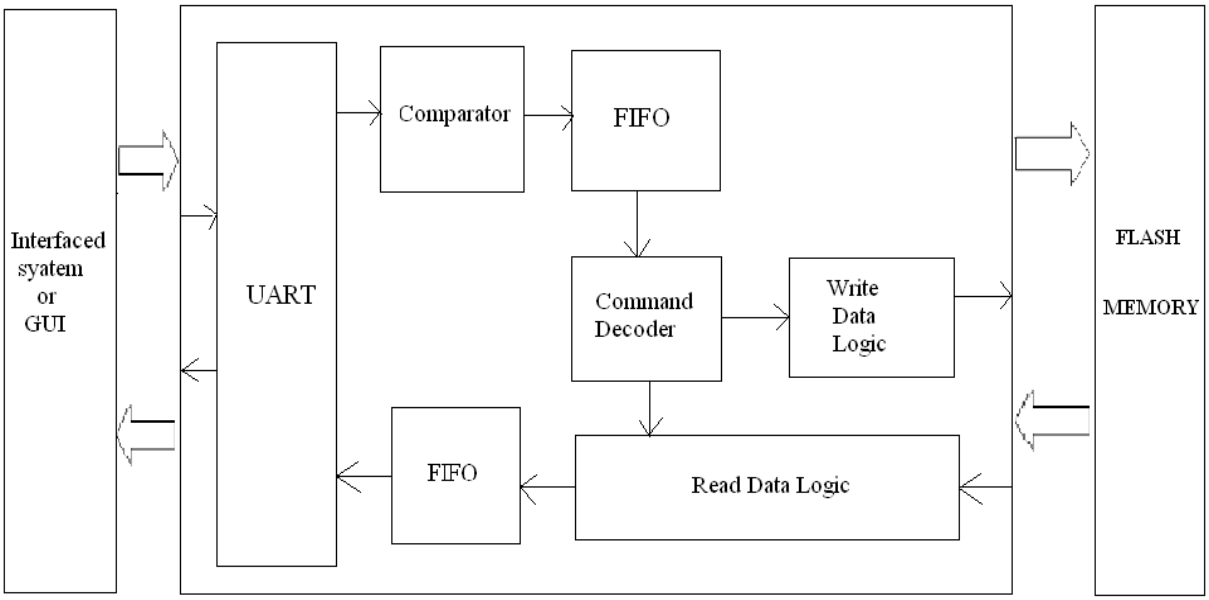

Figure 2: Block Diagram of Flash Memory Controller

B. UART :

It receives command,address and all other necessary information serially. It separates the incoming bit stream into four operands such as

- Command start bits
- Encoding bits
- Program address bits
- Program data bits

C. Comparator :

It checks the command start bits. For each valid command the command start bits are sent through the interface system or through GUI. For the design I have selected the start bit as 0xABh. If the received sequence is followed by the command start bit 0xABh then and then only the all other operands such as encoding bits, Program address, program -data are given to FIFO.

D. FIFO :

FIFO is used to store the incoming encoding bits, program address bits and program data bits. Sometimes flash memory goes into busy state, at that time control unit should remain idle and incoming commands from UART are need to be stored for further working of flash memory controller. After receiving valid command in FIFO generates enable signal to start the command decoder. With the start signal it gives all three stored operands to the command decoder. The Operands are encoding bits, program address bits and program data bits.

E. Command Decoder :

It receives encoding bits from FIFO. Depending on this encoding bits command decoder generates the command sequence with address and data cycle as per the requirement of flash memory. There are different standard command definitionfor the flash memory such as READ/RESET Command, PROGRAM Command, ERASE command. For each of these standard command sequence encoding bits are used which by forgets the command decoder to know which command is received and which type of address and data sequences are to be generated.

F. Write Data Condition:

Write data condition generates the signals which are required by the flash memory. For the flash memory different signals are required such as CE, WE, OE, Address, Data. Figure 3 shows the block diagram of parallel NOR flash memory. All the required signals are generated by the write data condition module. The paper focuses the design of flash memory controller for parallel NOR flash memory controller(M29W128GH). Memory requires different address – data cycles with specified timings of CE, WE, OE and other signals. Command decoder decides which address and data cycles have to be sent and in which sequence that are to be sent. But different signals required by the flash memory are generated with specified timings at write data condition module.

G. Read Data Condition :

When there is an read operation is selected by the GUI then first of all the standard command sequence is sent to the flash memory through write data condition module. Then data from an flash memory is available on the dout pin of flash memory. This data is read by Read data condition module. This data is then sent to interfaced system or to GUI through UART. Through UART this data is transferred serially to interfaced system.

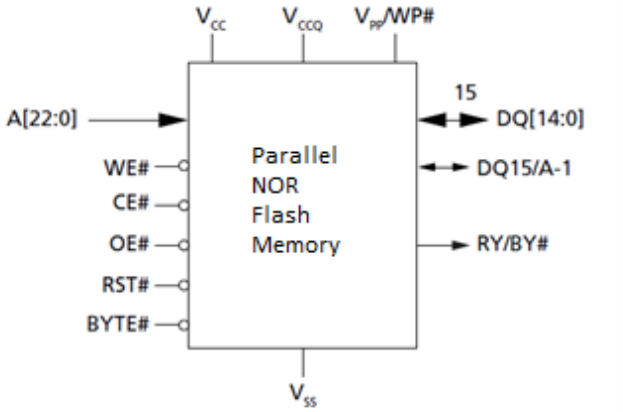

Figure 3: Block diagram of Parallel NOR Flash Memory (M29W128GH)

In reference with figure 3, the figure shows the block diagram of parallel NOR Flash Memory with its input and output signals.All these inputs signals are to be generated by flash memory controller with its timing specification. Memory can be operated in ×8 or × 16 modes. The paper deals with the ×8 bit mode.

III. COMMAND DECODING FORMATS

COMMAND START BIT	COMMAND ENCODINGBIT	COMMAND
AB h	0000 0001	PROGRAM Command
AB h	0000 0010	RESET Command
AB h	0000 0011	READ Command

Table 1: Command chart

In reference with table 1, it shows the actual commands are PROGRAM command, RESET Command, READ command. But for the decoding purpose command encoding bits are added to the command frame format. For valid command transmission command start bits are added to each command. Until and unless the valid command sequence does not receives at the flash controller it remains in idle state. While sending a data from GUI it sends the data in the sequenceas shown in figure 4[1].

COMMAND START BIT	COMMAND ENCODING BIT	PROGRAM ADDRESS (only for PROGRAM command)	PROGRAM DATA (only for PROGRAM command)

Figure 4: Frame format sent through GUI or through interfaced system

Command	A	D	A	D	A	D	A	D
PROGRAM command	AAA	AA	555	55	AAA	A0	PA	PD
RESET command	X	F0	-	-	-	-	-	-
READ command	AAA	AA	555	55	X	F0	-	-

Table 2: Standard Command Definition -Address, Data Cycle

In reference to table 2, these are the standard command definitions address- data cycles which are to be generated by the flash memory controller. For all the design of flash memory controller Parallel NOR Flash Memory (M29W128GH) is considered in x8 bit mode [1].

IV. RESULTS

Figure 5 shows RTL of flash memory controller. Encoding bits, Program address,program data are given as a input to the block. It generates the signals which are required for flash memory. Depending on the encoding bit it came to know which command sequence is to be generated.

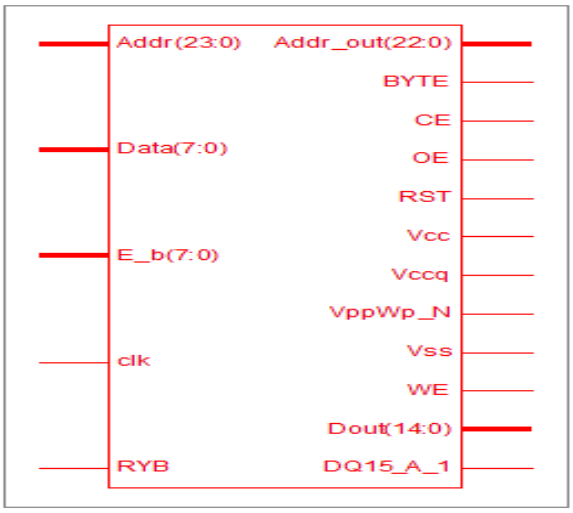

Figure 5: Flash memory controller

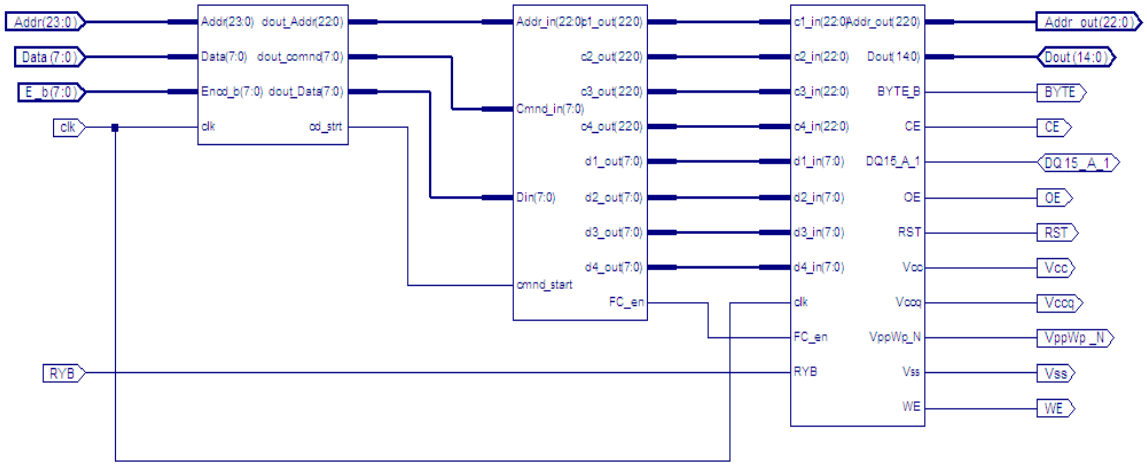

Figure 6: Flash memory controller with FIFO, Command decoder and control unit

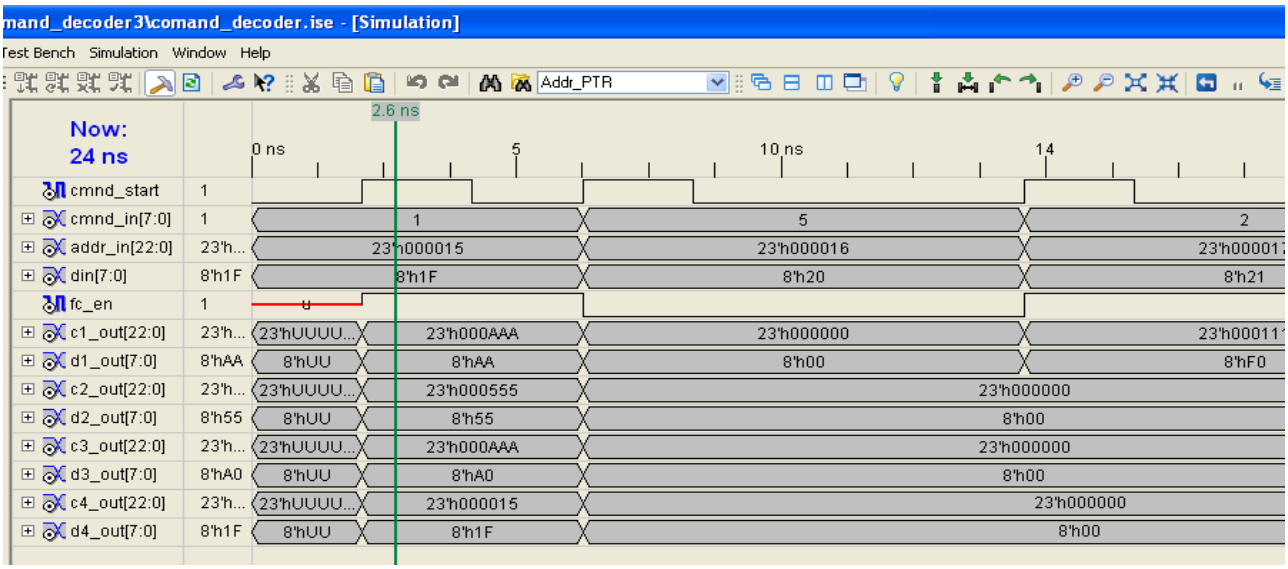

Figure 7: Output at command decoder

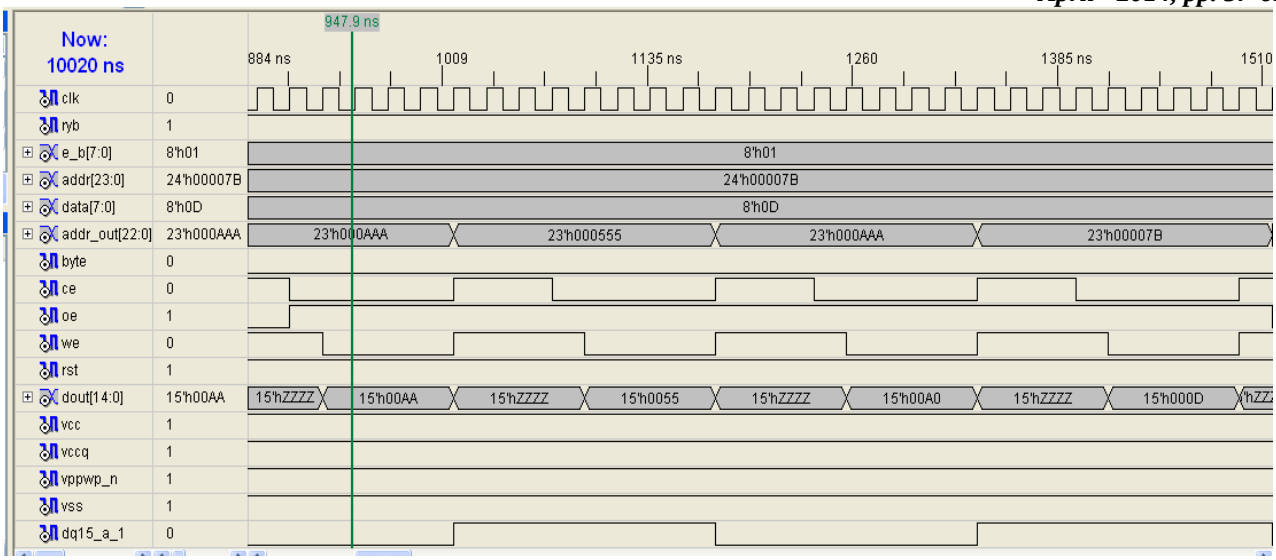

Figure 8: Output of Flash Memory Controller

After theapplication encoding bits, program address bit and program data anyhardware description language can be used to implement it and checked for functionality correctness. In this Paper, the code is implemented in VHDL language and XILINX simulation tool is used to simulate the design and generate the waveforms.

As shown in figure 7, it indicates output of command decoder. When there is rising edge on cmndstart command decoder starts to decode command. Depending on the encoding bits it generates address - data cycles. These values are then given to write data logic and read data logic. As shown in figure 8, it indicates output of flash controller. The block consists of FIFO, command decoder, write data logic, read data logic. Input is given to FIFO block. If valid command is received it will get stored if FIFO.According to operation, respective signals are generated at the output of flash controller.

V. CONCLUSION

According to operation requested by interfaced system the respective command sequence and signals are generated at the output of flash memory controller. If invalid command is received then flash controller doesn't generate any signals. For valid command the data and command related information stored in FIFO. After which is subsequently enables command decoder and flash memory controller to generate signals and address – data cycles. This paper designs different sub modules to design NOR flash memory controller.In this paper, working of Flash memory controller is discussedand implemented flash memory controller for PROGRAM commands, READ command, RESET command.

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