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Review on VHDL Implementation of UART Design with Embedded BIST Technique

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Abstract— The increasing development of Integrated Circuits or sub-micron technology has resulted in the difficulty of testing extremely complex circuits. Design and test engineers have no other choice but to accept new tasks that they have to design systems with full testability, reliability and the functionality to avoid the possibility of product failures, errors and missed target opportunities of market, that had been performed by groups of design and testing engineers in the last years. BIST is the most common design technique that allows self testability to avoid the product failures. A Universal Asynchronous Receiver Transmitter (UART), mostly used for short distance, low speed, low cost data exchange between processor and peripherals. UART allows full duplex serial communication link, also used in control system and data communication. There is a need for realizing the UART function in a single chip. This paper review on VHDL implementation of UART design with embedded BIST technique over FPGA. The paper shows the architecture of UART with status register and BILBO. Complete design is synthesized and verified by Xilinx ISE Simulator and realized over FPGA.

Keywords— Universal Asynchronous Receiver Transmitter; VHDL implementation, Embedded Built In Self Test, Status register, LFSR, BILB, serial communication protocol.

I. INTRODUCTION

Serial data is transmitted via its serial port. A serial port is one of the most universal parts of a computer. It is a connector where serial line is attached and connected to peripheral devices such as mouse, modem, printer and even to another computer. In contrast to parallel communication, these peripheral devices communicate using a serial bit stream protocol (where data is sent one bit at a time). The serial port is usually connected to UART, an integrated circuit which handles the conversion between serial and parallel data [4] [6] [7].

Asynchronous serial Communication has advantages of less transmission lines, long transmission distance and high reliability. UART allows full-duplex communication in serial link, thus has been widely used in the data communications and control system. UART communication needs only two signal lines called Receive and Transmit to complete full-duplex data communication [2] including three modules, the baud rate generator, receiver and transmitter. The baud rate generator produces a local clock signal which is much higher than the baud rate to control the UART receive and transmit; The UART receiver module [8] receives the serial signals at RXD, and convert them into parallel data; The bytes are now converted into serial bits according to the basic frame format by UART transmit module.

In field of electronic design, System on Chip technology requires to realize the complete system function in a single chip. Integration of only core functions over FPGA chip to achieve compact, stable and reliable data transmission avoids waste of resources and decrease cost. Designing processes are extremely complex, inducing designers or testing engineers to consider testability as a requirement to ensure that the reliability and the functionality of their designed circuits [3], [7]. Testing of integrated circuits (ICs) is important to ensure a high level of quality in product functionality in both commercially and privately produced products. In this paper, internal diagnostic capabilities are built into UART by the introduction of Built-In-Self-Test (BIST). A UART with traditional BIST module [1] was designed over Field Programmable Gate Array (FPGA) technology. Much lesser blocks and modules are used to design this UART so that the testing complexity can be reduced.

The paper is prepared into 5 sections.

Section-I gives the Introduction. Need for BIST Technique explains in section II. Section-III describes the UART architecture with BIST. Section-IV shows the Related Work of UART with BIST capability. Finally the paper is concluded by Proposed Work in section V.

II. NEED FOR BIST TECHNIQUE

To identify reliable testing methods which will reduce the cost of test equipment, a research to verify each VLSI testing problems [10] has been conducted. The major problems detected so far are as follows:

A. Test generation problems;

In VLSI circuits the numbers of test patterns are becoming too large to be handled by an external tester has resulted in high computation costs and has outstripped reasonable available time for production and testing.

Another problem is that computer algorithms providing Automatic Test Pattern Generation (ATPG) work well for combinatorial logic but rather poorly for sequential logic circuits. Sequential circuits demand too much computer memory and computation.

B. The input combinatorial problems;

A combinatorial logic circuit with N primary input nodes has a total set of 2^N possible input vectors. The number of test vectors required to exhaustively test a circuit for those functions that a customer might use. In Medium-Scale-Integrated circuits, the number of test vectors needed to exhaustively examine a VLSI circuit such as 32-bits microprocessor is prohibitive. However, a finite number of test vectors can still be applied to an IC and follow the economic rules of production. The finite number of test vectors is much lesser than the full exhaustive test set of a VLSI circuit.

C. The gate to I/O pin ratio problems.

As ICs grow in gate counts, it is no longer true that most gate nodes are directly accessible by one of the pins on the package. This makes testing of internal nodes more difficult as they could neither no longer be easily controlled by signal from an input pin (controllability) nor easily observed at an output pin (observe ability). Pin counts go at a much slower rate than gate counts, which worsens the controllability and observe ability of internal gate nodes.

The VLSI testing problems described above have encouraged designers to identify trustworthy test methods in solving these difficulties. An incorporation of special test circuitry on the VLSI circuit that allows efficient test coverage is the answer to the matter. The need for the incorporation has been addressed by the need for design for testability and hence the need for BIST technology.

BIST is an on-chip test logic that is utilized to test the functional logic of a chip. With the rapid increase in the design complexity, BIST has become a major design consideration in Design-For-Testability (DFT) methods and is becoming increasingly important in today's state of the art SoCs. Achieving high fault coverage while maintaining an acceptable design overhead and keeping the test time within limits is of utmost importance. BIST help to meet the desired goals.

BIST module composition or generic BIST architecture components [1] [7] [10] are;

Circuit under Test (CUT): This is the portion of the circuit tested in BIST mode. It can be sequential, combinational or a memory. It is delimited by their Primary Input (PI) and Primary Output (PO).

Test Pattern Generator (TPG): It generates the test patterns for the CUT. It is a dedicated circuit or a microprocessor. The patterns may be generated in pseudorandom or deterministically. Normally, the pattern generator generates exhaustive input test patterns to the CUT to ensure the high fault coverage. For example, a CUT with 10 inputs will require 1024 test patterns [12].

Test Response Analysis (TRA): It analyses the value sequence on PO and compares it with the expected output.

BIST Controller Unit (BCU): It controls the test execution; it manages the TPG, TRA and reconfigures the CUT and the multiplexer. It is activated by the Normal/Test signal and generates a Go/No-Go. During BIST mode, it selects input from the pattern generator to CUT while during functional mode, selects primary inputs.

There are various approaches being used to generate test patterns for BIST.

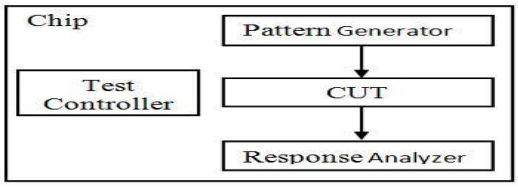

Fig. 1: A generic BIST module

II. UART ARCHITECTURE WITH BIST

Universal asynchronous receive transmit (UART) is an asynchronous serial receiver/transmitter. It is a piece of computer hardware that commonly used in PC serial port to translate data between parallel and serial interfaces. The UART takes bytes of data and transmits the individual bits in a sequential fashion. At the receiving point, UART re-assembles the bits into complete bytes.

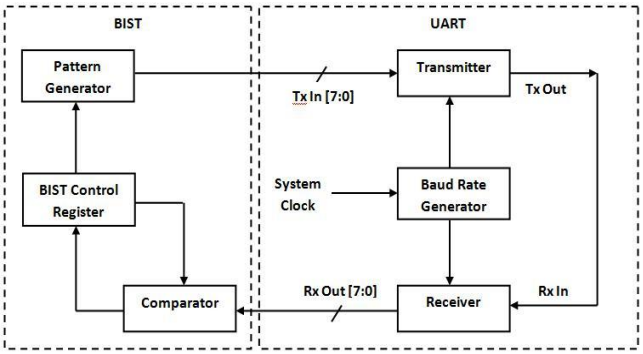

Fig. 2: UART Architecture [3]

The design of UART, shown in Fig. 2, has LCR, Baud Rate Generator (BRG), Transmitter and Receiver as its functional units. All these blocks are explained in brief as course of rest of this section.

Baud Rate Generator

The baud rate generator is programmable by three control bits Bit 0, Bit 1, Bit 2 in LCR as shown in Table 1. 8 different baud rates can be selected by different combinations of Bit 0, Bit 1 and Bit 2. For the selective baud rate the divisor can be obtained by dividing the system clock by desired baud rate

A. UART Transmitter

The transmitter accepts parallel data from peripheral/processor, makes the frame of the data and transmits the data in serial form on the Transmitter Output (TXOUT) terminal (fig. 3). The baud rate generator output will be the clock for UART transmitter.

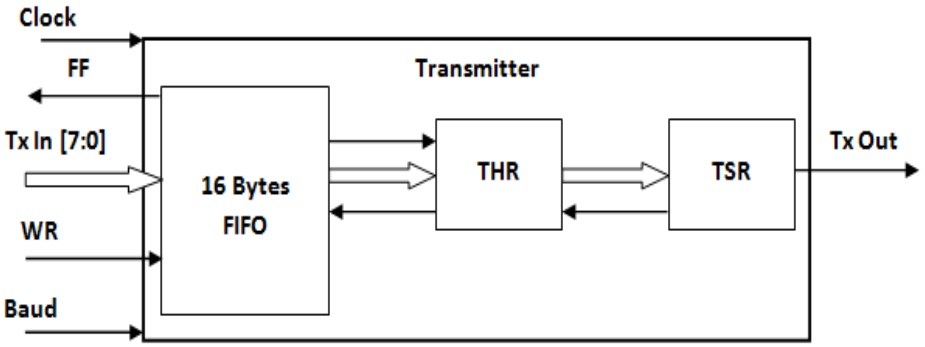

Fig. 3: UART Transmitter

Data is loaded from the inputs TXIN0-TXIN7 into the Transmitter FIFO by applying logic high on the WR input. If words less than 8 bits are used, only the least significant bits are transmitted. FIFO is 16-byte register. When FIFO contains some data, it will send the signal to Transmitter Hold Register (THR), which is an 8-bit register. At a same time, if THR is empty it will send the signal to FIFO, which indicates that THR is ready to receive data from FIFO. If Transmitter Shift Register (TSR) is empty it will send the signal to THR and it indicates that TSR is ready to receive data from THR.TSR is a 12-bit register in which framing process occurs.

B. UART Receiver

The received serial data is available on the RXIN pin. The received data is applied to the sampling logic block. The receiver timing and control is used for synchronization of clock signal between transmitter and receiver. The receiver sampling is 16 times to that of the transmitter baud rate. In the architecture of UART receiver (fig. 4), initially the logic line (RxIn) is high.

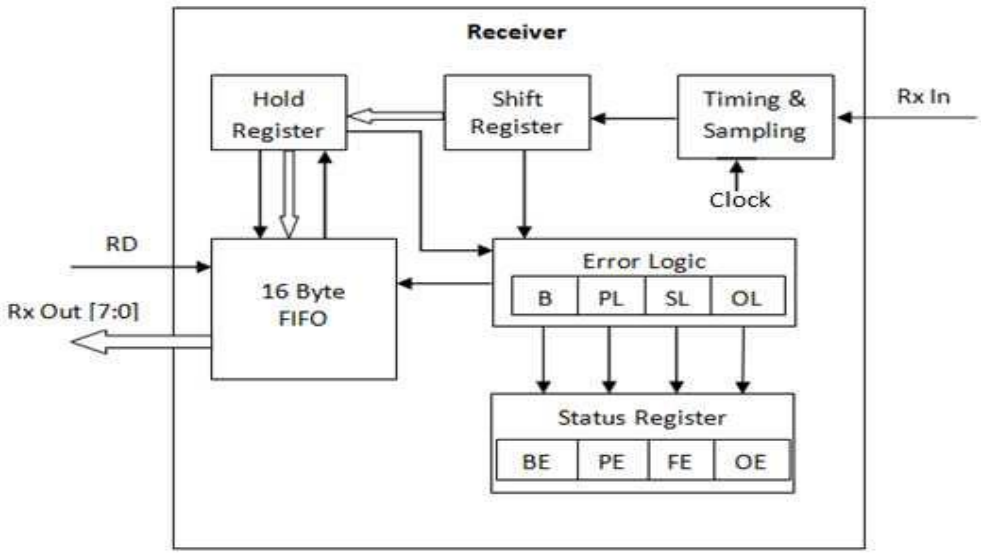

Fig. 4: UART Receiver

Whenever it goes low sampling and logic block will take 4 samples of that bit and if all four are same it indicates the start of a frame. After that remaining bits are sampled in the same way and all the bits are send to Receiver Shift Register (RSR) one by one where the entire frame is stored. RSR is a 12 bit shift register. Now if the Receiver Hold Register (RHR) is empty it sends signal to RSR so that only the data bits from RSR goes to RHR which is an 8 bit register. The

remaining bits in the RSR are used by the error logic block. Then, if receiver FIFO is empty it send the signal to RHR so that the data bits goes to FIFO [14]. When RD signal is asserted the data is available in parallel form on the RXOUT0-RXOUT7 pins.

The status register [5], [9] is implemented with flags for error logic operations performed on the received data. The error logic block handles 4 types of errors: Parity error (PE), Frame error (FE), Overrun error (OE), Break error (BE). If the received parity does not match with the parity generated from data bits, PE bit will be set which indicates that parity error occurred. If receiver fails to detect correct stop bit or when 4 samples do not match frame error occurs and FE bit is set. If the receiver FIFO is full and other data arrives at, RHR overrun error occurs and OE bit is set. If the RXIN pin is held low for long time than the frame time then there is a break in received data and break error occurs and BE bit is set.

IV. RELATED WORK

1. UART WITH BIST-BILBO

BILBO (Built in Logic Block Observer) is a scan register that can be modified to serve as a state register, a pattern generator, a signature register, or a shift register.

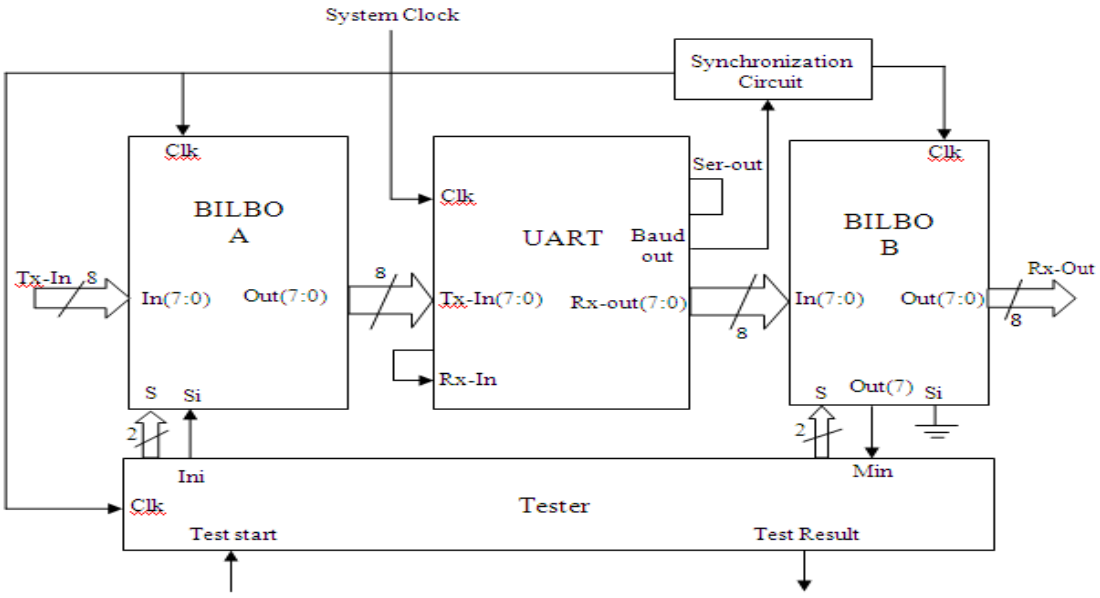

Fig. 5: UART with BILBO Register and Tester

In summary the BILBO operating modes are represented as follows:

TABLE I
BILBO OPERATING MODES [5]

B1B2	Operating Modes
00	Shift Register
01	FSR/PRPG
10	Normal
11	MISR

Figure 5 describes how to apply BILBO registers to test the UART design [1]. In this structure, "Register A" and "Register B" configured by mode control or Bilbo mode signal to act as either a shift register, a test pattern generator (PRPG), normal application mode function or a data compressor called MISR. The test starts with the initialization of the BILBO by applying a "seed" to its serial-in (si) pin. The initialization can be obtained by configuring BILBO's operating mode or "Bilbo mode". "Register A" (LFSR) produces an 8-bits pseudo random pattern data in parallel.

The parallel data is then fed to the UART's transmitter. The UART converts the pseudo random parallel data to serial data which is then looped back to its receiver to create an internal diagnostic capability. The UART's receiver converts the serial data back to parallel and will be accepted by "Register B" (MISR). A signature will be produced after 255 clock iterations (8 data bits produce 28 = 256 PRPG) and this completes the test. The signature is scanned out from serial output (so) pin by configuring Bilbo mode then compared with the correct signature achieved from the simulation of the entire self test sequence approach in a tester. If the signature produced by MISR is similar to the correct signature, it can be concluded that the UART is working properly [5].

2. Standard LFSR

There are various methods and approaches have been used to generate test patterns during BIST [13]. This can be described in brief below:

Linear Feedback Shift Register is used to generate pseudo-random test patterns. This normally requires a sequence of one million or more tests pattern in order to achieve high fault coverage. One of the advantages of LFSR is it uses very little hardware and thus is currently the preferred BIST pattern generation method. In this project, LFSR is being chosen as the test pattern generation method.

A binary counter can generate an exhaustive but not randomized test sequences. Draw back of binary counters as the pattern generator is, it requires more hardware than typical LFSR pattern generator.

Modified counters also have been successfully as test-pattern generators. However, they also require long test sequences.

This method stores a good test pattern set from an ATPG program in a ROM on the chip. However, drawback of this approach is relatively expensive in chip area.

The standard LFSR method [7],[10] has been used in this project as the test pattern generator for the BIST. In this section, the implementation of LFSR will be discussed in detail. A LFSR is a shift register where the input is a linear function of two or more bits (taps). It consists of D flip-flops and linear exclusive-OR (XOR) gates. It is considered an external exclusive-OR LFSR as the feedback network of the XOR gates feeds externally from X_0 to X_{n-1}.

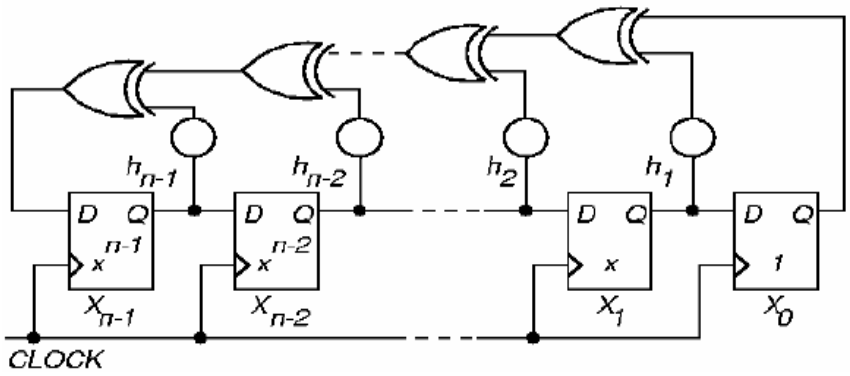

Fig. 6: Standard n-stage LFSR circuit

One of the two main parts of an LFSR is the shift register. A shift register is used to shift its contents into adjacent positions within the register or, in the case of the position on the end, output of the register. The position on the other end is left empty unless some new content is shifted into the register. The contents of a shift register are usually thought of as being binary, that is, ones and zeroes. If a shift register contains the bit pattern 1101, a shift (to the right in this case) would result in the contents being 0110; another shift yields 0011. In an LFSR, the bits contained in selected positions in the shift register are combined in some sort of function and the result is fed back into the register's input bit. By definition, the selected bit values are collected before the register is clocked and the result of the feedback function is inserted into the shift register during the shift, filling the position that is emptied as a result of the shift.

The bit positions selected for use in the feedback function are called "taps". The list of the taps is known as the "tap sequence". By convention, the output bit of an LFSR that is n bits long is the nth bit; the input bit of an LFSR is bit 1. The state of an LFSR that is n bits long can be any one of 2 different values. The largest state space possible for such an LFSR will be 2^n-1, all possible values except the zero state. All zero is not allow in LFSR, as it will always produce 0 in spite of how many clock iteration. Because each state can have only once succeeding state, an LFSR with a maximal length tap sequence will pass through every non-zero state once and only once before repeating a state.

3. Implementation of a BIST Embedded High Speed RS- 422 Utilized UART over FPGA

Testing of a circuit has become increasingly tough as the scale of integration grows. UART with the BIST capability provides the specified testability requisites and lowest-price with the highest performance implementation.

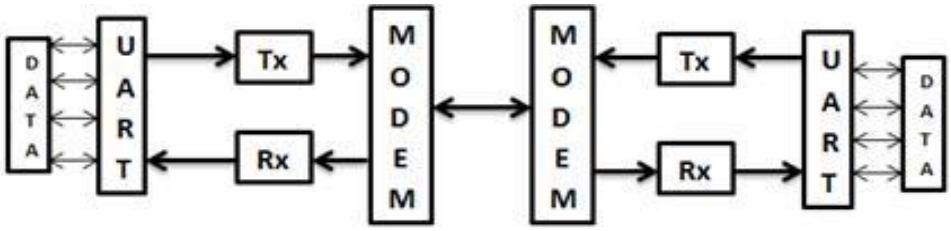

Fig. 7: Serial data transmission and reception in UART.

Several works have been done using VHDL in designing UART. Most of them focused on designing basic UART module [2], [10]. Some focused only on speed or on Communication standards [15] [16].

Though there are some works on BIST technique in recent years, A UART with traditional BIST module was designed [3] but also high speed and communication protocol utilization within it using Field Programmable Gate Array (FPGA) technology. Much lesser blocks and modules are used to design this UART so that the testing complexity can be reduced. Designed UART shows baud rate of 4 Mbps. The Bit error rate is only .000007

FPGAs can be used to implement any logical function that can be performed by an ASIC, and it should also be noted that FPGA design is more cost-effective than that of ASIC. They have lots of advantages over microcontrollers, such as greater speed, number of I/O ports and performance.

Fig.8 shows the testing of the total system. The RS-422 communication [2] terminal of a PC is connected with FPGA with the aid of daughter board DGB002. Here, first the data bits are sent to the DBG002 and then it feds the signal in RS-422 connector. Here, RTS means request to send and CTS means clear to send. The baud rate is 4 Mbps and RS-422 communication cables using twisted pair shielded is 3m long. The result shows the bit error rate is about 0.000007.

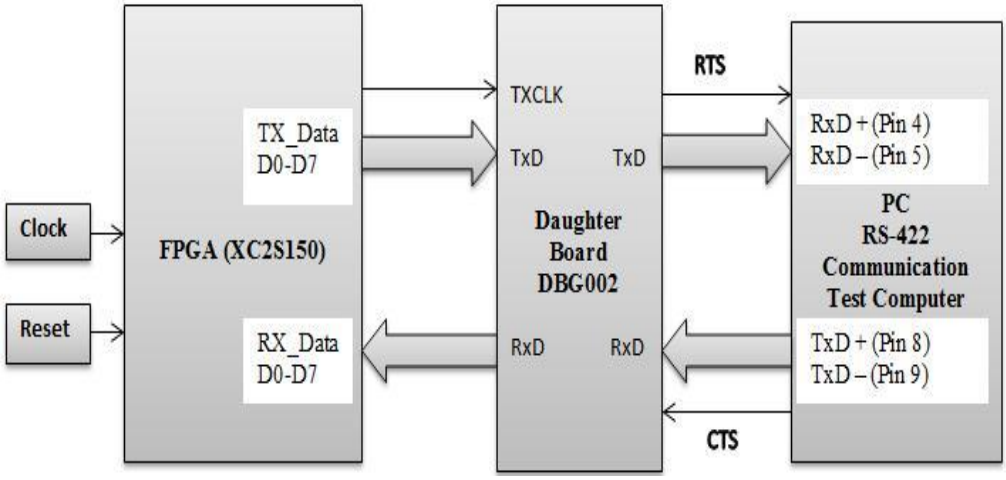

Fig. 8: RS-422 Utilization

V. PROPOSED WORK

The proposed work will be the architecture of UART with BIST technique. This will allow testing the circuit itself. Working of UART will have been tested using Xilinx ISE simulator, implemented on FPGA. The results would be more enhanced in terms of Area, Speed and Power.

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