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Implementation of OFDM based Transreciever for IEEE 802.11a on FPGA

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Abstract— This paper focus on the implementation of Transreciever for the IEEE 802.11a WLAN standard which incorporates OFDM as its multiplexing and modulation technique .An OFDM is a multicarrier modulation technique which divides the available spectrum into many subcarriers. Due to orthogonality of carriers and sharing of data, OFDM has high bandwidth efficiency. OFDM can be viewed as many slowly modulating narrow signals instead of a single rapidly modulating wideband signal .as our main focus is to implement this design on FPGA kit main constraint that has to be under taken is area efficiency and low power dissipation. In digital domain IFFT/FFT block are responsible for providing orthogonality to carrier and most hardware consuming we will be therefore more concern about reducing the effective area consumed by this block .Hardware description Language used will be Verilog for generating gate level net list of the design. The proposed design will be operated at 20 MHZ.

Keywords— OFDM, FPGA, FFT/IFFT, ASIC, HDL.

I. INTRODUCTION

With the rapid advancement of digital communication in recent years, there is a increase in the need of high speed data communication. The mobile telecommunications service providers face the problem for provide the technology which can support various services ranging for voice communication with bit rate of a few kbps to 2 Mbps. One of the important applications of high speed wireless communication is WLAN which is covered under IEEE 802.11a standard. This standard provide a high data rate up to 54 mbps although data rate can be varied from 6 mbps to 54 mbps depending on type of modulation technique(constellation mapper) is employed at transmitter side. Multiplexing technique employed for achieving the high data rate is OFDM which stands for Orthogonal Frequency Division Multiplexing. as the name suggest OFDM is analogous to FDMA where each carrier signal is dedicated their own signal band and all band are multiplexed together and transmitted along the single channel, Similarly in OFDM many slowly modulating narrow signals instead of a single rapidly modulating wideband signal this provide higher bandwidth efficiency and also the fact that each message signal is orthogonal to each other leads to the low ISI between the channel.

OFDM scheme has become the essence of most 4G communication systems like fixed Wi-Fi system, mobile Wi-Fi system fixed WiMAX system mobile WiMAX system and Long Term Evolution (LTE system) so it is mandatory to built OFDM system on a suitable hard ware. Main aim of our project is to implement OFDM technique for IEEE 802.11a in such a way that any up -gradation or enhancement is possible in future .FPGA is a obvious choice for our project as it provide us with the option of reconfigrability and efficient resource utilization .Key advantage of FPGAs over traditional Digital Signal Processor (DSP) processors is its flexibility. Many recent high speed digital signal processing applications such as video and image processor and various communications and networking devices are implemented by using FPGA.

The rest of this paper is organized as follows. Section II describes the OFDM theory and its Fundamental. System Design is described in section III. Hardware Description Language and Synthesis process are discussed in section IV. Result of verilog emulation is discussed in section V. Section VI concludes paper.

II. OFDM OVERVIEW

OFDM is used for encoding digital data on the multiple carrier frequency .Multiple carrier frequency termed here is obtained by selecting suitable point from the constellation diagram. It is important to know a fundamental understanding of OFDM (Orthogonal Frequency Division Multiplexing) because this technology is used to build a basic building blocks for many of the currently used modulation schemes that includes; 802.11 WLAN, 802.16 WiMAX, and 3GPP LTE standards. OFDM is a digital multicarrier modulation scheme which is achieved by extending the concept of single subcarrier modulation to multiple subcarrier modulation. Instead of transmitting a single subcarrier for higher bit rate stream of data, In OFDM scheme we use large number of closely time spaced orthogonal subcarriers that are multiplexed together and transmitted in parallel. All subcarriers are modulated with a conventional digital modulation scheme i.e QPSK 16QAM, 64 QAM etc. at low symbol rate.

Talking in terms of frequency domain essence of OFDM concept lies in the fact that each subcarrier has different frequency. Subcarrier frequency is chosen in such a way that each signal becomes orthogonal to each other.

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Orthogonality provide independence to each signalling frequency so that these frequency are uncorrelated to each other mathematically it means that if two signal are orthogonal to each other the product of their area gives zero.

$$\int_a^b \emptyset n(t)\emptyset' m(t)d(t) = 0; n \neq m \qquad \text{Eqn-1}$$

This orthogonality should be maintained throughout the communication for proper reception at receiver side. Due to use of orthogonal subcarriers, system allows more subcarriers per bandwidth which increase in spectral efficiency. In a conventional OFDM signal, Orthogonality prevents interference between distinct but overlapping carriers.

Using combination of Building block of Digital Signal Processing like IFFT (Inverse Fast Fourier Transform) and FFT (Fast Fourier Transform) we can extend the concept of analog OFDM to the digital domain. Due to used for mapping digitally modulated input data onto orthogonal subcarriers, these transforms are important from the OFDM implementation. In principle, the IFFT block converts frequency-domain input data in its bin into the time-domain output data.

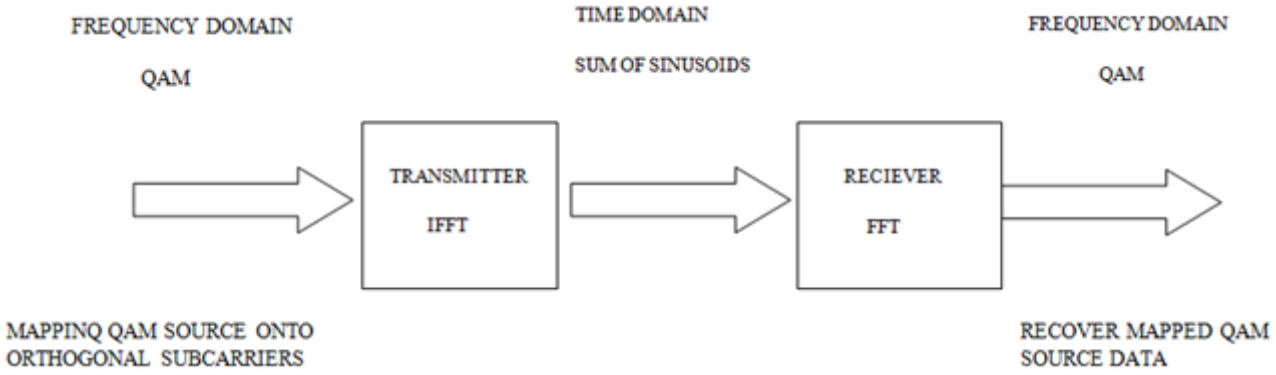

Figure 1 Simplified OFDM System

If N sub-carriers are used for transmission, and each sub-carrier is modulated using M distinct symbols, the OFDM symbol alphabet consists of M^N combined symbols.

A low pass OFDM signal is expressed as

$$v(t) = \sum_{k=0}^{N-1} X(k) e^{\frac{j2\pi kt}{T}} \; 0 < t < T \qquad \text{Eqn-2}$$

Where X(k) is data symbol ,N is number of sub carrier , T is OFDM symbol time ,sub carrier spacing of 1/T make them orthogonal over each symbol period.

$$V(t) = \frac{1}{T}\int_0^T e^{\frac{j2\pi(k2-k1)t}{T}} d(t) \qquad \text{Eqn-3}$$

III. SYSTEM DESIGN

Our main focus in this paper is to design a Transreciever for IEEE 802.11a that works on OFDM scheme to provide successful wireless communication at higher data rate. Desired system design will revolve around following specification at physical layer

TABLE -1 IEEE 802.11A SPECIFICATION AT PHYSICAL LAYER

Bandwidth	20MHz
Operational Bandwidth	16.MHz
Subcarrier spacing	312.5KHz(20/64 point FFT)
Information Rate	6-54Mbps
Modulation	BPSK,QPSK,16-QAM,64-QAM
Coding Rate	½
Total subcarrier	52(-26 to +26)
Total data carrier	48

For further discussion we will divide our system into a. Transmitter Section b. Receiver Section.

a) Transmitter Section

To transmit an OFDM signal first there is a need of creating OFDM signal from input bits. OFDM signal creation process starts with scrambling of input bits .scrambling is done to eliminate the dependency of a signal power upon the actual transmitted data. Scrambler is also referred to as Randomizer. Randomized bits are then feed into the encoder block that performs channel coding of the data bits. Encoder block comprises of RS Encoder and Convolution coding. Encoded bits are the fed to Interleaver block that Interleave the bits such that two adjacent bits are no more adjacent to each other. Data stream is divided into group of n-bits

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where n is decided by type of modulation scheme(QPSK,16-QAM,64-QAM) is used .modulated data symbol are passed to Serial To Parallel converter this parallel data are the fed as input to IFFT bin, 52 parallel data bits are loaded at a time to IFFT bin. IFFT block provide desired orthogonality and convert frequency domain data into time domain sinusoid signals. Orthogonality is maintained by the addition of cyclic prefix to the IFFT output data are the converted into serial stream and RF modulated to propagate through communication channel in our case of IEEE 802.11a channel is wireless.

b) Receiver Section

Reception of the OFDM signal is an opposite process of transmission. On reception of OFDM signal first operation perform is removal of Cyclic Prefix from the signal. Serial stream of input is then passed through serial to parallel converter and then fed to FFT bin. On successful FFT operation orthogonality is removed time domain signal is converted into frequency domain signal.FFT output converted into serial stream and fed into Constellation Demapper or Demodulator. Output of this block is binary bit stream, this bit stream is then passed through De-Interleaver, Decoder and De-scrambler to obtain originally transmitted bit stream.

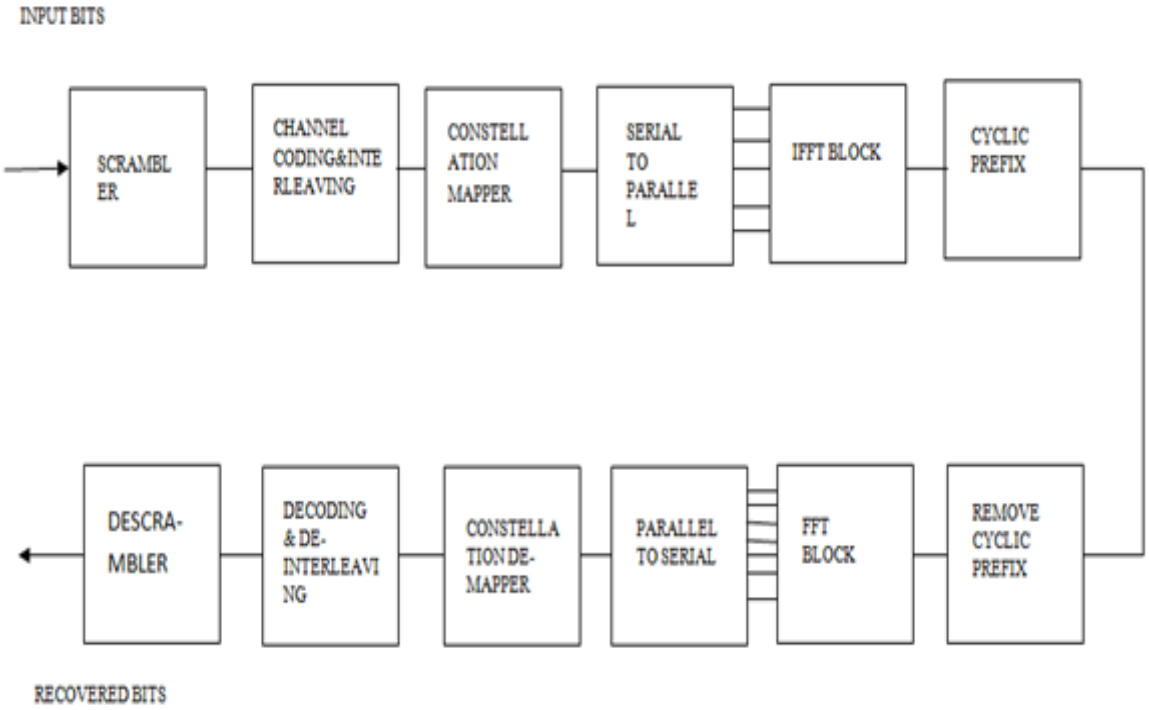

Figure 2 Transceiver for 802.11a

When the IFFT block is completely loaded with complex parallel input from the constellation mapper , the Inverse FFT of all frequency domain input is computed. After computation, it gives a set of complex time-domain samples which represent the combined OFDM subcarrier. The samples are clocked out at speed of 20 Mbps to create an OFDM frame of 3.2 us (20Mbps/64) . To complete the OFDM symbol, a guard interval (GI) of 0.8usis added. It produces one OFDM symbol with time duration of 4 us in length. The process is repeated in order to create OFDM symbols of the remaining input data bits. The combination of OFDM symbol is sent along in burst mode.

IV. HDL&SYNTHESIS PROCESS

Verilog HDL is preferred HDL used in the project, main reason being its similarity with c language and thus easily understandable. Design described in HDL are easy to debug and more readable than schematics for large circuit.

Verilog can be used to describe design at four level of abstraction

I. Behavioural level.
II. Register transfer level.
III. Gate level.
IV. Switch level.

Synthesis process means to construct a gate level net list from a model of a circuit described in Verilog or any other HDL language. The synthesis process is described in fig 3. A synthesis program generates an RTL net list which consist of RTL level blocks such as flip flop, arithmetic-logic-unit& multiplexer. All this are performed using RTL module builder. This builder is incorporated to build or acquire from a library predefined components, each of the required RTL blocks in the user specified target technology.

The above synthesis process may produce an unoptimized gate level net list. A logic optimizer can be used to produce net list and constraint specified to produce optimized gate level net list

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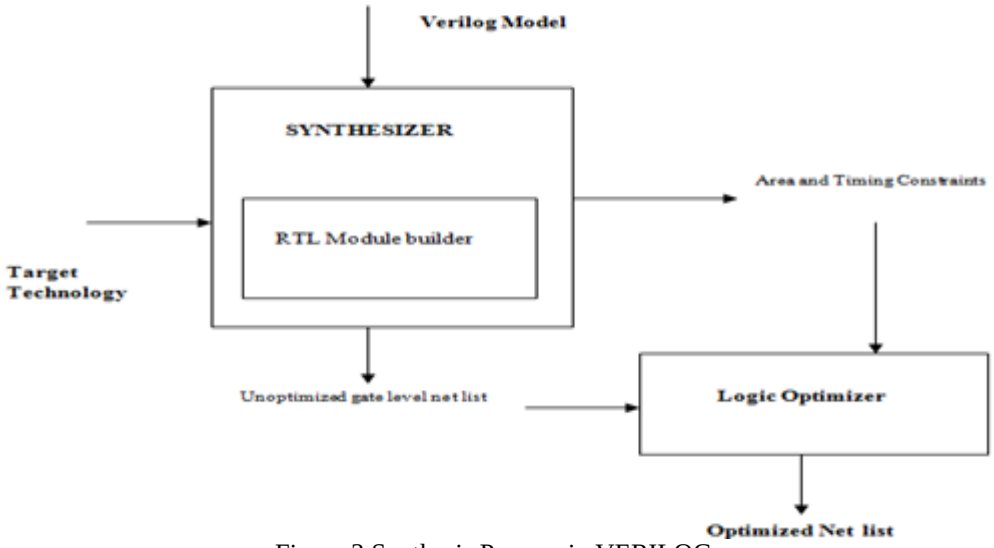
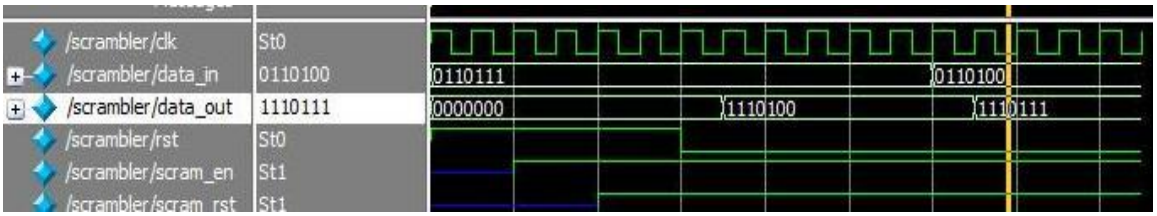


Figure 3 Synthesis Process in VERILOG

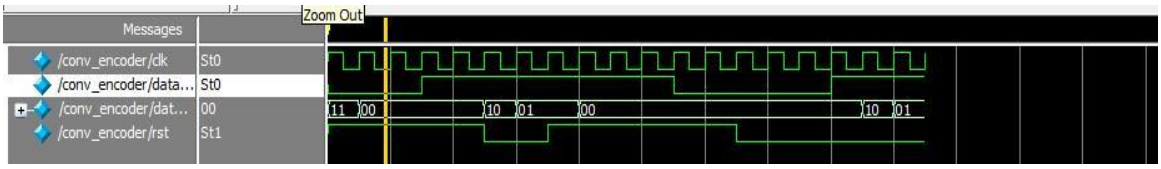
V. RESULTS & DISCUSSION

In this section we will cover simulation result of major functional block of our proposed design. For simplicity and easy understanding we will be showing simulation result for certain set of input from large test input set that we have have tested successfully

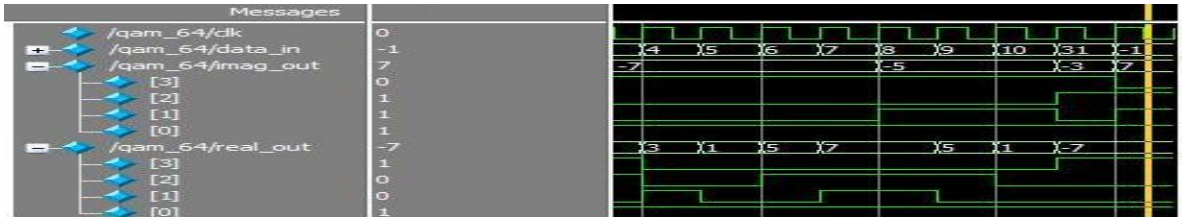
Simulation resultof 8-bitscrambler



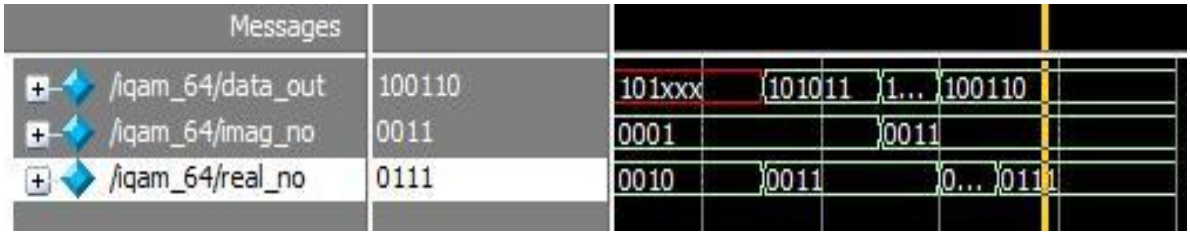
Simulation result of convolution encoder rate-coding rate(1/2)



Simulation result of 64-qam



Simulation result for 64-iqam



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VI. CONCLUSION

The main aim of this project is to implement the core signal processing blocks of IEEE 802.11a Transreciever system on FPGA using Verilog HDL to generate an optimized gate level net list which is fed to the FPGA. Xilinx tool is used to synthesis the net list and to generate the synthesis report of our design. Modelsim is used to simulate the behavior of the design at various levels it helps to generate simulation result for various data entry at various blocks in the design. Channel coding helps in providing error correction and detection for the input signal. Our main concern throughout design implementation will be minimizing hardware requirement for each module. Of all the block IFFT/FFT block is most hardware consuming and power hungry due to large number of complex multiplication involved .designed system can be used to achieve data rate ranging from 6-54 Mbps by varying type of modulation technique used.

REFERENCES

[1] JOAQUIN GARCIA, RENE CUMPLIDO "*ON THE DESIGN OF AN FPGA-BASED OFDM MODULATOR FOR IEEE 80211A.* " 2ND INTERNATIONAL CONFERENCE ON ELECTRICAL AND ELECTRONICS ENGINEERING (ICEEE) AND XI CONFERENCE ON ELECTRICAL ENGINEERING (CIE 2005)

[2] Magis Networks, Inc. "*Orthogonal Frequency Division Multiplexing (OFDM) Explained"* February 8, 2001.

[3] Manjunath Lakkannavar, Ashwini Desai "*Design and Implementation of OFDM (Orthogonal Frequency Division Multiplexing) using VHDL and FPGA"*. ISSN: 2249 – 8958, Volume-1, Issue-6, August 2012

[4] International Engineering Consortium "*An Introduction to OFDM*",

[5] Loo Kah Cheng "*Design of an OFDM Transmitter and Receiver using FPGA"* UTM, 2004.

[6] Ahmed Saeed, M. Elbably, G. Abdelfadeel, and M. I. Eladawy "*Efficient FPGA implementation of FFT/IFFT"*.

[7] Koushik Maharatna, Eckhard Grass, and Ulrich Jagdhold "*A 64-Point Fourier Transform Chip for High-Speed Wireless LAN Application Using OFDM"* IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 39, NO. 3, MARCH 2004

[8] (2002) The IEEE website. [Online]. Available: http://www.ieee.org/.

[9] http://wireless.agilent.com/wireless/helpfiles/89600B/WebHelp/Subsystems/wlan-ofdm/Content/ofdm_80211-overview.htm/

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