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Compression and Decompression of Signal Using CMOS Technology...A Review

Miss NEHA B. Kale
M.E. 2nd year
Dept. of Electronics and Telecommunication
PRPCET, Amravati, India

Mr. VISHAL B. Padole
Assistant Professor
Dept. of Electronics and Telecommunication
PRPCET, Amravati, India

Abstract— The advent of new technologies & advancement in medical science we are trying to process the information artificially as our biological system performs inside our body. Furthermore nature has evolved techniques to deal with imprecise analog computations by using redundancy & massive connectivity. Artificial intelligence is realized based on many things like mathematical equations & artificial neurons. We are making use of Artificial Neural Network (ANN) to demonstrate the way in which the biological system processes in analog domain. The analog component like Gilbert cell multiplier, Adder, Neuron activation function are used in the implementation. The functionality of design neural network is verified for analog operation like signal amplification &frequency multiplication. Using 32 nm CMOS technology will be for layout designing & verification of proposed neural network. The improvement for neural network for compression & decompression in signal processing will be done with CMOS 32 nm technology.

Keywords- Neural Network Architecture (NNA), Artificial Neural Network (ANN), Analog Signals.

I. INTRODUCTION

Intelligence is the ability to achieve the hold the word. Intelligence is a biological word is acquired from past experience. Artificial intelligence is implemented by using neuron and this artificial neuron artificial neuron comprised of several analog component. An ANN is configured for a specific application, pattern recognition function approximation; learning in biological system involves adjustment to the synaptic connection that exists between the neuron. The most promising approach for implementing neural network is to fabricate special purpose very large scale integration chips.

Today's integration density a large number of simple processor can be packed on a single chip together with necessary interconnection to make a collective computing neural network. The neuron selected a analog component like multiplier and adder along with the tan-sigmoid function. The working of neuron is add together and calculating an output to be passed on. The neural architecture is trained using back propagation algorithm and also it may be a feed forward network. 32 nm CMOS technology will be used for layout design of neural network will be verified for analog operation lie signal amplification and frequency multiplication. Due to the rapid advance in integration technology, large- scale system design-in short and due to the advent of VLSI technology the electronics industry has achieved a phenomenal growth over the last two decade. So the neural network is implemented in VLSI using analog component like Gilbert cell multiplier, adder and differential amplifier are used for different blocks.

.II. LITERATURE

From the rigorous review of related work and published literature, it is observed that many researchers have designed Neural Network by applying different techniques like analog simulation. Researchers have undertaken different systems, processes or phenomena with regard to design and analyze Neural Network and have designed Neural Network by applying different techniques like analog simulation. Researchers have undertaken different systems, processes or phenomena with regard to design and analyze Neural Network and attempted to find the unknown parameters. Since in the real world today VLSI is in very much in demand, from the careful study of reported work it is observed that very few researchers have taken a work for designing Neural Network for compression & decompression in signal processing using 32 nm CMOS technology. A survey of Neural Network is presented by Kumar et al. in his paper he discussed the analog component used are comprises of multiplier & adder along with tan sigmoid function circuit using MOS transistor in sub threshold region. The layout design & verification of the proposed design is carried out using Tanner EDA 14.1 tool & Synopsys Tspice. The technology used in designing is MOSIS/HP 0.5 u SCN 3M Tight Metal. In this technology required the low speed, high speed and many other problems was occurred.

Yammenavar et al. this paper makes use of Artificial Neural Network to demonstrate the way in which the biological system processes in analog domain.Using180nm CMOS VLSI technology for implementing analog and digital circuits which performs arithmetic operations and for implementing Neural Network. In this technology required large input

voltage range & large area required for chip designing. In 180 nm technology was occurred may problem for signal amplification for speed, power and circuit design area.

Kshirsagar et al. in this paper used 45 nm CMOS technology for signal processing in neural network. In this 45 nm technology the area required for designing of analog component was large, more voltage was required, large power consumption. It is quite expensive and the uniformity of the device structure may be affected due to process variation. In the following technology there was many problem occurred in signal amplification for compression and decompression. So to rectify the problem we are implementing this neural network by using different block like multiplier, adder and neuron activation function by using 32 nm CMOS technology with the required parameters.

III. CMOS TECHNOLOGY

The evolution of important parameter in CMOS technology .in the integrated circuit complexity, gate length, switching performance and required supply voltage with prospective vision down to the 11 nm technology. The trend of CMOS technology improvement continues to drive by the need to integrate more function within a given silicon area.

A] Reduce the fabrication cost.
B] Increase operating Speed.
C] Dissipate less power.

32nm CMOS Technology.

32 nm technologies have been introduced by various manufactures addressing different type of application. The First production of 32 nm CMOS technology in 2009 with the effective gate length.32 nm technology is addressing low power application such as mobile communication device. 32 nm CMOS technology related to the high-k gate oxide and very low-K interconnect dielectric material. 45 nm technology VS 32 nm technologies offer,

I] 30% increases in switching performance
II] 30% less power consumption
III] 2 times higher density
IV] Leakage between source and drain through the gate oxide are two times reduces.

In the proposed work will be used the 32 nm technology for implementation of neural network for signal compression and decompression. The effective gate length required for 32 nm is 16 nm.

[A] Neural Network

The simplest definition of a neural network is 'A made up of a number of simple interconnected processing nodes, which process information response to external input'.

Neural Network layers are made up of number of interconnected nodes, & these nodes contain an 'activation function'. In the network each node are internally connected and present some layers and all this layers in the neural network are hidden layers & this hidden layers are connected to the output of the neural network.

[B] Signal Compression

In analog signal when the signal become compressed than reduction of dynamic range of signal. In the neural network when the analog signal become compress than the frequency become decreases & amplitude become reduces. Signal compression is used in the analog as well as digital signal system for improving signal to noise ratio in the system.

[C] Signal Decompression

In analog system decompression is exact reveres process of compression. The decompression output signal which is processed by a compressor, after the decompression signal that exactly match or approximate to the compression signal. In the proposed work we will be design of neural network for signal compression and decompression by using 32 nm CMOS technology. First we will be design the analog component like Gilbert cell multiplier, adder and neuron active function. So the design of neural network for compression and decompression of analog signal in 32 nm CMOS technology required less power, high switching performance and as compared to other technology width and length of transistor become reduces.

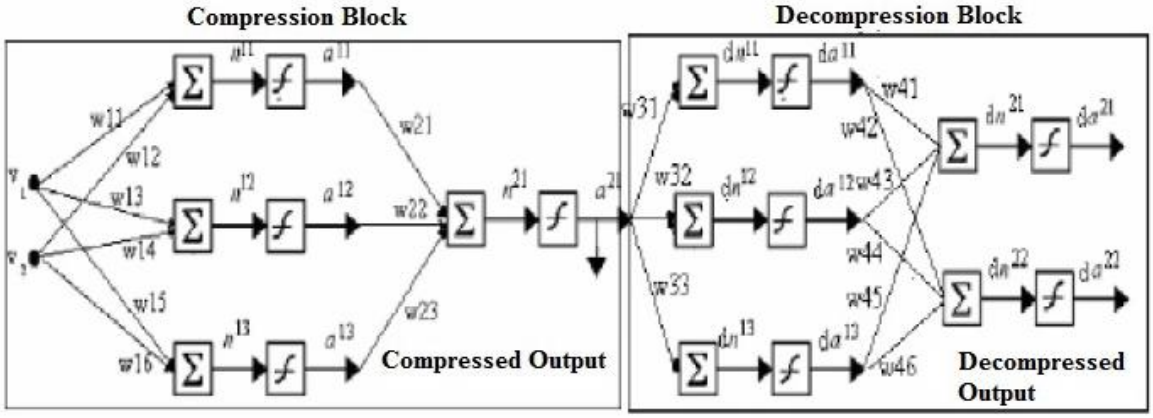

Fig1. Image Compression and Decompression using proposed neural architecture.

IV. CONCLUSION

Simulation results can be obtained VLSI technology is the fastest growing field today. Considering the advancement of future technology and the advantage of 32 nm technology over 45 technology, the selection of 32m technology for the proposed project will be the proper choice of technology. The VLSI implementation of a feed forward neural network for analog signal processing has been demonstrated in this project. To give an application oriented approach two analog signals are compressed and decompressed using the designed feed forward neural network and the in 32nm CMOS VLSI technology.

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