Volume 4, Issue 1, January 2014 ISSN: 2277 128X

International Journal of Advanced Research in Computer Science and Software Engineering

Research Paper

Available online at: www.ijarcsse.com

An Optimized Realization of ALU for 12-Operations by using a Control Unit of reversible gates

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***Abstract*— Reversible logic is one of the most important issues at present time and it has different areas for its application. The main purposes of designing reversible logic are to decrease quantum cost, depth of the circuits and the number of garbage outputs. A control unit is proposed in this paper which consists of reversible gates.This control unit is more efficient with respect to the existing control unit . This paper also represents an optimized realization of arithmetic logic unit by using the proposed control unit and DKFG reversible gate .**

***Keywords*: Reversible logic, Basic Reversible Gates, Full adder, Arithmetic operation Logic operation, control unit, Garbage, Quantum cost.**

I. INTRODUCTION

Energy dissipation is one of the most important factors in electrical circuit designing. Reversible logic was first related to energy when Landauer states that information loss due to function irreversibility leads to energy dissipation in 1961 who stated that there is small amount of heat dissipation the circuit due to loss of one bit of information and it would be equal to kTln2 where 'k' is Boltzman constant and T is the temperature [1]. This principle is further supported by Bennett that zero energy dissipation can be achieved only when the circuit contains reversible gates in 1973.It was proved by Bennett that the energy kTln2 would not be dissipate from the circuit if input can be extracted from output and it would be possible if and only if reversible gates are used[2]. According to Moore's law the numbers of transistors will double every 18 months. Thus energy conservative devices are the need of the day. The amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Reversible circuits are those circuits that do not lose information A circuit will be reversible if input vector can be specifically retrieved from output vectors and here is one to one correspondence between input and output [3]. Younis and Knight [4] showed that some reversible circuits can be made asymptotically energy-lossless if their delay is allowed to be arbitrarily large. A reversible logic circuit should have the following features [6]:

• Use minimum number of reversible gates.
• Use minimum number of garbage outputs.
• Use minimum constant inputs.

II. BASIC REVERSIBLE LOGIC GATES

A. *Reversible logic Function*

It is an n-input n-output logic function in which there is a one-to-one correspondence between the inputs and the outputs. Because of this bijective mapping the input vector can be uniquely determined from the output vector. This prevents the loss of information which is the root cause of power dissipation in irreversible logic circuits. The reversible logic circuits must be constructed under two main constraints. They are

- Fan-out is not permitted.
- Loops or feedbacks are not permitted

The quantum cost(QC) of any reversible gate(circuit) is the number of 1×1 or 2×2 reversible gates and quantum logic gates such as V, V+ (V is also named square root of NOT gate *NOT* and V+ is hermitian of V). The V and V+ quantum gates have some properties that are shown in Equation (1) (Mohammadi et al., 2009).

$$\left.\begin{aligned} V \times V &= NOT \\ V \times V^{+} = V^{+} \times V &= I \\ V^{+} \times V^{+} &= NOT \end{aligned}\right\} \text{Equation (1)}$$

Any reversible logic gate (circuit) is realized by using mentioned gates above, NOT and FG gates. The properties above show that when two V gates are in series they will behave as a NOT gate. Similarly, two *V* + gates in series also function as a NOT gate. A V gate in series with *V* + gate, and vice versa, is an identity

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B. Reversible logic Function

The important basic reversible logic gates are, Feynman gate [7] which is the only 2*2 reversible gate which is as shown in the figure.1a and it is used most popularly by the designers for fan-out purposes. There is also a double Feynman gate [8], Fredkin gate [9] and Toffoli gate [10],New Gate[11] , Peres gate[12] , all of which can be used to realize important combinational functions and all are 3*3 reversible gates and are as shown in the figure.1b to figure.1e .The figures also shows the switching functions for terminals

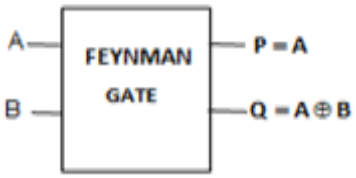

Fig.1a Feynman gate – 2*2 gate

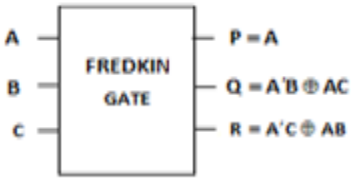

Fig.1b Fredkin gate – 3*3 gate

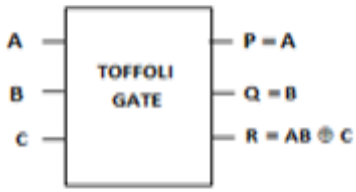

Fig.1c Toffoli gate – 3 * 3 gate

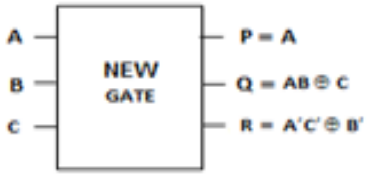

Fig.1d New gate – 3 * 3 gate

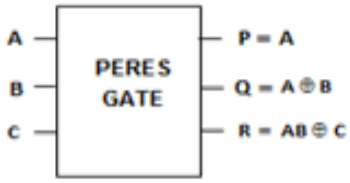

Fig.1e. Peres gate – 3 * 3 gate

III. A 4X4 DKFG REVERSIBLE GATE

A 4 * 4 reversible gate DKFG already had been proposed [13] shown in figure 2. In this gate the input vector is given by I_V = (0, A, B, C) and the corresponding output vector is O_V= (P, Q, R, S).

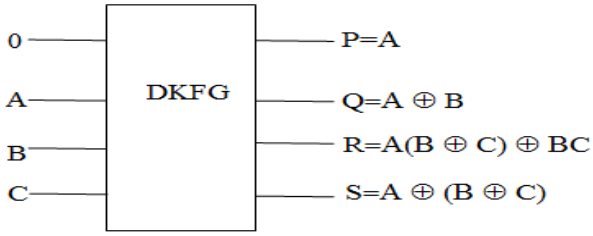

Figure 2: DKFG Gate

We can implement half-adder by using DKFG gate as shown in fig 2a.We can use DKFG gate as a full-adder as shown in fig2b

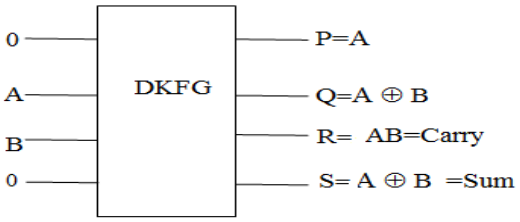

Figure2a. Implementation of DKFG gate as a half-adder

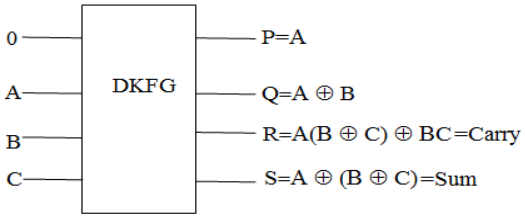

Figure 2b. Implementation of DKFG gate as a full-adder

IV. DESIGN OF ARITHMETIC CIRCUIT

ALU is a data processing component, which is an important part in centre process unit (CPU). Different kinds of computers have different ALUs. But all of the ALUs contain arithmetic unit and logic unit, which are the basic structures. The basic component of the arithmetic section of an ALU is a parallel adder. A parallel adder is constructed with a number of full adder circuits connected in cascade. By controlling the data inputs to the parallel adder, it is possible to obtain different types of arithmetic operations. Figure 3 shows the arithmetic operations obtained when one set of inputs to a parallel adder is controlled externally.

The number of bits in the parallel adder may be of any value. The input carry C_{in} goes to the full adder circuit in the least significant bit position and the C_{out} comes from the full adder circuit in the most significant bit position. From the figure 4(a) to 4(h) we can see various type of eight operations can be achieved by controlling the B input and C_{in}. So to design the circuit we need two parts, one is control circuit and the another one is full adder.

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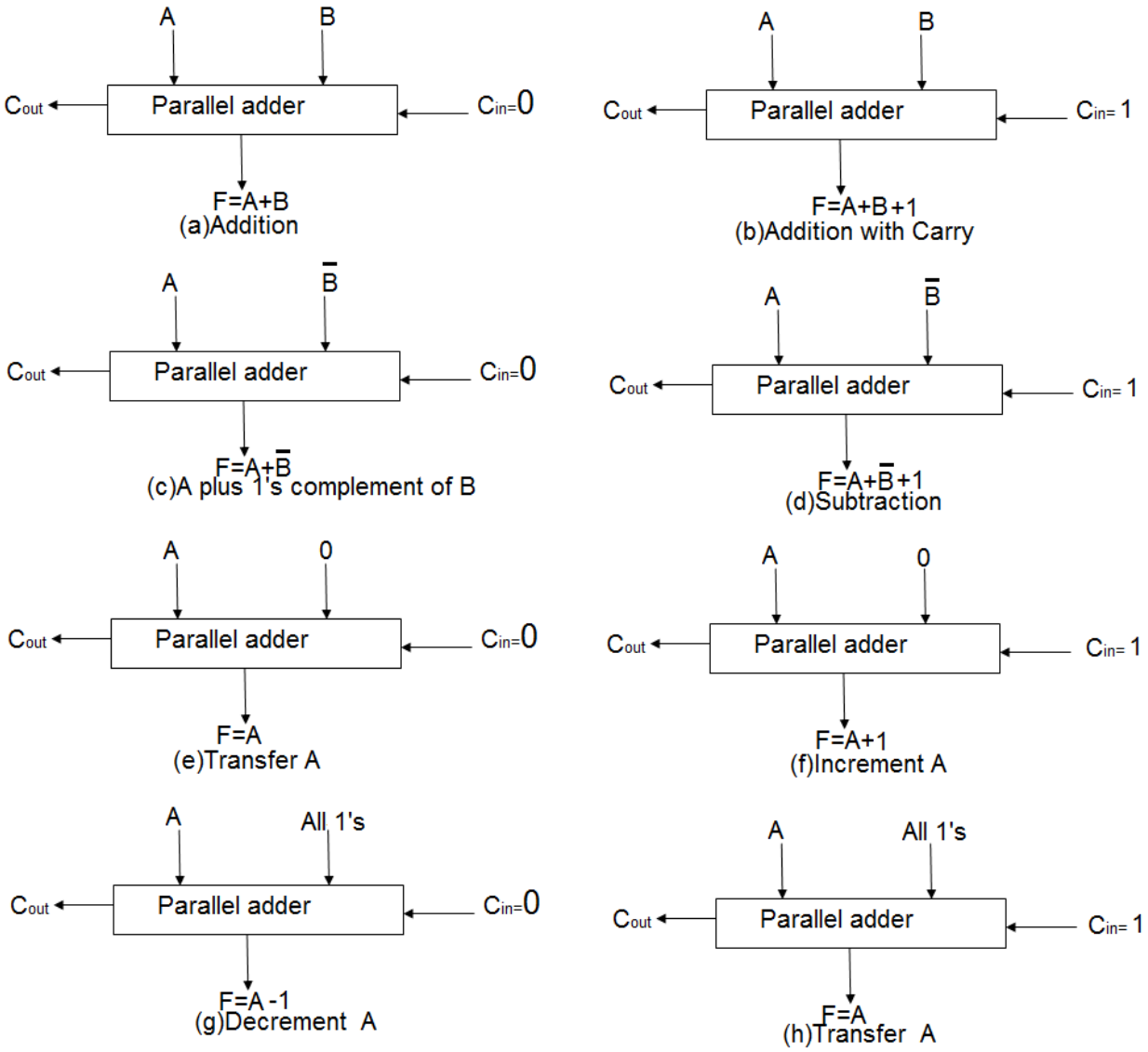

Figure 3. Eight operations obtained by controlling one set of inputs to a parallel adder

V. CONVENTIONAL LOGIC DIAGRAM OF ARITHMETIC LOGIC UNIT

The conventional logic diagram of arithmetic logic unit is shown in figure 4.The S_2,S_1 and S_0 are the selection lines and C_{in} is the input carry ,A_i,B_i are the input lines .When S_2=0,the circuit performs eight arithmetic operations and when S_2=1 we get the four logic operations OR,XOR,AND and NOT. Here the conventional circuit represents for 2 bit arithmetic logic unit. The external circuit consists of NAND,OR and NOT gates ,which controls the input values X_i,Y_i and Z_i of the full adder as well as the circuit operation. The inputs of the full adder can be expressed as follows

$$X_i=A_i + S_2S'_1S'_0B_i + S_2S_1S'_0B'_i$$
$$=Ai + S_2S'_0 (S'_1B_i + S_1B'_i)$$
$$Y_i =S_0B_i + S_1B'_i$$
$$Z_i =S'_2C_i$$

When S_2=0 , input values X_i,Y_i and Z_i are as follows

$$X_i=A_i$$
$$Y_i =S_0B_i + S_1B'_i$$
$$Z_i =C_i$$

And we will get the arithmetic functions. But when S_2=1 , input values X_i,Y_i and Z_i are as follows

$$X_i=A_i$$
$$Y_i =S_0B_i + S_1B'_i$$
$$Z_i =0$$

And logic operations are generated. For $S_2S_1S_0$=101 or 111 the output F_i will be the exclusive OR and complement operation. When $S_2S_1S_0$=100 each A_i is ORed with B_i to provide OR operation. When $S_2S_1S_0$=110 each A_i is ORed with B'_i to provide AND operation.

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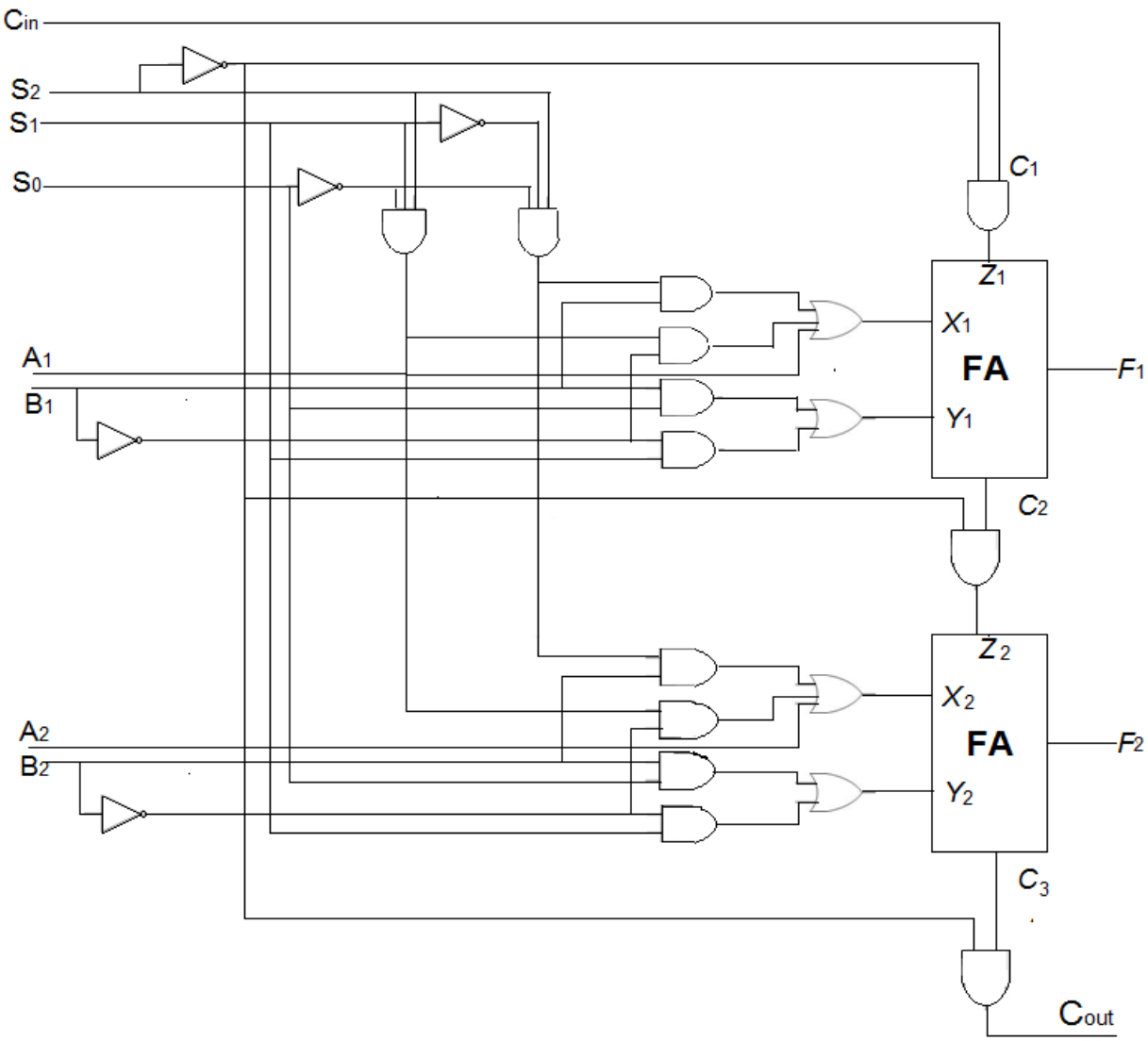

Figure 4. Logic diagram of 2 bit Arithmetic logic unit

The 12 operation generated in the arithmetic logic unit is given below in Table I. The particular function is selected through S_2,S_1 , S_0 and C_{in}

TABLE I:Function Table for the Arithmetic Logic Unit(ALU)

Function select				Output equals	Function
S2	S1	S0	C_{in}		
0	0	0	0	F=A	Transfer A
0	0	0	1	F=A+1	Increment A
0	0	1	0	F=A+B	Addition
0	0	1	1	F=A+B+1	Add with carry
0	1	0	0	F=A+B’	Substract with borrow
0	1	0	1	F=A+B’+1	Subtraction
0	1	1	0	F=A-1	Decrement A
0	1	1	1	F=A	Transfer A
1	0	0	X	$F=A \cup B$	OR
1	0	1	X	$F=A \oplus B$	XOR
1	1	0	X	$F=A \cap B$	AND
1	1	1	1	F=A’	Complement

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VI. DESIGN OF CONTROL UNIT BY REVERSIBLE GATES

We have designed the control unit of arithmetic logic unit by reversible gates shown in figure 5. We have used here three PERES gates , one FREDKIN gate and three FEYMAN gates. From the control unit we will get three input values X_i ,Y_i and Z_i for the full adder. The quantum cost of this proposed circuit is 20.

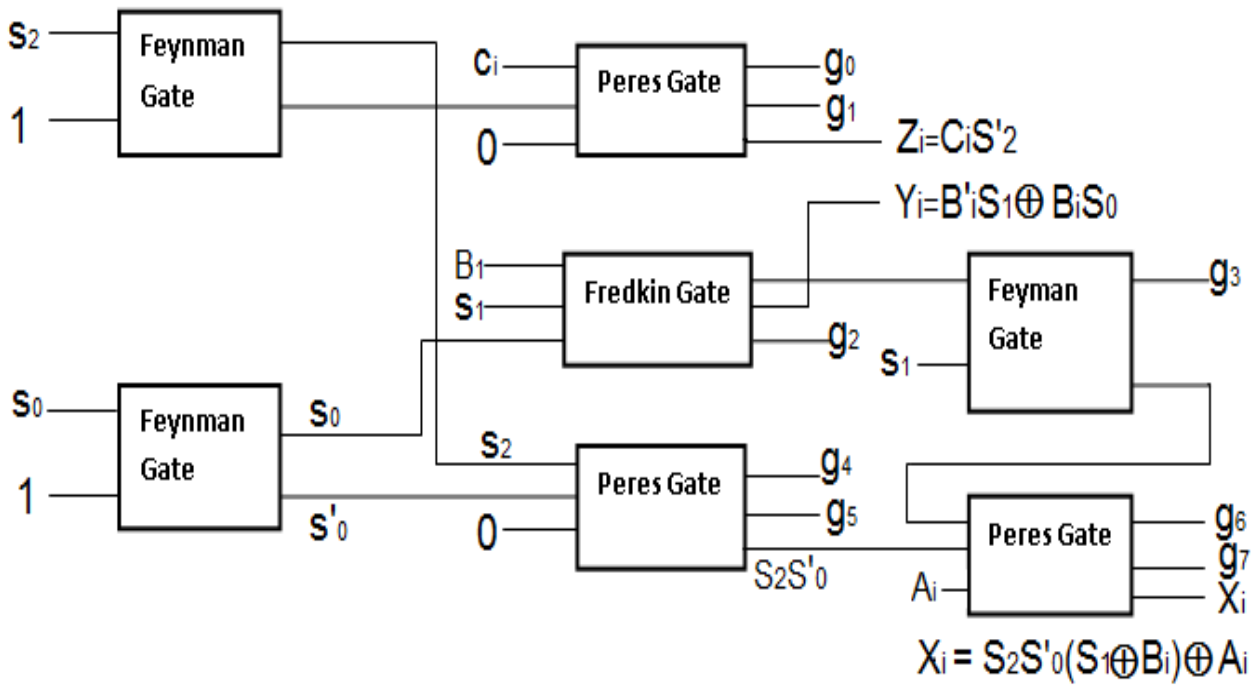

Figure 5. Proposed Control Unit for Arithmetic logic unit

VII. IMPLEMENTATION OF 1-BIT ARITHMETIC LOGIC UNIT BY REVERSIBLE GATES

We can implement one bit arithmetic logic unit by using the proposed control unit shown in fig 6. we can see that the inputs X_i ,Y_i and Z_i can be controlled depending upon the values of the selection lines S_2, S_1 S_0 and carry input C_{in} and the input values of A_i ,B_i.The final output is F_i will be of 12 different operations either arithmetic or logical, depending upon the values of selection lines and carry input.

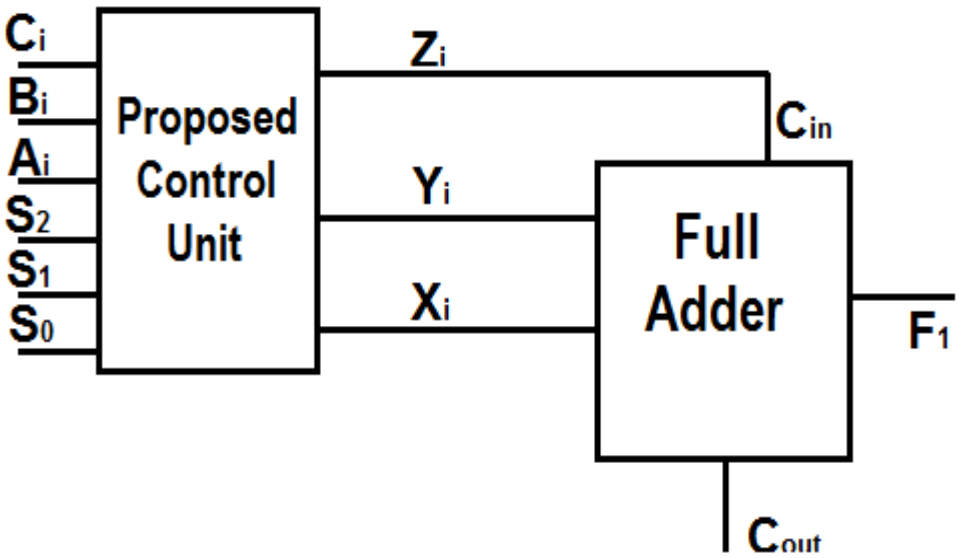

Figure 6. Proposed control unit to construct ALU

We can now implement the 1 bit arithmetic logic unit for twelve operations by cascading the proposed control unit which is consist of reversible gates and a full adder shown in figure 7. But here DKFG reversible gate has been used as a full adder. So we need one DKFG reversible gate for constructing 1 bit ALU. So finally eight reversible gates are required to design 1bit ALU. There are ten number of garbage values. The quantum cost of this proposed circuit is 27.We can construct n-bit ALU by cascading n number of this 1–bit ALU circuit.

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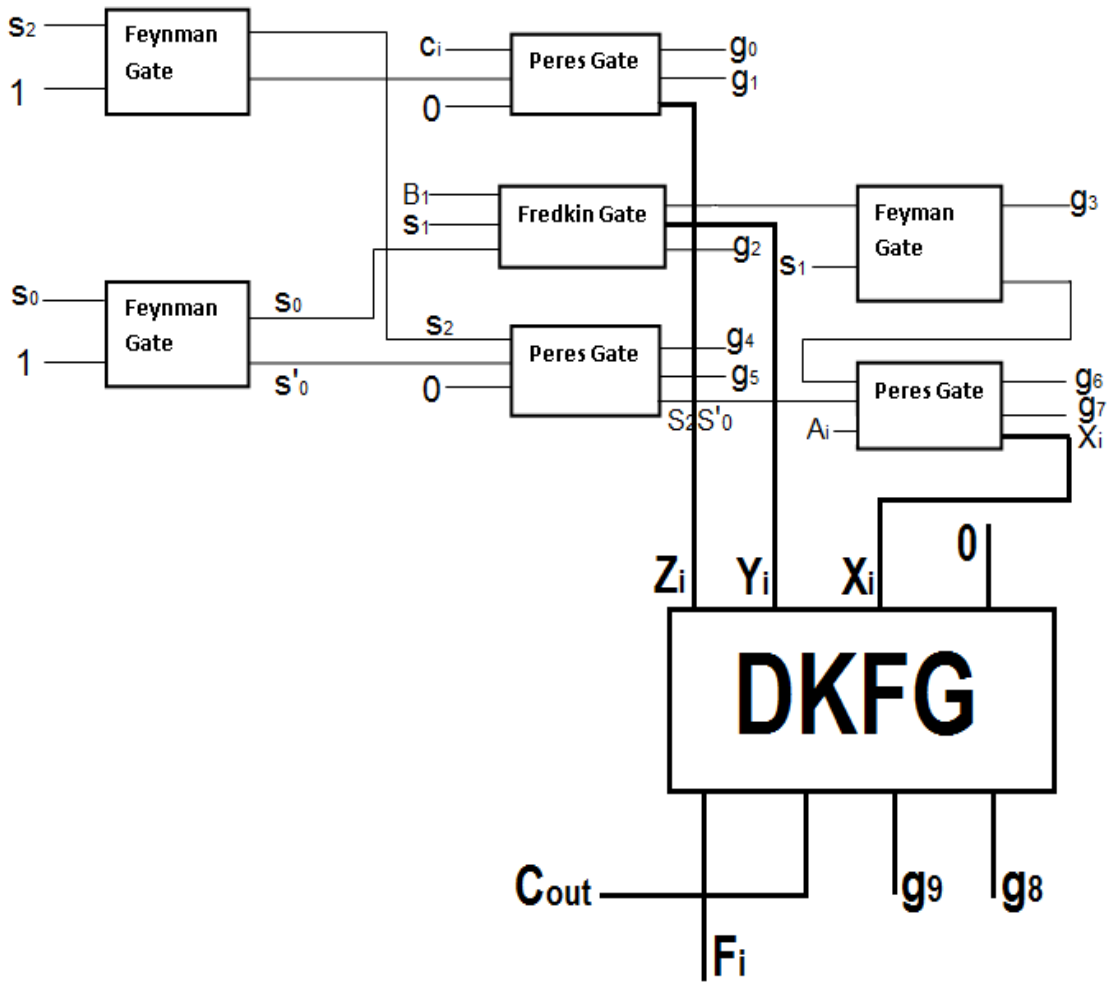

Figure 7. Proposed 1 bit arithmetic logic unit for 12 operation

TABLE II
COMPARISON OF EXISTING 1 BIT ALU AND CONTROL UNIT TO THE PROPOSED ONE

Parameter Which has to be compared	1 bit ALU			Control unit		
	Existing 1 bit ALU[14]	Existing 1 bit ALU[15]	Proposed 1 bit ALU	Existing control unit[14]	Existing control unit[15]	Proposed control unit
Gate count	22	10	8	15	9	7
Garbage outputs	12	8	10	8	6	8
Constant input	10	4	3	8	3	2
Quantam cost	53	29	27	41	23	20

VIII. CONCLUSION

In this paper, a new control unit consists of reversible gates is proposed for realizing 1-bit arithmetic logic unit . We also used DKFG reversible gate as a Full Adder for this designing of ALU. We have compared these proposed design with the existing designs [14,16] in terms of reversible gates used, garbage outputs, quantum cost, constant inputs, & arithmetic functions. Arithmetic reversible control unit has also great improvement over existing designs [14, 15]. So the proposed design is an optimized realization and its implementation of reversible ALU in terms of number of gates used, garbage outputs and constants input can be used for low power applications. In future we can design complete reversible computer architecture with the help of proposed designs. The reversible ALU will be a central unit in a future design of a fully reversible architecture using only reversible logic elements..

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