Volume 4, Issue 1, January 2014 ISSN: 2277 128X

International Journal of Advanced Research in Computer Science and Software Engineering

Research Paper

Available online at: www.ijarcsse.com

Low Power QPSK Modulator on FPGA

Prashant D. Thombare *, Ameed M. Shah
Electronic and Telecommunication Engineering
Government College of Engineering, Amravati, India

Abstract — QPSK is a widely used digital modulation technique in wireless communication, such as TDMA cellular telephone, OFDM, Bluetooth, Satellite communication etc. due to its higher noise immunity, bandwidth efficiency and simpler circuitry. Speed, power and area are the three main factors taken into consideration while designing any electronic system. Low power devices are always demanding for electronic devices since power consumption is one of the main factors; the focus is given on reducing the power consumption of the device. To minimize the power consumption the size of actual block diagram is reduced by removing some blocks which will provide the same output signal. In this paper a QPSK modulator is proposed and discussed to implement on FPGA kit using Active HDL coding software tool.

Keywords— QPSK, FPGA, MATLAB, Simulink, ROM, Serial in Parallel out (SIPO), DAC etc.

I. INTRODUCTION

Modulation is the process of sending data signal over carrier signal to minimize the noise or fading effect. They are mainly divided into two categories i.e., analog and digital. In analog modulation carrier signal is modulated with the help of analog data signal and in digital it modulates with digital signal. Digital modulation is called shift keying because in this, the carrier signal is shifted in amplitude, frequency or phase by digital input signal. Different PSKs can be obtained by M-ary PSK, where M is the no. of states or no. of phase shifts which is depend upon the no. of signals are combined for modulation. In QPSK two signals are combined for modulation. BER of QPSK is better than higher order PSK signals such as 8-PSK, 16-QAM, 32-QAM etc. which are easily affected by noise. At higher order PSK, larger bandwidth is require for higher data transfer rate and consume more power, whereas QPSK is more bandwidth as well as power efficient.

There are many applications where QPSK modulator is used, out of which few are of battery operated devices such as Bluetooth, TDMA cellular communication, Medical Implant Communication Services (MICS) etc. therefore it is necessary to minimize the power consumption of these devices so that the battery will last for longer time. It can be reduce by reducing size of circuit or reducing the speed of operation.

II. CONVENTIONAL MODULATOR

The QPSK modulator can modulate two signals in same frequency band as shown in fig. 1. Each signal is to be converted from analog to digital, then modulate one signal with sine and another with cosine which gives four different phase shifts with two signals, by adding these two phase shifted signals we get QPSK output signal[1].
The QPSK signal can be given as

$$S_{QPSK} = \sqrt{\frac{2Es}{Ts}} \cos\left(2\pi f_c t + (i-1)\frac{\pi}{2} \right) \quad \text{for} \quad i = 1, 2, 3, 4 \tag{1}$$

Where,

$\sqrt{\frac{2Es}{Ts}}$ = Constant amplitude with E_s energy and T_s time period of the signal

f_c= Frequency of carrier signal

i = phase no. of signal as per the symbols of the data signal

from the trigonometric equation given below,

$$\cos(A+B) = \cos(A)\cos(B) - \sin(A)\sin(B) \tag{2}$$

Fig. 1. Shows that separate sine and cosine waves are generated which require two ROM's to store these signals [2]. This is then modulated by the input binary data signal. These two signals are then added to generate the QPSK signal. All these process is discuss in [5] with design flow diagram.
from eq. (2) we can write

$$S_{QPSK} = \sqrt{\frac{2Es}{Ts}} \cos(2\pi f_c t)\cos[(i-1)\frac{\pi}{2}] - \sqrt{\frac{2Es}{Ts}} \sin(2\pi f_c t)\sin[(i-1)\frac{\pi}{2}] \tag{3}$$

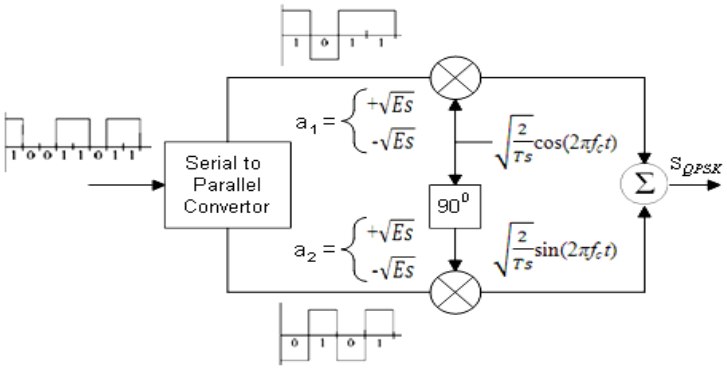


Fig. 1. Conventional block diagram of QPSK modulator

There are two signals in QPSK signal i.e. in phase I(t) and Quadrature phase Q(t). Which is given in eq. (3) can be written as

$$S_{QPSK} = \sqrt{\frac{2}{Ts}} \cos(2\pi f_c t)\, I(t) - \sqrt{\frac{2}{Ts}} \sin(2\pi f_c t)\, Q(t)$$

where,

$I(t) = \sqrt{Es}\cos[(i-1)\frac{\pi}{2}]$ and $Q(t) = \sqrt{Es}\sin[(i-1)\frac{\pi}{2}]$

Output QPSK waveform with four different phase shifts is as shown in fig. 2. In this, we can see that for each symbol phase angle of original signal is different.

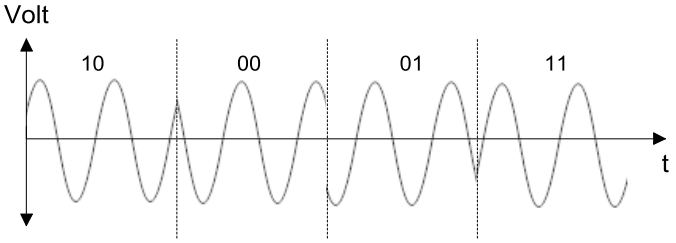


Fig. 2. Output waveform of QPSK modulator i.e., S_{QPSK}

III. PROPOSED WORK

We can see, day by day the digital devices are getting smaller, many research is going on to minimize the size of the design which reduce the power consumption of the device, hence cost of the device will get reduce. If we observe the QPSK output waveform, we found that there is a sinusoidal wave shifting with the change in symbol and the phase angle is same for different symbols as shown in table 1, means we can say that, for specific symbol there will be specific phase shift output signal. So, instead of generating the phase shift by multiplying data signal with carrier one, we will just store the signal in ROM and call it for specific symbol from specific phase. It means the output waveform will be the same sinusoidal signal with starting from specific phase angle. In this case we don't require more than one ROM to store our signal since it is only the sinusoidal signal. We just have to start the output signal from different phase angle according to input symbol (00, 01, 11, 10). The phase shift angle may be 0^0, 90^0, 180^0 and 270^0 or it may be 45^0, 135^0, 225^0 and 315^0. In proposed block diagram as shown, we are shifting signal from 45^0.

The constellation diagram shows the phase angle and amplitude of signal for different symbols. In above diagram the phase angles are 45^0, 135^0, 225^0 and 315^0 for "00", "01", "11" and "10" respectively. The symbols are taken as gray codes i.e. one bit change per symbol or 90^0 phase shift per symbol.

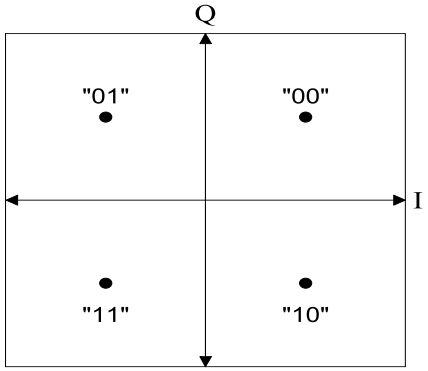


Fig. 3. Constellation diagram of QPSK modulator

TABLE I
PHASE SHIFTED SIGNAL FOR DIFFERENT INPUT SYMBOLS

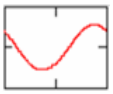
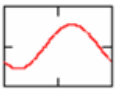
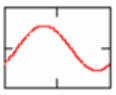
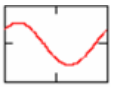
Symbol	Bits	S(t)	Phase (Deg.)	Mod. Signal
S1	00	$\sqrt{\frac{2Es}{Ts}}\cos(2\pi f_c t + \frac{\pi}{4})$	45^0	
S2	01	$\sqrt{\frac{2Es}{Ts}}\cos(2\pi f_c t + \frac{3\pi}{4})$	135^0	
S3	11	$\sqrt{\frac{2Es}{Ts}}\cos(2\pi f_c t + \frac{5\pi}{4})$	225^0	
S4	10	$\sqrt{\frac{2Es}{Ts}}\cos(2\pi f_c t + \frac{7\pi}{4})$	315^0	

Table I shows the phase change of the signal is depend on the change in symbols, each symbol is having particular phase angle or signal pattern. The proposed block diagram is shown in fig. 4, the size of the design is reduced up to much extent, no. of blocks is few as compared to conventional block diagram. In proposed block diagram only one ROM is used for carrier signal instead of two ROMs for sine and cosine signal generator. Each block of proposed block diagram is as explained below,

A. Carrier Source

It provides a sinusoidal carrier signal of specific frequency which is modulated by the data signal. A ROM is used to store the amplitude values of the signal which can be read by using VHDL coding for FPGA to produce sine signal. On board frequency is in MHz which is high to observe the output signal on DSO, a shift register can be developing to provide various frequency signals.

B. Phase Shifter

It shifts the sine signal into four different angles as shown in fig. 4. It is nothing but the ROM which stored the sinusoidal signal and we are sending the signal at the output with different starting point of signal or different phase angle which is specific for different symbols. Actually it is a DMUX which takes one input as carrier signal i.e. sinusoidal signal and giving output as different phase shifted sinusoidal signal. These output are selected by two select lines which are two input signals I and Q.

C. Shift Register

Practically we take two input data signals to modulate them with same carrier signal, but on board we need to generate two signals from a random signal. Here we are taking one data signal and separating it into two signal i.e. Serial in Parallel out (SIPO).

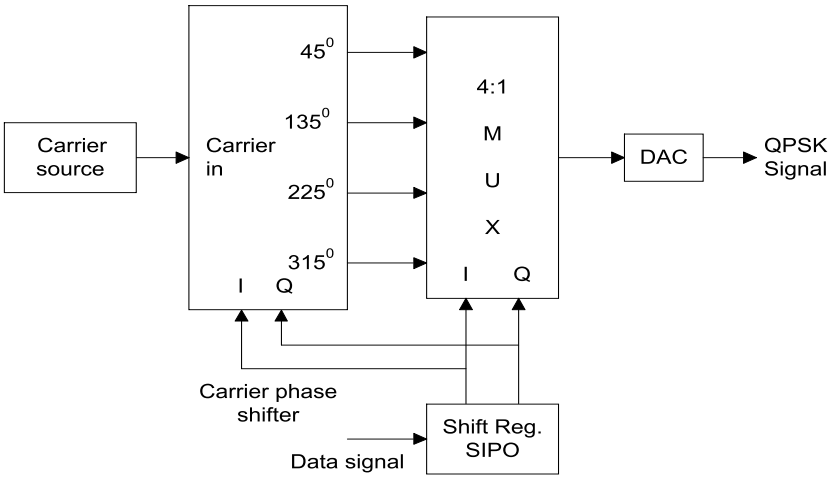


Fig. 4. Proposed block diagram of QPSK modulator

D. Multiplexer

It selects only one signal at a time out of four shifted signals and gives as output QPSK signal. The signal is selected by two select lines I and Q, means output will be the phase shifted signal according to the input symbol.

E. DAC

All the above blocks can be dump into FPGA kit which gives output digital QPSK signal so, we need to convert it into analog form using DAC. The waveform can be observed on DSO.

The ROM contains values of sinusoidal signal, it requires a clock to read the values i.e. one value per clock pulse, similarly shift register require a clock signal to take input data signal then

$T = \frac{1}{fc} * x = T_d$

Where,

T = Time period of sine signal

x = No. of values stored in the ROM

f_c = clock frequency applied to carrier signal

T_d = Time period of data signal

To divide the frequency a divider block with factor x is required to design, it will take the input clock frequency f_d which is to be divided by x to get the frequency equal to freq. of sine signal.

In this paper, Active HDL tool is use to generate the blocks with VHDL coding. The FPGA kit will be use to implement these blocks on hardware to observe the output waveform. But the FPGA is a digital circuit which provide digital output signal hence we need a DAC to covert this signal to analog one and it can be observe on DSO. Before this the Simulink software is used to verify the block diagram and check it's output waveforms.

IV. CONCLUSION

In this paper we try to achieve a design which will give the same result by minimizing it's size or area. The reduced size of the design will reduce the power consumption. The proposed block diagram replaces several block diagram such as adder, multiplier and minimizes no. of ROMs which will help to increase speed of operation of the design. It means proposed block diagram try to improve all the three main factors which are taken into consideration for any system design. The comparison of performance between conventional and proposed design can be done on FPGA kit i.e. speed, device utilization, power consumption etc.

ACKNOWLEDGMENT

We thank to all the staff and friends who helps to get the ideas, the material related to the topic and providing facility of software and manuals.

REFERENCES

[1] S.O. Popescu, A.S.Gontean and D.Ianchis, "QPSK Modulator on FPGA," *IEEE 9th International Symposium on Intelligent Systems and Informatics*, September 8-10, 2011, Subotica, Serbia

[2] Wenmiao Song, Qiongqiong Yao, "Design and Implement of QPSK Modem Based on FPGA" North China Electric Power University, Baoding, China.

[3] Michal Kováč "BPSK, QPSK Modulator Simulation Model" Doctoral Degree Programme (1), FEEC BUT.

[4] A. Amsavalli, K.R. Kashwan, "FPGA Implementation of Low Complexity VLSI Architecture for DS-CDMA Communication System," *International Journal of Computer Applications* (0975 – 8887) Volume 42– No.20, March 2012

[5] K. A. Monpara, S. B. Parmar, "Design and Implementation of QPSK Modulator Using Digital Subcarrier," *Journal of Information, Knowledge and Research in Electronics and Communication Engineering*, ISSN: 0975 – 6779, Nov 11 to Oct 12, Volume – 02, Issue - 01 p.no. 394-398

[6] G. Elamary, G. Chester, J. Neasham, "A Simple Digital VHDL QPSK Modulator Designed Using CPLD/FPGA for Biomedical Devices Applications," *Proceedings of the World Congress on Engineering* 2009 Vol. I, WCE 2009, July 1 - 3, 2009, London, U.K.

[7] A. M. Moubark, Mohd. Alauddin Mohd. Ali, Sawal Hamid Md Ali, Hilmi Sanusi, "FPGA Implementation of Low Power Digital QPSK Modulator using Verilog HDL," *Journal of Applied Science* 13(3): 385-392, 2013

[8] A.M.Bhavikatti, Subhash Kulkarni, Uday Kalyani, " FPGA Implementation of π/4 -QPSK Modulator and Demodulator," *IJCEM International Journal of Computational Engineering & Management*, Vol. 15 Issue 4, July 2012

[9] T. Sakla, D. Jain, S. Gautam, "Implementation of Digital QPSK Modulator By Using VHDL /Matlab," *International Journal of Engineering Science and Technology*, Vol. 2(9), 2010, pp.4827-4831

[10] B. Krongold, Timo Pfau, N. Kaneda and S. C. Jeffrey Lee, "Comparison Between PS-QPSK and PDM-QPSK With Equal Rate and Bandwidth," *IEEE Photonics Technology Letters*, Vol. 24, No. 3,pp. 203-205 Feb. 1, 2012

[11] Jason H. Anderson, F. N. Najm, and Tim Tuan, "Active Leakage Power Optimization for FPGAs," pp. 33-41.

