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Study of Various Techniques for Designing of Efficient FIR Digital Filter

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Abstract: Finite Impulse response filters are highly desirable in digital filter design because of their inherent stability and linear phase. These are often used in phase-sensitive applications because they can always be designed to have linear phase. However, when narrow transition band characteristics are required, they typically have a much higher filter order than their infinite impulse response counterparts with equivalent magnitude spectrums [1]. In this paper various techniques are discussed and described how these techniques reduce the power consumption of Digital Filter, making it more efficient.

Key words: FIR filter, linear phase, Design techniques, coefficient, power.

I. Introduction:

The recent proliferation of portable battery-powered gadgets that make extensive use of Digital Signal Processing (DSP) and demand an ever improving performance, like cellular phones, laptop computers etc. has made low power high performance DSP increasingly important. One of the most basic operation performed in DSP applications is Finite Impulse Response (FIR) filtering. An N-tap FIR filter perform the following convolution:

$$Y_j=\sum C_k X_{j-k}$$

The C_k's are called the coefficients of the filter, Xj and Y_j are the j-th component of the input and output sequences respectively.

Design techniques for FIR filters can vary widely from one that uses dedicated hardware multipliers and adders to one that uses code which is executed by a general purpose processor and its ancillary units. A combination of hardware and software that allows sharing of multi-purpose hardware units (like adders and multipliers), without using a full-fledged processor can also be used. In all these implementations the basic FIR filtering algorithm called the multiply and accumulate sequence, remains same. There are three significant sources of power dissipation in CMOS circuits: the switching component $\mathbf{P_{sw}}$, the short circuit component $\mathbf{P_{sc}}$ and the leakage current component $\mathbf{P_{leakage}}$.Various techniques have been investigated in the past to control and minimize their contributions to the total power dissipated in CMOS circuits, with the constraint of acceptable performance. Since P_{sw} is often the most significant contributor, efforts have been focused on reducing P_{sw} .These techniques can be grouped into the following four broad categories: a)Technology level b) Circuit level c) Architecture level d)Algorithm level[5].

II. Review on different design techniques of Digital Filter

Eugene B. Hogenauer [2] in their research presented a class of digital linear phase finite impulse response (FIR) filters for decimation and interpolation. They require no multipliers and use limited storage making them an economical alternative to conventional implementations for certain applications. According to him a digital filter in this class consists of cascaded ideal integrator stages operating at a high sampling rate and a equal number of comb stages operating at a low sampling rate. The above configuration is designated cascaded integrator-comb (CIC).Using CIC filters, the amount of passband aliasing or imaging error can be brought within prescribed bounds by increasing the number of stages in the filter. However, the width of the passband and the frequency characteristics outside the passband are severely limited.

Y.C. Lim [3] describes in his research Frequency Masking Technique to design linear phase digital filter. According to this technique if each delay element of a linear phase low-pass digital filter is replaced by M delay elements, an (M+1) band filter is produced. The transition width of this (M+1) band filter is 1/M that of prototype low pass filter. A complimentary filter can be obtained by subtracting the output of the (M+1) band filter from suitably delay version of the input. If frequency responses of original filter and its complimentary are properly masked and recombined,narrow transition band filter can be obtained with very sharp transition band which result in saving in arithmetic operations as high as four to one.

M. Mehendale,S.D. Sherlekar and G. Venkatesh [4] describes in their research an algorithm for optimizing coefficients of a Finite Impulse Response(FIR) filter, so as to reduce power dissipation of its implementation on a programmable Digital Signal Processor. In this paper author first identify that the power dissipation depends on the total Hamming distance between successive coefficient values and design an algorithm to minimize the Hamming distance. The algorithm achieves this optimization in two stages. The first stage uses coefficient scaling technique and the second phase adopts local strategy for coefficient perturbation. Experimental results on six FIR filter examples show that the coefficient optimization algorithm results in upto 36% reduction in the total Hamming distance which reduces the power dissipation In the coefficient memory data bus and multiplier.

N. Sankarayya and Kaushik [5] Roy describes in his work a algorithm level technique which is known as Differential Coefficient Method(DCM).A low power FIR filter is realized by using this algorithm which use various orders of differences between coefficients for computing the convolution with input data rather than directly the coefficients. The results of computations are stored and reused, thus requiring more storage and storage accesses. This technique result in a reduction in the computations necessary per convolution as compared to directly using the coefficients which result in a net energy dissipated. It require more storage.

S.F. Lin, F.S. Yang, C.W. Ku and L.G. Chen [6] presents a novel approach for implementing power-efficient finite impulse response (FIR) filters that requires less power consumption than traditional FIR filer implementation in wireless embedded systems. The proposed scheme is the combination of following methods.

a)Symmetrical retimed direct form architecture(SRDFA) b) Balanced modulator architecture(BMA) c) Separated signed processing architecture(SSPA) d) Modified to CSD representation(MCS).

In this work the author also compare above methods with reference to the power consumption. From power analysis the SRDFA just needs 47% power consumption compare with the original direct-form architecture. Applying BMA will reduce to 64% of original power. By combining SSPA with MCSD representation, the power consumption can be reduced to 78% of the original one. If the four schemes are adopted together, the power consumption can be further decreased to 24% from the original direct-form architecture. Simulation results are shown in table I and fig1.

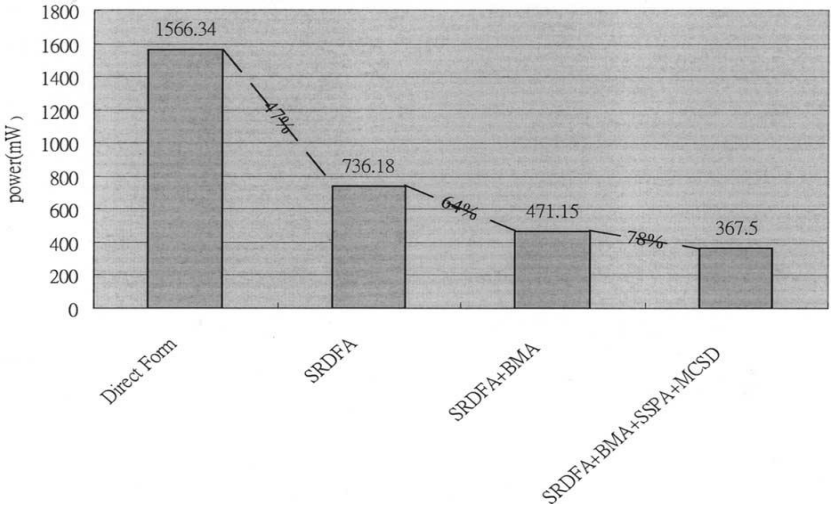

fig1. Power comparison of the proposed four schemes.

TABLE I

COMPARISON RESULTS OF THE PROPOSED FOUR SCHEMES

	Direct Form	SRDFA	SRDFA+BMA	SRDFA+BMA+ SSPA+MCSD
power(mW)	1566.34	736.18	471.15	367.5
Area(transistor)	88923	48095	52805	39816
Vdd(v)	5	5	4	4
Frequency	50MHz	50MHz	50MHz	50MHz

The designed filter by S.F. Lin is a combination of four techniques which results reduction of 76% power consumption of the original direct form structure with slight area overhead.

R.Mahesh and A.P. Vinod [7] describes in his work coefficient decimation approach for designing low complex and reconfigurable FIR filter. According to their work if every M^{th} and replacing all other coefficient to zero, a multiband frequency response is obtained having center frequency at $2*\pi K/M$,where K is an integer having value 0 to M-1.If these frequency responses properly masked, different filters are obtained. If every M^{th} coefficient grouped together removing zero coefficients, a decimated frequency response obtained in comparison to the original filter. This results in to low complexity because of less multiplication and addition. It also results in design of reconfigurable FIR filter design by simply controlling the coefficient.

Z. U. Sheikh [8] presented in his work Coefficient decimation technique using linear programming, which gives better results in terms of approximation error than previous work done by R. Mahesh and A.P. Vinod.The comparison of this

technique with the conventional technique (previous work) in terms of approximation error is given in following table for different value of decimation factor (D_{max}) .

TableII: Maximum approximation errors for different $D_{max.}$

D_{max}	Proposed	Conventional
1	-55.97dB	-55.97dB
2	-55.50dB	-47.30dB
3	-55.37dB	-47.03dB
4	-55.27dB	-45.25dB

III. Conclusion:

The need of the hour is an efficient Digital Filter in terms of low power and area. Low power consumption is achieved in a digital filter by reducing in computational complexity through different techniques given by various author. Although FIR filters have much greater computational complexity than IIR counterparts with equivalent magnitude spectrums, linear-phase characteristics are often desirable. The review of different techniques provide avenue for further research for minimizing the power of a Digital Filter.

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