



Implementation and Comparative Study of Adder Circuit for Low Power & High Performance System

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Abstract: Adding two binary numbers is a basic operation in binary electronic processing system. Adder plays an imperative role in arithmetic process such as addition, subtraction, multiplication, division etc. In VLSI applications, area, delay and power are the key factors which must be taken into account in the design of a fast adder for high performance system. The depiction and optimization of such adder will support in comparison and choice of adder modules in system design. This paper deals with the performance & comparative study of the power, delay, and power delay product (PDP). In this paper, adder using transistors is designed and simulated with the help of DSCH 3.1 and Microwind3.1 CAD tool.

Keywords— VLSI, CMOS, PDP, adder and low power.

I. INTRODUCTION

Addition is one of the fundamental arithmetic operations. It is used extensively in many VLSI systems such as application specific DSP architectures and microprocessors[1]. In addition to its main task, which is adding two binary numbers, it is the nucleus of many other useful operations such as subtraction, multiplication, division, address calculation, etc. In electronics, an adder or summer is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations. VLSI design is a modular methodology for saving microchip area by minimizing the interconnect fabrics and to increase circuit efficiency in terms of complexity of circuit, power consumption and frequency response associated to the design. Logic chip such as microprocessor chip and digital signal processing chips contains large array of memory cell and different functional unit. Hence their design complexity is considered much higher than memory chip. the level of circuit performance depend on the efficiency of the design methodology and design style[2,3].

Several logic styles have been used in the past to design full adder cells. Each design style has its own merits and demerits. Classical designs of full adders normally use only one logic style for the whole full-adder design. In this paper, the power and delay performance characteristics of adder using 10-transistor, 14 transistor and 28 transistor adder circuits has been verified. The basic advantage of 10 transistors full adders [4]-[7] are low area compared to higher gate count full adders, lower power consumption, and lower operating voltage.

II. LITERATURE REVIEW

Various static CMOS logic styles have been used to implement low-power and high-performance Full Adder. The power dissipation is one of the most serious design parameter in battery performance. The three most commonly conventional metric to measure the value of a circuit or to evaluate various circuit styles are area, delay and power dissipation. Portability imposes a strict limitation on power dissipation while still demands high computational speeds. Therefore now a days the power-delay product becomes the most essential metric for the performance system in VLSI. The design of VLSI is a modular methodology for saving microchip area by minimizing the interconnect fabrics and to increase circuit efficiency in terms of complexity of circuit, power consumption and frequency response associated to the design. The diminution of the power dissipation and the improvement of the speed require optimizations at all levels of the design procedure. A detailed assessment of the existing CMOS circuit design styles is explained and implementation of adder circuit with the help of transistors were studied in the terms of delay and power consumption using micro wind.

CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication [1]. Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Significant power is only drawn when the transistors in the CMOS device are switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor-transistor logic (TTL) or NMOS logic.

III. CMOS CONCEPT

Complementary metal-oxide-semiconductor (CMOS) is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS also allows

a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips. The phrase "metal-oxide-semiconductor" is a reference to the physical structure of certain field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor material.

CMOS circuits use a combination of p-type and n-type metal-oxide-semiconductor field-effect transistors (MOSFETs)[1,3].The CMOS transistors (devices) are formed by the intersection of the polysilicon and diffusion; N diffusion for the N device & P diffusion for the P device[6]. The output is connected together in metal. Connections between metal and polysilicon or diffusion are made through contacts. The N device is manufactured on a P-type substrate while the P device is manufactured in an N-type well (n-well) as shown in figure 1. A P-type substrate "tap" is connected to V_{SS} and an N-type n-well tap is connected to V_{DD} to prevent latch up.

IV. POWER DELAY PRODUCT

The power-delay product is a figure of merit correlated with the energy efficiency of a logic gate[3,5] i.e in other word we can say that figure of merit is used to determine quality of a digital gate and also determines the energy of gate. The PDP is measured in Femto joule. By reducing the number of transistor it is possible to reduce the delay of all adders without significantly increasing the power consumption[6]. This helps to achieve minimum PDP. To achieve minimum PDP, an iterative process of redesigning and transistorizing was carried out. The comparison of full adders designed to achieve minimum PDP is discussed below.

V. ARCHITECTURE OF ADDER

Adder is one of the most important components of a CPU (central processing unit), Arithmetic logic unit (ALU), floating point unit and address generation like cache or memory access unit use it[4].

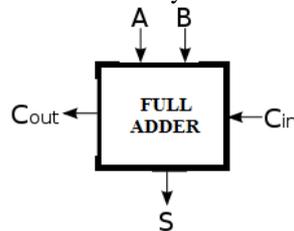


Fig. Full Adder

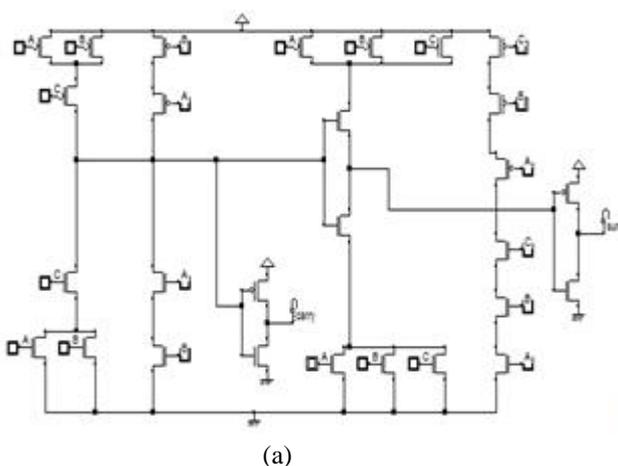
In addition, Full-adders are important components in other applications such as digital signal processors (DSP) architectures and microprocessors. Arithmetic functions such as 'addition', 'subtraction', 'multiplication' and 'division' are some examples, which use 'adder' as a main building block. Addition is the most commonly used arithmetic operation in microprocessors and DSPs, and it is often one of the speed-limiting elements [2], [7]. Hence optimization of the adder both in terms of speed and power consumption should be pursued. In the following section we briefly describe the adder modules.

The 28 Transistor full adder is the pioneer CMOS traditional adder circuit. The schematic of this adder is shown in Figure 1. This adder cell is built using equal number of N-fet and P-fet transistors [5]. The logic for the Complimentary MOS logic was realized using the Eqs.(1) and (2)

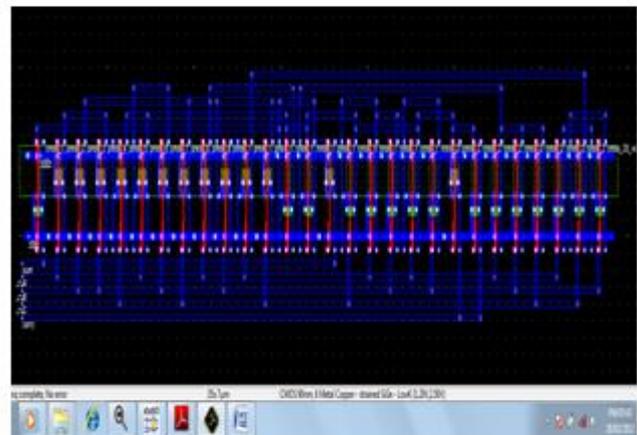
$$C_{out} = AB + BC_{in} + AC_{in} \quad (1)$$

$$Sum = ABC_{in} + (A + B + C_{in}) C'_{out} \quad (2)$$

The first 12 transistors of the circuit produce the C_{out} and the remaining transistors produce the Sum outputs. Therefore the delay for computing C_{out} is added to the total propagation delay of the Sum output. The structure of this adder circuit is huge and thereby consumes large on-chip area [3-4].



(a)



(b)

Fig.1. CMOS adder & its layout using 28 transistors.

The 14 transistor full adder is shown in figure 2. The 14 transistors are used to realise the adder function [6]. This design is area efficient. The 14 transistor is adder circuit is similar to transmission gate adder cell and implement the complementary pass logic to drive the load. Layout of 14 transistors as shown in figure 2.

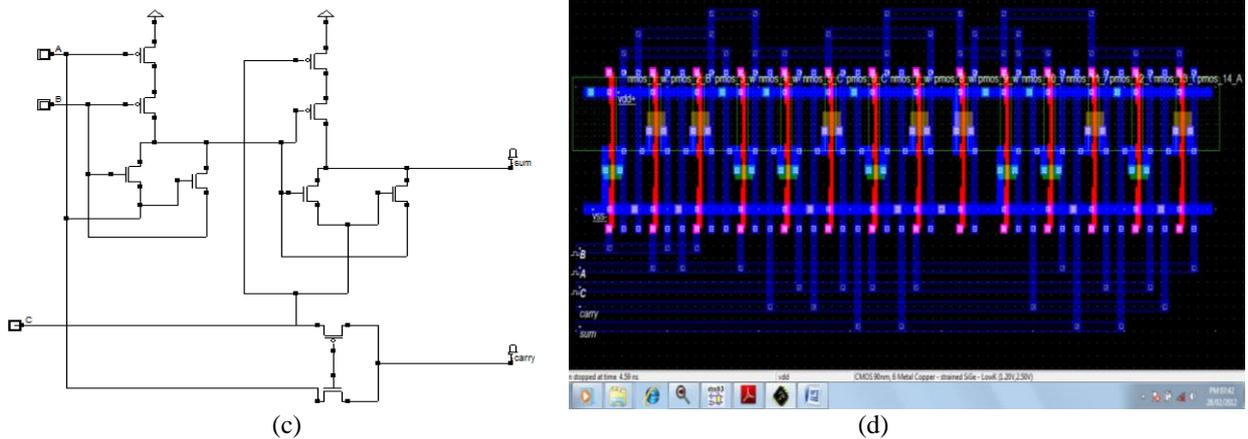


Fig. 2 Schematic & Layout of adder using 14 transistors

The adder using 10 transistors is as shown in figure and does not require any inverter. In non energy recovery design the charge applied to load capacitance during logic level high is drained to the grounded during the logic level low. The schematic of 10 transistor adder and its layout is as shown in figure 3.

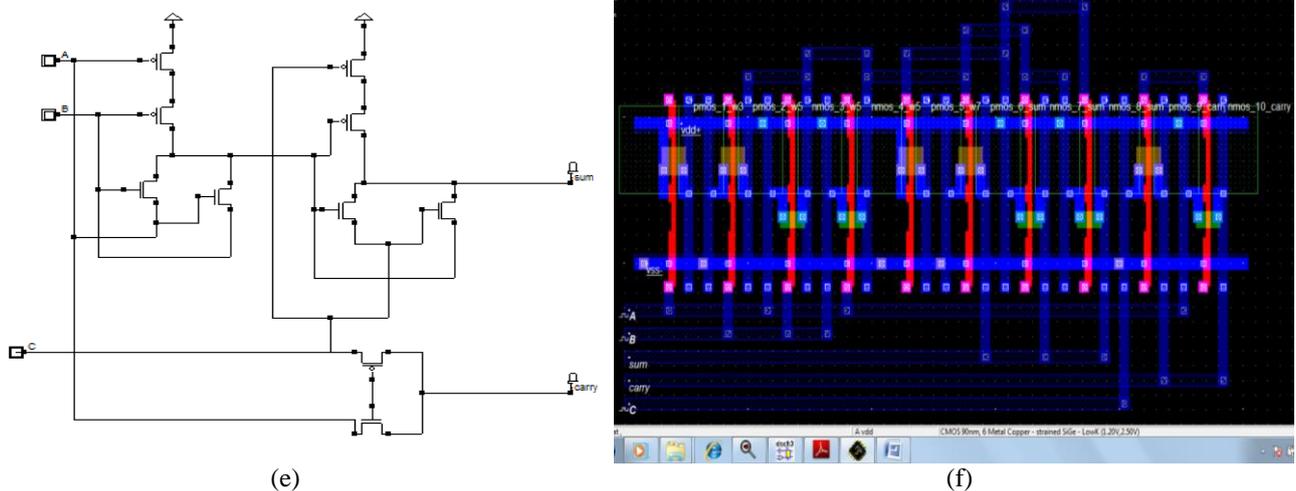


Fig.3 Schematic & Layout of 10 transistor adder

VI. SIMULATION RESULT

28 transistor, 14 transistor and 10 transistor adder circuit are implemented in micro wind 3.1 tool and obtained various result are presented in following table .

Parameter	28T	14T	10T
Power	49.67μ	27.13μ	14.07μ
Delay	10ps	10ps	19ps
PDP	0.49f	0.271f	0.267f

From the table it cleared that power consumption of 28T is more as compared to 14T and 10T . The delay of 10T is some more than the other having more frequency. power delay product of 14T is less than 10T and 28T then also 10T adder is best because less transistors are required to construct it , less power consumption and easy to implement .

VII. CONCLUSIONS

In this work, adder circuits using 10T, 14T and 28T are successfully implemented in DSCH 3.1 and Microwind3.1 CAD tool. As less number of transistor consumes less power and their Comparison of power shows less power dissipation by 10T adder whereas 28T adder consumes more power .PDP of 14T adder is less. Finally it is conclude that 10T adder is better in power and power delay product.

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