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## Future to Wireless Systems

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**Abstract**— Wireless systems have seen a large number of researches going on over the past decades. There is an increasing need for bandwidth savings. This paper addresses the main concepts of the Spectrally efficient FDM (SEFDM) systems. SEFDM systems offer better bandwidth savings when compared to the Orthogonal Frequency Finite Division Multiplexing (OFDM) systems while utilizing non-orthogonal overlapped carriers. The study mainly concentrates on the SEFDM transmitters that is considered to be one of the key research challenges. The digital baseband architecture is then presented using modulation algorithm that uses the Discrete Fourier Transform (DFT) implemented efficiently using the Fast Fourier Transform (FFT): the multi-stream architecture, to reduce the circuit area. A modification to the above architecture is performed using the Co-Ordinate Rotation Digital Computer (CORDIC) algorithm that makes the architecture further area efficient. The SEFDM transmitters were synthesized and verified in FPGA. Analysis on circuit area has been performed to ensure the practicality of the SEFDM transmitters.

**Keywords**— SEFDM, OFDM, FFT, CORDIC, FPGA.

### I. INTRODUCTION

Over the past few decades wireless communications have seen tremendous growth which is likely to continue in the future too. This huge demand has led to many advancements in the field to improve high data rate transmission at low cost to as many as users with high reliability, large bandwidth, and with great flexibility for varying traffic condition. In order to meet these requirements within limited spectrum various multi carrier modulation techniques were employed. The most widely adopted multi carrier technique that is presently the main core of wireless application is the Orthogonal Frequency Division Multiplexing (OFDM). The technique employs orthogonal overlapped sub-carriers. OFDM provides the highest possible spectral efficiency for an orthogonal system. But the ever growing demand for spectral savings has led to the growth of the Spectrally Efficient FDM Systems (SEFDM) [1]. SEFDM is a Multi Carrier Modulation (MCM) Technique that utilizes non orthogonal overlapped sub- carriers. Spectral savings is offered by this technique by placing the carriers close to each other and transmitting them at a rate faster than the Nyquist rate [2].

Loss of orthogonality makes the detection of the signal an overly complex problem. Maximum Likelihood (ML) SEFDM detector has demonstrated attractive BER performance. However, ML detection complexity increases exponentially with the increase in the system size. In addition, linear detection techniques such as Zero Forcing (ZF) and Minimum Mean Squared Error (MMSE) perform well only for small sized systems in high Signal to Noise Ratio (SNR) conditions. But they limit the size of the SEFDM system. Finally, Sphere Decoders (SD) is shown to achieve optimum performance at a much reduced but random complexity whose volatility depends on the noise and the system coefficient matrix properties.

When we move on to SEFDM systems from basic OFDM systems the main issue is the increasing complexity that arises due to increase in area and power consumption. Both these issues are dealt in this paper while adopting the Fixed Sphere Decoders (FSD) techniques [3]-[4] and the CORDIC algorithm [5]-[6].

The paper is organized as follows. Section II describes spectrally efficient FDM system. Section III describes SEFDM transmitter architecture. Section IV gives the proposed modified SEFDM architecture. Section V and VI gives the results and the conclusion.

### II. SEFDM SYSTEM

The SEFDM signal consists of a stream of SEFDM symbols each carrying a block of  $N$  complex input symbols, denoted by  $s = s_R + js_{IM}$ , transmitted within  $T$  seconds. Each of the  $N$  complex input symbols modulates one of the non-orthogonal and overlapping subcarriers, hence, giving the SEFDM signal  $x(t)$  as

$$x(t) = 1/\sqrt{T} \sum_{n=0}^{N-1} (s_{1,n} e^{j2\pi n k \alpha / T}) \times g(t) \quad (1)$$

Where  $\alpha$  denotes the bandwidth compression factor defined as

$$\alpha = \Delta f T, \alpha < 1 \quad (2)$$

For  $\Delta f$  denoting the frequency distance between the subcarriers,  $T$  is the SEFDM symbol duration,  $N$  is number of subcarriers and  $s_{1,n}$  denotes the symbol  $m$  modulated on the  $n$ th subcarrier in the  $l$ th SEFDM symbol.

A discrete model of the SEFDM system can be obtained by sampling the SEFDM frame with index zero from (2) at a rate  $N/T$ , where  $N \geq M$ , giving:

$$X(k) = 1/\sqrt{Q} \sum_{n=0}^{N-1} (s_n e^{j2\pi nka/Q}) \quad (3)$$

Where  $X[k]$  is the  $k$ th time sample of the SEFDM symbol in equation (1),  $k = 0, 1, \dots, Q - 1$ ,  $Q = \rho N$ ,  $\rho$  is an oversampling factor and the factor  $1/\sqrt{Q}$  is a normalization constant.

The SEFDM signal can be realized with a single IDFT block, with a length longer than  $N$ . The SEFDM transmitter in this case is depicted in Fig. 1. Furthermore, it is shown in that by expressing the term as a rational number, that is by taking  $\alpha=b/c$ , where both  $b$  and  $c$  are integers and  $b < c$ , the SEFDM signal can be expressed as

$$X(k) = 1/\sqrt{N} \sum_{n=0}^{cN-1} (s'_n e^{j2\pi nkb/cN}) \quad (4)$$

As for the case above, here we define  $S'$  as

$$|S'| = \begin{cases} S_i b & , i \in I \\ 0, & \text{otherwise} \end{cases} \quad (5)$$

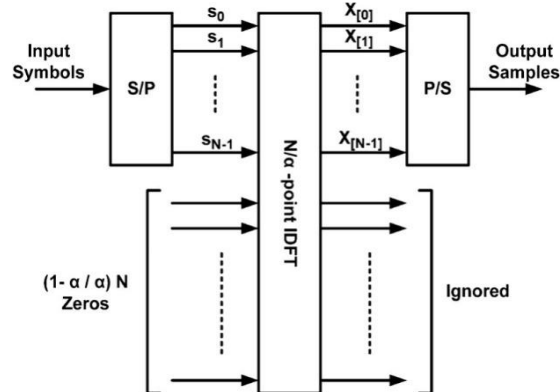


Fig. 1 SEFDM conceptual block diagram.

The samples of the SEFDM signal can be generated using  $c$  IDFT operations each of length of  $N$  points. The input symbols are padded with  $(c-1)N$  zeros and then arranged as a  $c \times N$  matrix in column major order. An IDFT operation is then performed on each row. The signal is finally composed by combining rotated versions of the IDFT outputs as depicted in Fig. 2.

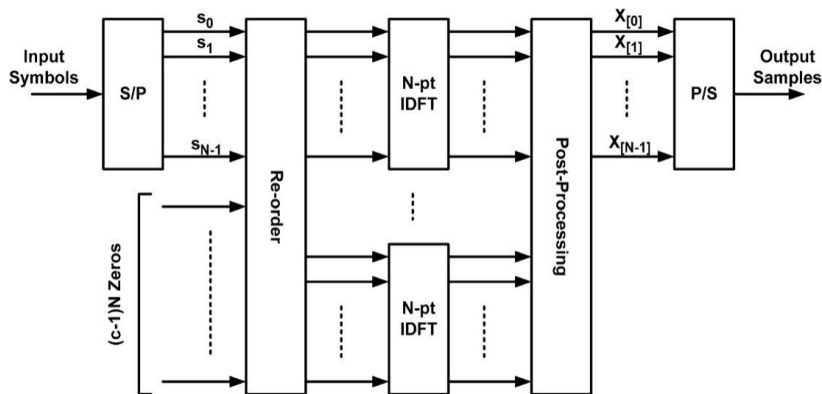


Fig. 2 SEFDM IDFT Based Transmitter

### III. SEFDM TRANSMITTER ARCHITECTURE

The generation of the SEFDM signal is realized by modulating the incoming input stream through a bank of modulators running at the different subcarriers frequencies. With the increase in the number of subcarriers it becomes exceptionally complex to realize this bank of modulators. In addition, the system will be susceptible to higher frequency offsets and timing errors, as the number of oscillators increases. Thus we generate SEFDM signals using the Fourier Transform. The proposed framework eliminates the need for a bank of analogue modulators to generate the SEFDM signal, therefore allowing for the digital implementation of the SEFDM transmitter.

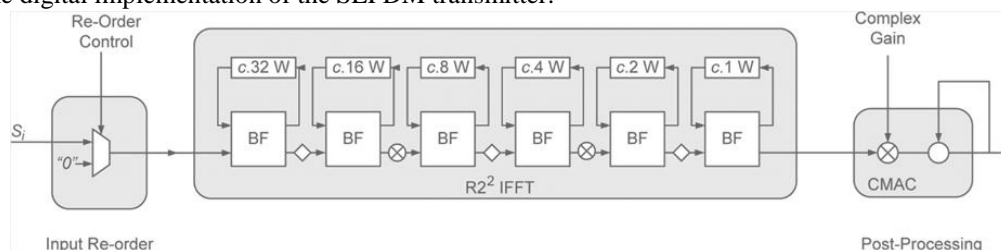


Fig.3 Multistream SEFDM transmitter architecture

**A. Zero Insertion and Reorder:**

Fig. 4 illustrates the general symbol reordering operation, which consists of padding the input symbols with (c-1) N zeros before arranging them as a c X N matrix in column major order. A naive implementation of this operation implies a buffer of complex words to hold the sparse complex matrix. The multi-stream IFFT accepts alternately interleaved samples from a number of input streams on successive cycles, such that transformed output samples appear at the output, as opposed to transforming the whole symbol at once. With a multi-stream IFFT, the symbol reorder block is only required to generate a single complex sample per cycle and therefore reduces to a single multiplexer, presuming the modulated sub- carrier symbols are suitably arranged in a preceding buffer.

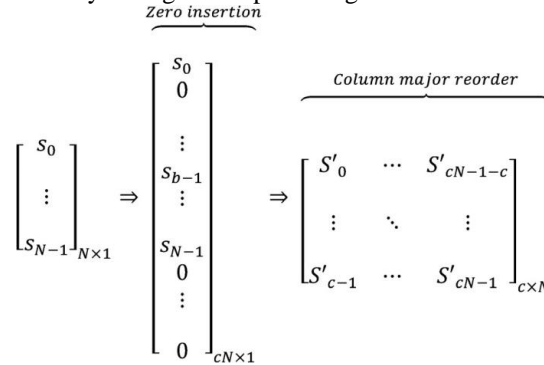


Fig. 4 General operation of symbol reordering

**B. Multi-stream IFFTs:**

The -point IDFTs are implemented in this section as cN-point IFFTs, which can be implemented as N multi-stream IFFT blocks. Multi-stream offers reduced circuit area and power consumption. The 64-point, 16-bit complex IFFT blocks-based on the radix- flow graph is used. The IFFTs have an enable signal which when de-asserted gates the internal clock and clears the output registers to zero. The multi-stream IFFT accepts alternately interleaved samples from a number of input streams on successive cycles, such that transformed output samples appear at the output, as opposed to transforming the whole symbol at once.

**C. Post-processing:**

The post processing operation combines the multi-stream IFFT outputs after multiplication with a complex exponential in order to produce the discrete-time output sample. The complexity of the post processing is a linear function of c, where we require (c-1) complex multiply accumulate (CMAC) operations. The hardware required includes the CMACs and LUTs to store pre-calculated rotation coefficients in read-only memory (ROM).

**IV. MODIFIED SEFDM ARCHITECTURE**

For low throughput systems, it is also possible to replace the CMAC with the CORDIC algorithm to reduce further circuit area and power dissipation. The proposed circuit modification is as shown in Fig 5.

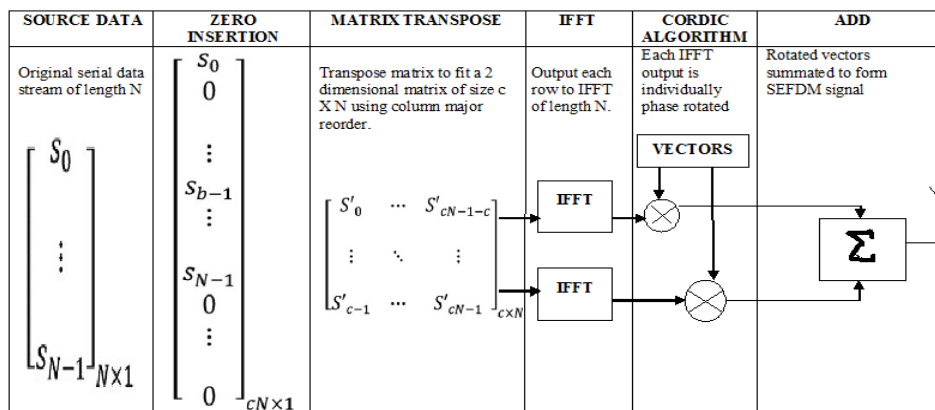


Fig.5 Modified Multi stream SEFDM transmitter architecture concept

As per methodology, the outputs of the IFFT blocks should be phase rotated with some values and their outputs are added up to produce our final desired SEFDM signal. In the above proposed system, the outputs of the IFFT blocks are phased rotated using the predetermined values that are stored in the RAM. The outputs of the vectoring blocks are added up to produce the SEFDM signals. The disadvantages of this system are that RAM occupies more space and the vectoring can't be done with different values to obtain different types of output SEFDM signals. Also, all the values in RAM should be changed every time with new values to produce different values of vectoring and on the output. In the modified system, which is illustrated in the Fig 6 the RAM has been replaced by the CORDIC algorithm implementation block.

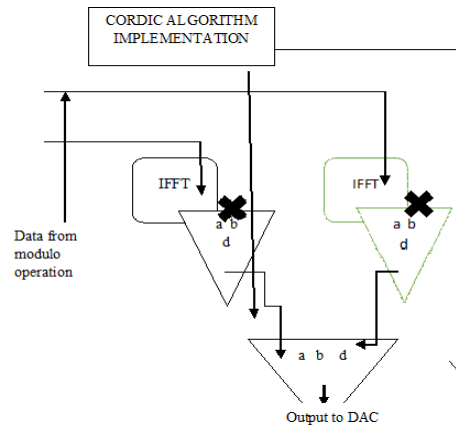


Fig.6 Block diagram of the proposed flexible CORDIC SEFDM transmitter

This will help us to produce different values for vectoring very easily just by changing the angle of rotation. This further implies that different values for vectoring can produce different phase rotated SEFDM signals. We need not have to change the values quite often as in case of the existing system. The advantage of using CORDIC algorithm is that just by changing the value of rotating angles different values of real and imaginary values are generated that can be given as the input of multipliers that perform the vectoring of IFFT outputs. Finally, these signals are added up then to produce the final output of SEFDM signal.

### V. RESULT

The proposed architecture was described with hardware description language VHDL as fixed-point arithmetic and synthesized with XST tool in Xilinx ISE FPGA chip and simulated using ISE Design Suite 14.2. Fig.7 shows the simulation results for the SEFDM architecture and Fig.8 shows the simulation results for the proposed SEFDM architecture. The synthesis tool has allocated the following resources as shown in Fig.9 and Fig.10.

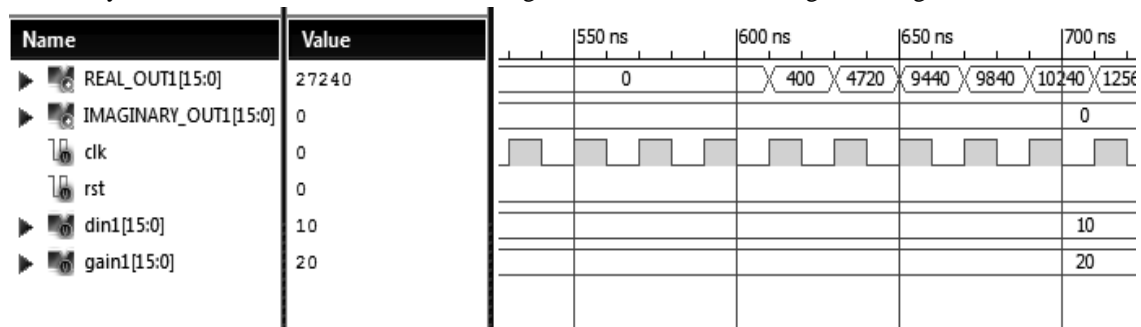


Fig.7 Simulation window of Multi stream SEFDM transmitter system

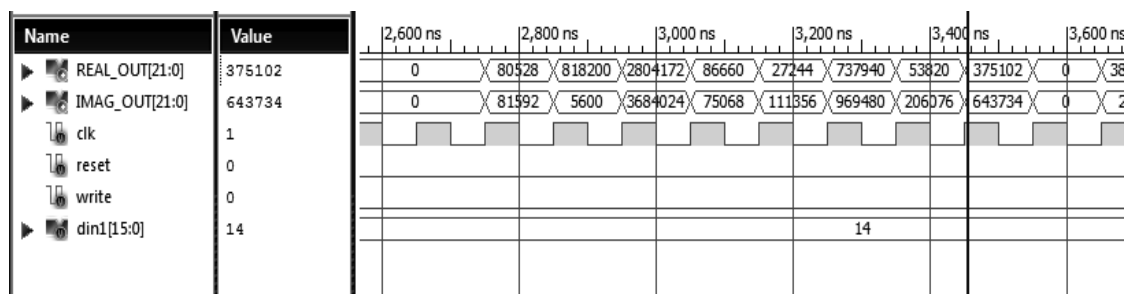


Fig.8 Simulation window of Modified Multi stream SEFDM transmitter system

Device Utilization Summary (estimated values)				[ - ]
Logic Utilization	Used	Available	Utilization	
Number of Slice Registers	266	54576	0%	
Number of Slice LUTs	641	27288	2%	
Number of fully used LUT-FF pairs	245	662	37%	
Number of bonded IOBs	35	218	16%	
Number of BUFG/BUFGCTRLs	2	16	12%	

Fig.9 Device utilization summary of Multi stream SEFDM transmitter

Device Utilization Summary (estimated values)			[1]
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	216	54576	0%
Number of Slice LUTs	2902	27288	10%
Number of fully used LUT-FF pairs	210	2908	7%
Number of bonded IOBs	25	218	11%
Number of BUFG/BUFGCTRLs	2	16	12%
Number of DSP48A1s	2	58	3%

Fig.10 Device utilization summary of Modified Multi stream SEFDM transmitter

## VI. CONCLUSIONS

This dissertation work has been carried out to implement SEFDM transmitter on FPGA. The SEFDM transmitter was implemented and tested on Spartan 3-XC3S400 board and its simulation results are discussed. The project focuses on algorithm which employs multiple IFFTs, for reasons of low complexity and general suitability to hardware implementation and applies the concept of multi-stream IFFT to realize the multiple transforms at minimal circuit area overhead. Then by proposing the CORDIC algorithm to replace the CMAC unit further reduction in circuit area was obtained.

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