Fault Detection at Minimization of Multiple Output Function of Reed-Muller Canonical form in Logical Networks

Sharad Pratap Singh	**Dr. B. B. Sagar**
Assistant Professor,	Assistant Professor,
Department of ECE,	Department of CSE,
Vira College of Engineering	Birla Institute of Technology,
Bijnor, India	Mesra-Ranchi (Noida Campus), India

Abstract- *The paper presents the structure of reed –Muller and generalized Reed-Muller transform metrics is discuss. Easily testable design techniques offer an attractive method by simplification of the test procedure as well as test data compression and hence they are in variably use in hence digital system reliability by incorporating fault tolerant/fail safe features. The detection of fault is an important prime consideration in development of testing schemes and it has significant impact on the requirements of building/self test hardware overhead and computational complexities as well as testing time. Therefore, the selections of fault detection technique become critical for complex circuits/systems particularly in situations where the fault in multiple output functions to be detected simultaneously.*

Keywords: Fault Detection, Reed-Muller Canonical (RMC), Polarity, System Reliability.

I. INTRODUCTION
Digital systems are becoming increasingly complex and sophisticated development in LSI/VLSI technology which has allowed not only higher package density but also made ,it feasible to implement additional peripheral support devices that were earlier interconnected externally .in addition it permitted on-chip in corporation of novel advanced features such as self testing , supervisory and fail-safe etc. and hence simplified the task of design and maintenance of complex systems by reducing external interconnecting lines as also thought improved reliability. Many digital hardware building blocks such as Encoders/ Decoders, ROM / Demux, ROMs, PLAs and ASICs are frequently use to generate multiple output combinational function to implement digital systems intended for various application areas such as DSP, Automation , Control and computer systems etc.

II. SYNTHESIS OF MULTIPLE OUTPUT SYSTEMS
The synthesis of multiple output function are based on the all types of common terms among the R.M.N. polynomials of the output functions, the number of common terms increases the number of EX-OR gates saved also increases. Here P[f] method has been used to compute to RM coefficient as requires fewer computations and gives batter performance then efficient algorithm.

III. METHOD FOR FAULT DETECTION:
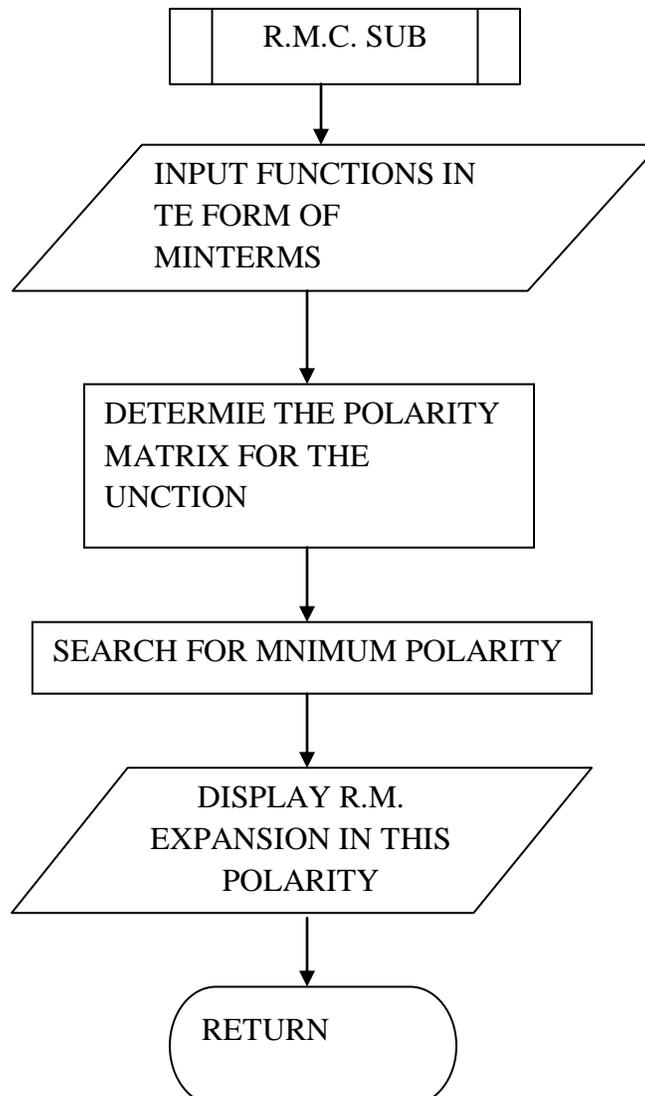Most commonly four methods are for used
1. Fault table method,
2. Boolean difference method
3. Path sensitization method and
4. D-algorithm

IV. FLOW CHART FOR MINIMIZATION OF MULTIPLE OUTPUT FUNCTIONS
The advantage of this representation is the fact that the resulting circuit needs at most n inputs in contrast to up to 2n inputs in other cases. The second essential advantage is the fact that for each function represented in RMC form there exists circuit, which can be tested with maximum $3n + 4$ tests, most of them independent of the realized function [2]. It is easy to see that for a Boolean function with n variables there exist 2" different RMC forms. Each of these forms can be characterized by 2" Boolean values a, indicating the presence or the absence of a given product term.
The aim is now to find the RMC form with the least number of a, = 1. Algorithms existing up to now build up a 2" x 2" matrix, called polarity-matrix [7], where every coefficient a, of each of the 2" polarities is given. This polarity-matrix is constructed using matrix multiplication [3], which means that these algorithms
 5 FLOW CHART FOR R.M.C. NETWORK SUBROUTINE

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                      ┌──────────────────┐
                      │   R.M.C. SUB     │
                      └──────────────────┘
                              │
                              ▼
                  ╱───────────────────────╲
                 ╱  INPUT FUNCTIONS IN      ╲
                ╱   TE FORM OF               ╲
               ╱    MINTERMS                  ╲
              ╲───────────────────────────────╱
                              │
                              ▼
                  ┌───────────────────────┐
                  │ DETERMIE THE POLARITY │
                  │ MATRIX FOR THE        │
                  │ UNCTION               │
                  └───────────────────────┘
                              │
                              ▼
                  ┌───────────────────────┐
                  │ SEARCH FOR MNIMUM POLARITY │
                  └───────────────────────┘
                              │
                              ▼
                  ╱───────────────────────╲
                 ╱  DISPLAY R.M.            ╲
                ╱   EXPANSION IN THIS        ╲
               ╲    POLARITY                  ╱
                ╲───────────────────────────╱
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                      ╭──────────────────╮
                      │    RETURN        │
                      ╰──────────────────╯
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Definition: Let T n be a 2n x2n

Considered Functions and Fault Types:

The program for synthesis of multiple output functions is highly flexible and can be used to synthesize the combinational circuit having large no. of input and output variables.

Although the simulation study has been carried out by considering three output functions each having three input variables, but can be extended for more number of output functions having large no of input variables, and for different functions having different no. of input variables by slightly modifying the developed program.

The testing program can be used to test any multiple input and multiple output combinational circuits. Although the simulation study has been carried out by considering Different circuits having a maximum of five input lines and three output functions. For RMC form of circuits, multiple inputs single output circuits are considered.

The types of faults that have been simulated and tested on different circuits are single as well as multiple stuck at faults and / or single bridging fault. Matrix multiplication [3], which means that these algorithms belong to the class with complexity $AT2 = O (16'') [I 3]$ binary matrix. T n will recursively be defined as.

$$Tn = \begin{bmatrix} t^{n-1} & 0 \\ t^{n-1} & t^{n-1} \end{bmatrix} \quad \text{And To= [l]}$$

It becomes apparent that the same matrix can be obtained by the nth Kronecker-power [12] of T'.

Definition:

Consider a Boolean function f given as

$\quad\quad [f] = [f', f'']$

Where, $\quad [f'] = [f0 ,……,f 2^{n-1}-1]$

And, $[f''] = [f\,2^{n-1}, \ldots, f\,2^{n-1}]$

Then $2^n \times 2^n$ matrix B[f] is define as $[F] = \begin{bmatrix} B[F'] & B[F''] \\ B[F''] & B[F'] \end{bmatrix}$ Let z^n be the nth kronecker power of $Z' = \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix}$

Then m[f] =B[f].2 z^n

P is an automorphism, because

P[f'] / P[f''] = P[f' / f''] = P[f'']

P is defined as above, then P[f]=m[f]

$$\begin{bmatrix} P[0\,0\,1\,0] & P[1\,1\,1\,1] \\ P[1\,1\,0\,1] & P[1\,1\,1\,1] \end{bmatrix} = \begin{bmatrix} P[00] & P[10] & P[11] & P[00] \\ P[10] & P[10] & P[11] & P[00] \\ P[11] & P[10] & P[11] & P[00] \\ P[01] & P[10] & P[11] & P[00] \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 \\ 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 1 & 1 & 0 & 0 & 0 \end{bmatrix}$$

That computation of the coefficients of the RMC forms off for a given polarity is possible without constructing the whole matrix P. This can be advantageous in cases of lack of storage The 3-output
 Polynomials with polarity (000) are as follows:

f0 = X1 $\oplus$ XOX1 $\oplus$ X2 $\oplus$ X0X1X2X3

f1 = X1 $\oplus$ XOX1 $\oplus$ X2 $\oplus$ X0X1 $\oplus$ XOX2X3

f2 = 1 $\oplus$ X0 $\oplus$ X0X2 $\oplus$ X0X2 $\oplus$ XOX1X3

 P[f]=P[0 0 1 0 1 1 0 1]

TABLE-1 The number of Ex-OR gates for the example

Inputs			Outputs		
X2	X1	X0	f1	F2	f0
0	0	0	1	0	0
0	0	1	0	0	0
0	1	0	1	1	1
0	1	1	0	0	0
1	0	0	1	0	1
1	0	1	1	1	1
1	1	0	1	1	0
1	1	1	0	0	0

The advantage of this representation is that resulting circuit need only small and input in contrast 2n inputs in other case. If a function is represented in R.M.C. form, there adjust a circuit which can be tested with(n+4) test for single fault and most of test are independent of the realized function. due to these advantages the second form of R.M. expansion

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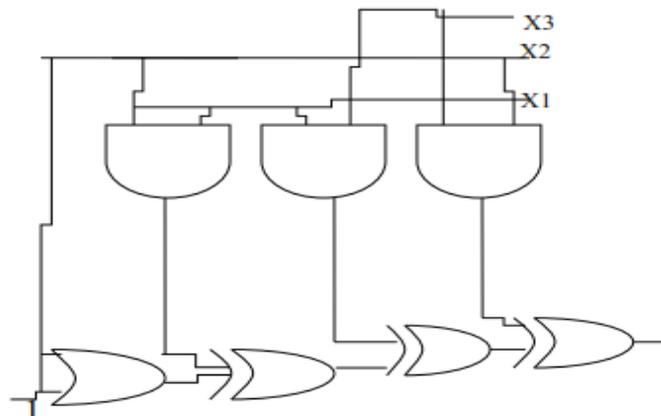
$$T1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix}$$

In addition, the test st T1 will also detect:
1.   Any stuck –at -0 fault on the input or output of an AND gate (test 0111,1111)
2.   Any stuck- at -1 fault on the output of an AND gate (tests 0000,1000)However, an stuck –at -1 fault on the AND gate inputs must be detected separately using the test set

$$T2 = \begin{bmatrix} d & 0 & 1 & 1 \\ d & 1 & 0 & 1 \\ d & 1 & 1 & 0 \end{bmatrix}$$

Where "d" is a don't care condition. Thus for n-variable function T2 will contain n test & the full test set will consists of T=T1+T2=(n+4) tests. This result was extended by Saluja and Reddy to detect multiple stuck- at faults. In an n- variable R.M. Canonical network, to detect "t" faults (t≥1), the number outset required will be

$$4 + \sum_{i=1}^{\lfloor Log_2 2t \rfloor} \begin{bmatrix} n \\ i \end{bmatrix}$$

But these are function specific thereby reducing the attractiveness of RMC networks. The tests sets discussed above are applicable only for R.M. Canonical networks. R.M. transform can also effectively be used for fault detection in an arbitrary combinational network

Synthesis of Multiple Output Functions
     Synthesis of multiple output functions. The program developed is very flexible and user interactive. Here P(f) matrix has been generated using some of it's properties instead of previously.
(i)The 0th column elements are the same as the
(ii)The 1st column elements a_{i1} are generated as

$a_{i1} = a_{i+1\,1} = a_{i0} \oplus a_{i+1\,0}$
     Where $i = 0,2,4,\ldots,2^n - 1$ and n is the no. of input variables
(iii)The second column elements will be given by

$a_{ij} = a_{i+2\,j} = a_{i\,j-2} \oplus a_{1+2\,j-2}$
     Where $i = 0,1,2 \ldots, 2^n - 1$ and $j = 2$
(iv)Similarly the 3rd column elements can be given as

$a_{ij} = a_{i+2} = a_{i\,j-2} \oplus a_{i+2\,j-2}$
Where $i = 0,1,2.\text{---------},2n -1$ and $j = 3$
                    $j = 4,5,6,7$
(vi) If we divide P[f] matrix into four quadrant. _____ nd that 1st quadrant is same as the 4th quadrant. Therefore generation of P[f] matrix using above properties leads to less number of iterations.
     After development of polarity matrices, the number of EX-OR gates required by each function for every polarity has been calculated without considering the effect common terms. The m-common matrix ws generated by taking the bit-wise logical AND among the P[f] matrices of all the functions and no. of m-common gates saved for each polarity has been calculated. To find the other combinations of common matrices, the reminder matrixes and residue matrixes were generated and no. of gates saved by all types of common function has been calculated. At last, the computation of number of EX-OR gates required to realize the circuit for every polarity has been carried out based on that optimum polarity was determined.

V.   SOFTWARE DEVLOPMENT

     The entire simulation study has been carried out on a 486 PC-AT platform in Turbo C environment. The software developed for synthesis of multiple/single output combinational circuits and simulation of stuck-at and bridging faults in either of the cases and then testing is performed. The program for synthesis and testing has been developed separately. After development of polarity matrices, the number of EX-OR gates required by each function for every polarity has been calculated without considering the effect common terms. The m-common matrix ws generated by taking the bit-wise logical AND among the P[f] matrices of all the functions and no. of m-common gates saved for each polarity has been calculated. To find the other combinations of common matrices, the reminder matrixes and residue matrixes were generated and no. of gates saved by all types of common function has been calculated. At last, the computation of number of EX-OR gates required to realize the circuit for every polarity has been carried out based on that optimum polarity was determined., the subroutine first asks the user to input min terms of the functions to be synthesized. After this it constructs the polarity matrix using p(f) matrix method to generate the compete 2^n sets of R.M. coefficients. Then the subroutine searches for the row having minimum number of ones as to have minimum number of terms in the R.M.C. expansion and hence resulting in minimal hardware. After determining this optimal polarity, the program displays the R.M.C. expansion of the function using optimal polarity and returns to the main program.

VI. CONCLUDING REMARKS

a new method for the polarity matrix which is used for minimization of RMC forms of Boolean function is presented. It can be used for fully specified and incomplete specified functions. In place of R. M. spectral coefficients techniques of fault detection, a morefaster technique can be proposed to reduce further test sets and hardware overhead P[f] matrix may be generated with further less no. of iterations, by modifying generation process of it.

The entire simulation study has been carried out on a 486 PC-AT platform in Turbo C environment. The program for synthesis and testing has been developed separately. After development of polarity matrices, the number of EX-OR gates required by each function for every polarity has been calculated without considering the effect common term

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About Authors

SP Singh received his B. Tech. Degree in Electronics & Communication Engg. In 2005 from CSJM University and M. Tech. Degree in Digital Communication in 2010 from BIET Jhansi, he is GATE Qualified in 2006 and goat a scholarship from HRD Delhi. Presently he is working as a Assistant professor department of ECE, in Vira college of Engineering, bijnor, UP. He is member of ISTE New Delhi.

Dr. B. B. Sagar received his MCA degree in 2004 from UPTU and Awarded Ph. D in Computer Science and Communication in 2011 from SHIATS Allahabad, U.P., India. Dr. Sagar is a well-known reviewer and editorial board member of various international journal of repute. His area of interest is software reliability, digital communication and network reliability. He is also member of IETE. Presently he is working as an Assistant Professor in Birla Institute of Technology, Mesra - Ranchi (Noida Campus)