Volume 3, Issue 8, August 2013 ISSN: 2277 128X

International Journal of Advanced Research in Computer Science and Software Engineering

Research Paper

Available online at: www.ijarcsse.com

Common NBLV SRAM Assist Circuits in Nano-CMOS Technology

Pardeep Bansal
ECE Deptt, HCTM Kaithal
India

Sandeep Dhariwal
ECE Deptt, HCTM Kaithal
India

Pawan Kumar
ECE Deptt, RPIIT (Karnal)
India

Abstract— As the technology is moving towards the lower Nano regimes, due to scaling the read and write margins in SRAM are decreasing sharply and may lead to operation failure. So it becomes mandatory to use SRAM Assist circuits in these regimes. In this paper new NBLV assist circuits are presented which gives better margins as compared to conventional SRAM Assist circuits. The proposed circuit utilizes the merit of negative bit line voltage and negative Vss techniques for write and read assistance respectively. This circuit is designed in 250nm CMOS technology. Increased write and read margins makes these circuits more robust, stable and fast.

Keywords— CMOS, NBLV, Write margins and Read margins, Process Variation, Readability

1 INTRODUCTION

One of the key features that led to the success of complementary metal-oxide semiconductor (CMOS) technology was its intrinsic low-power consumption. Reduction of power consumption makes a device more reliable. The need for devices that consume a minimum amount of power was a major driving force behind the development of CMOS technologies. As a result, CMOS devices are best known for low power consumption. Another interesting feature of CMOS technology is its nice scaling properties, which has permitted a steady decrease in the feature size allowing for more and more complex systems on a single chip, working at higher clock frequencies. Moore's law predicts that the number of transistors that can be placed on an integrated circuit is doubled approximately every two years. In parallel, the need for bit counts in an embedded Static Random Access Memory (SRAM) has been growing exponentially. Thus, the probability of a defect in an embedded SRAM cell is constantly increasing. In addition, as the process technology continues to scale, the stability of an embedded SRAM cell is not only a major design consideration, but also a concern for testing as well. SRAM cell's designers encounter many challenges as technology scales. First of all, it has become increasingly complicated to maintain an acceptable Static Noise Margin (SNM) in a SRAM cell while scaling the minimum size and supply voltage. Secondly, it has been observed that there are many variability problems at a transistor level in the SRAM bit-cell. For example, as the Operating Voltage (VDD) is reduced, it causes Read/Write/ Access or Data retention failures. In addition there are other failures relating to variability in the SRAM cell's Sense Amplifier circuitry. Thirdly, tightly packaged chip areas can be especially susceptible and sensitive to manufacturing defects and process variations. Process variation is one of the main reasons which lead the SRAM to operation failure. So in Nanometres (nm) regimes it becomes necessary to use SRAM Assist circuits. The static RAMs hold the stored value in the flip flop circuits as long as the power is on The core storage element used for most register file and cache designs on high performance microprocessors is a six-transistor CMOS cell with a single word-line and both true and complementary bit-lines. Figure 1 shows the circuit diagram of a 6T pair of cross-coupled inverters and an access transistor for each bitline as combination read/write port. True and complementary versions of the data are stored on the cross-coupled inverters. If the data is disturbed slightly, positive feedback around the loop will restore it to VDD or GND.

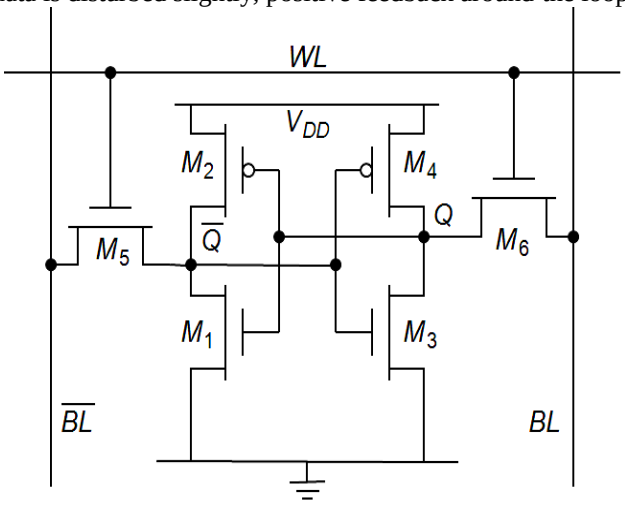

Figure 1 Six-transistor SRAM cell

The word line is inserted to read or to write the cell. The six transistor (6T) static memory cell in CMOS technology is used in majority of the designs, today. The cross-coupled inverters, M1 M2, M3 and M4 act as the storage element. Major design effort is directed at minimizing the cell area and power consumption so that millions of cells can be placed on a chip. If initially the value of node Q is high, for a correct read operation it should not change and should flip for a correct write operation when data applied at bitlines is opposite of initial state. As the scaling is done there is not a corresponding decrease in process variation, hence in deep sub–micron regions there is chances of read and write failure. So in these regimes it becomes mandatory to Use the SRAM assist circuits.

2. CONVENTIONAL NBLV SRAM ASSIST CIRCUIT

This scheme is as shown in Fig.2. It consists of a negative voltage generator and control circuit. IO driver section and the associated waveforms at the various nodes in the NBLV generator are shown in Fig.2. It consists of a capacitive-coupling-based negative voltage generator and IO write driver circuitry. As shown in Fig.2, the write control circuitry consists of two sets of write drivers (MNL1, MNR1) and (MNL2, MNR2). Whenever write enable (WE) signal goes high. Depending on the status of write data (DIN), one of the first set of write drivers, MNL1 or MNR1, becomes on and pulls the corresponding bit-line to low. When one of the bit-lines goes low, it disables the first set of write drivers and enables the second set of write drivers (MNL2, MNR2) which finally takes the bit-line to negative voltage VKK ($\simeq$ -150 mV). So, the bit-lines go to negative in two steps, first goes to 0 and then negative as in [27]. This circuit does not interfere in the read operation, as column mux isolates the read and write path. As shown in Fig.2, there is no loading effect on bit-lines (BL and BLB) or sense amplifier internal nodes (SAL and SAR), because of the additional circuitry. So, there is no loss in read performance. When the bit-line goes to a lower voltage during read operation (VDD -100 mV typically), there cannot be any glitch on the input of second set of write driver as this is gated by write signal. Also the negative voltage on line NBLV is generated when WE signal goes high, so write operation is fast. The negative voltage generator along with waveforms is shown in Fig. 2. When WE signal is low, WEB1 signal is high, so NBLV line is pre-discharged to vss. When WE signal goes high, the coupling capacitor couples the NBLV line to negative voltage, VKK and WEB1 signal also goes to VKK [28].

3. PROPOSED COMMON SRAM ASSIST CIRCUIT

We have studied Process variations aware area efficient negative bitline scheme in last section which is found very effective technique among all write assist techniques [28] and similarly for read operations negative Vss technique is found very effective technique. The negative points of these techniques are that they are separately used for read and write problems. In the case of write operations scheme [28] doesn't provide any positive assistance during read operation. Similarly negative Vss technique provides assistance for read operations only. If in the same SRAM cell we use two different circuits for read and write assistance then it will increase the area overhead by a large amount. So in this paper, a common assist circuit [29] is presented. As shown in fig 3, it can provide the assistance during both, read and write operations. In this design we have combined above mentioned two techniques using common circuit. The conventional circuitry presented in scheme [28] works only during write operation. In this scheme [29] we have added a NMOS transistor with a read signal applied at the gate terminal so that, during read cycle negative voltage can be applied at drain end of pull down transistor. While in the case of write operation Vss will be applied at this point through another NMOS transistor where a complement of read signal is applied at the gate of this transistor, so that it can connect the Vss='0' only during the write operations. Also a NOR gate in series with a NOT gate is connected at the input of negative voltage generator.

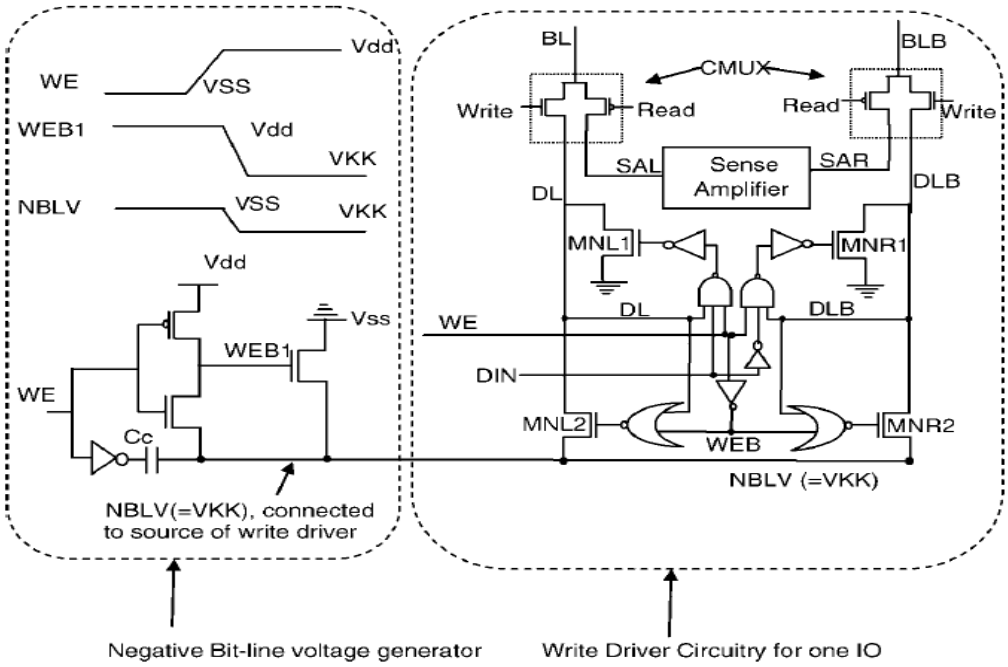

Fig. 2 Process variations aware area efficient negative bit line scheme [28]

So that negative voltage can be generated in both read and write cycles. . The working in write cycle will be almost same as that of scheme [28] but there are slight changes, here in this scheme Vss is not connected directly in fact it is provided through a NMOS transistor which is gated by read (RE) signal through a NOT gate, otherwise the write cycle working and performance in scheme [29] is same that of scheme [28]. In the case of read operation when read enable signal (RE) goes high it will turn on the NMOS transistor connected between NBLV node and Vss point of the SRAM cell and hence a negative voltage will get applied at the drain terminals of the pull down transistors instead of Vss ='0' during the read cycle and hence improving the readability. But in the case of write operation Vss ='0' is required at this point so we have connected a logic circuit here at this point. A read enable signal after passing through a NOT gate is applied at the gate of a NMOS transistor whose drain is connected at Vss, So during the write operation when read enable signal goes high it will connect the Vss at this point. We have made some changes in the negative voltage generator circuit as well, because now negative voltage requires to be generated in both read and write cases. So we connected a combination of NOR gate and NOT gate which will give the input to negative voltage generator and hence generating negative voltage in both, the read and write cases. A negative voltage at pull down transistor's drain terminal will make it more conductive and hence improving readability. As shown in the fig.4 without proposed scheme although the read operation is successful but the read margins are low. As shown in fig.5 with scheme [29] read margin will improve because a negative voltage instead of Vss='0' will make pull down transistors more conductive and hence improving the read margins.

Without this scheme [29] the read margins are same throughout the read cycle. The value of RT node is 2.99V and that of node RB is 650 mv and hence giving a read margin of 2.340 mv, while with this proposed scheme, in starting of read cycle the read margin is 2.818V in the middle of read cycle it is 2.580V while towards the end of read cycle it is 2.50V hence giving an improvement of 478mv, 240mv and 160mv in read margins respectively. As shown in fig 6 the results are always positive, in the case of scheme [29] read margins are changing during the whole read cycle because in the starting the negative voltage generated, pull down the RB easily but as time passes this negative voltage losses its effect as it starts to rise towards positive voltage because the voltage dumped on it and node RB again starts to rise hence lowering the read margin. But still the lowest margin during read cycle is 2.50V giving an improvement of 160mv as compared to scheme [28], which is a significant amount.

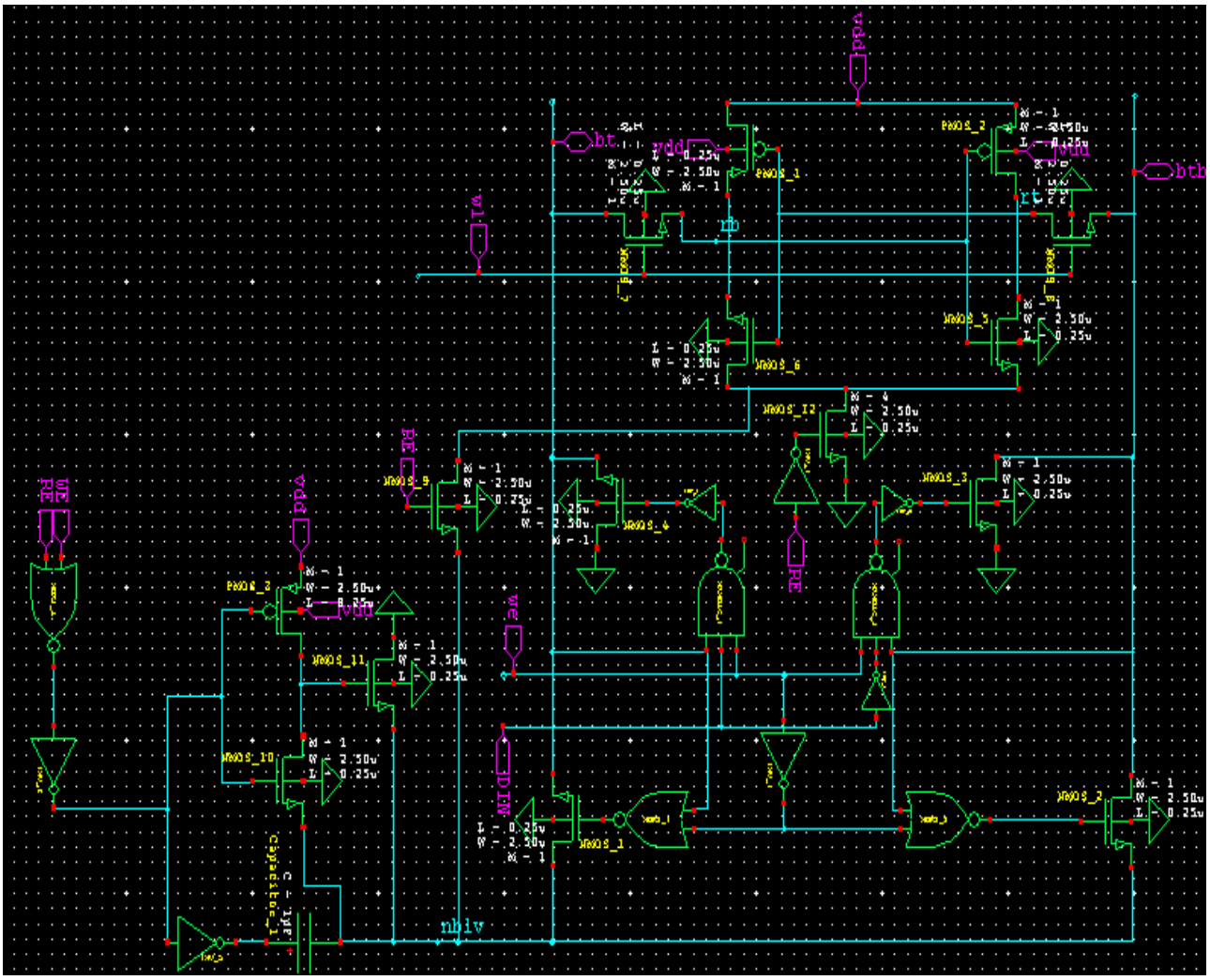

Fig 3 Schematic of the proposed common write and read assist circuit [29] in tanner tool

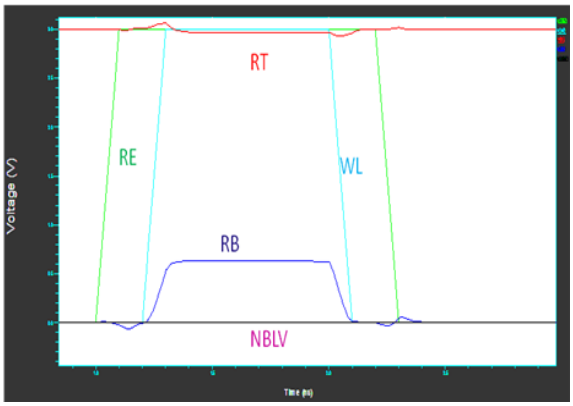

Fig 4 Successful read operation without proposed circuit [29]

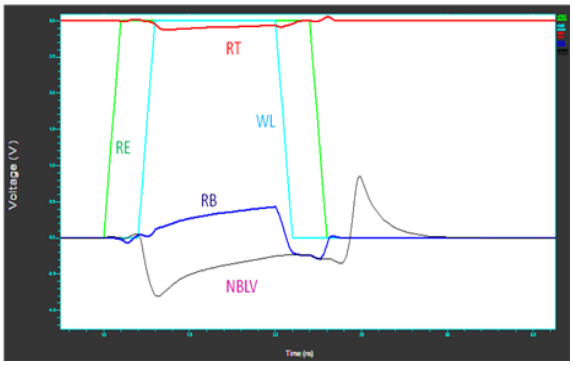

Fig 5 Successful read operation with proposed circuit [29]

Read margin comparison table of scheme [28] and scheme [29]

Time	Read margins (volts)	
(nanoseconds)	scheme [28]	scheme [29]
1.30 ns	2.34 V	2.818 V
1.65 ns	2.34 V	2.580 V
2.00 ns	2.34 V	2.500 V

4. COMPARISON GRAPH

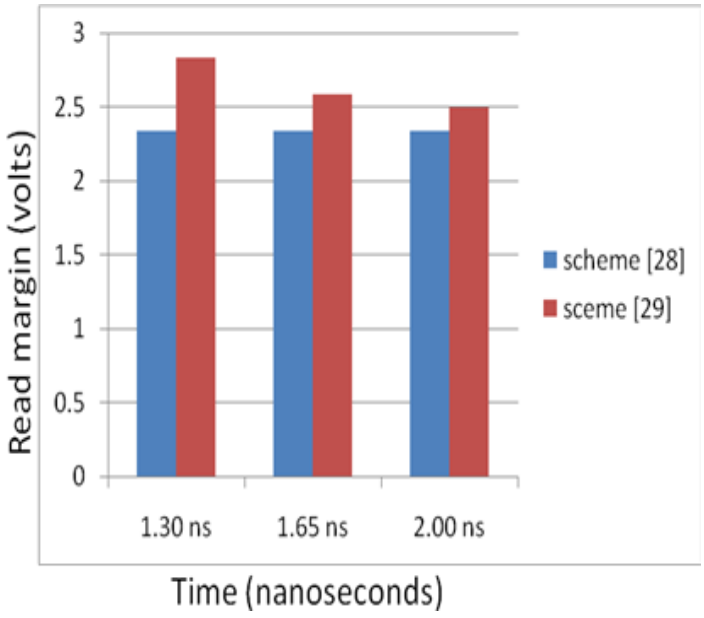

Fig 6 Comparison of read margins between scheme [28] and proposed scheme [29]

5. Conclusion

In present work new circuits in SRAM assist circuits is presented which shows improvement in read margins. Proposed common read and write assist circuit [29] gives read margin of 2.340V in comparison of conventional area efficient write assist technique [28] which has a read margin of 2.580V. So we have conclude that by using common write and read assist technique [29] we can improve the read margin by 240mv which is an improvement of 10.25% and it has been observed that with a small increment in Area, read margin has increased considerably.

Acknowledgment

The author acknowledges the ALVERT TECHNOLOGY, Kurukshetra, for the support given to carry out the research work.

References

1. Sung-Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits -Analysis and Design, 3rd ed., Tata McGraw Hill, New York, 2003
2. David A Hodges, Resve Saleh, Horace G. Jackson, Analysis and Design of Digital Integrated Circuits, 3rd ed., McGraw Hill Inc. 2005.
3. Vasudha Gupta and Mohab Anis, "Statistical Design of the 6T SRAM Bit Cell",@ IEEE, January 2010.
4. Chang, L., Fried, D.M., Hergenrother, J., et al.: 'Stable SRAM cell design for the 32 nm node and beyond' Symp VLSI Circuits Digital Technical Papers, June 2005, pp. 128–129
5. Nii, K., Tenoh, Y., Yoshizawa, T., et al.: 'A 90 nm low power 32 Kbyte embedded SRAM with gate leakage suppression circuit for mobile applications'. Symp. VLSI Circuits Digital Technical Papers, June 2003, pp. 247 - 250
6. Chirag Agrawal, Benjamin Chai, Abhinav Dubey, Greg Slovin, "Design and Layout of a 128-bit Static Random Access Memory" University of Florida
7. Sreerama Reddy G.M, P. Chandra-shekara Reddy, "Negative Word Line Scheme Based Low Power 8Kb SRAM for Stand Alone Devices", European Journal of Scientific Research ,ISSN 1450-216X Vol.26 No.2 (2009), pp.223-237
8. S O Toh, Z. Guo, T.-J K. Liu, and B. Nikoli´c, "Characterization of dynamic SRAM stability in 45 nm CMOS," IEEE J. Solid-State Circuits, vol. 46, no. 11, pp. 2702–2712, Nov. 2011.
9. Douseki, T., Shigematsu, S., Yamada, J., Harada, M., Inokawa, H., Tsuchiya, T.: 'A 0.5-V MTCMOS/SIMOX logic gate', IEEE J. Solid- State Circuits, 1997, 32, (10), pp. 1604–1609
10. Yamaoka, M., Shinozaki, Y., Maeda, N., et al.: 'A 300-MHz 25-A/Mb leakage on-chip SRAM module featuring process-variation immunity and low leakage-active mode for mobile-phone application processor', IEEE J. Solid-State Circuits, 2005, 40, (1), pp. 186–194
11. v. Sharma et.al., SRAM design for wireless sensor networks, analog circuits and signal processing DOI:10.1007/978-1-4614-4039-0-2 © Springer science+ business media new York 2013
12. Heller, L.G., Spampinato, D.P., Yao, Y.L.: 'High sensitivity charge-transfer sense amplifier', IEEE J. Solid-State Circuits, 1976, 11, (5), pp. 596–601
13. Yamaoka, M., Osada, K., Ishibashi, K.: '0.4-V logic-library-friendly SRAM array using rectangular-diffusion cell and delta-boosted array voltage scheme', IEEE J. Solid-State Circuits, 2004, 39, pp. 934–940
14. Shibata, N., Kiya, H., Kurita, S., Okamoto, H., Tan'no, M., Douseki, T.: 'A 0.5-V 25-MHz 1-mW 256-Kb MTCMOS/SOI SRAM for solar power-operated portable personal digital equipment – sure write operation by using step-down negatively overdriven bitline scheme', IEEE J. Solid-State Circuits, 2006, 41, p. 728
15. Mizuno, H., Nagano, T.: 'Driving source-line cell architecture for Sub-1- V high-speed low-power applications', IEEE J. Solid-State Circuits, 1996, 31, p. 552
16. Shibata, N., Douseki, T., Kurita, S.: 'Bitline-overdriven writing circuitry for ultralow-voltage MTCMOS SRAMs'. Proc. IEICE Electronics Society Conf., September 2003, vol. C-12–25, p. 100
17. Douseki, T., Shibata, N., Yamada, J.: 'A 0.5–1 V MTCMOS/SIMOX SRAM macro with multi-V memory cells'. Proc. IEEE Int. SOI Conf., October 2000, p. 24
18. hibata, N., Inokawa, H., Tokunaga, K., Ohta, S.: 'Megabit-class size configurable 250-MHz SRAM macro-cells with a squashed-memory cell architecture', IEICE Trans. Electron., 1999, E82-C, (1), pp. 94–104
19. Ishibashi, K., Takasugi, K., Yamanaka, T., Hashimoto, T., Sasaki, K.:'A 1-V TFT-load SRAM using a two-step word-voltage method', IEEE J. Solid-State Circuits, 1992, 27, (11), pp. 1519–1524
20. Mann, R.W., Wang, J., Nalam, a S., et al.: 'Impact of circuit assist methods on margin and performance in 6 T SRAM', Solid-State Electron., 2010, 54, pp. 1398–1407
21. Zhang, K., Bhattacharya, U., Chen, Z., et al.: 'A 3-GHz 70 Mb SRAM in 65 nm CMOS technology with integrated column-based dynamic power supply', ISSCC Dig. Tech. Papers, 2005, pp. 474–475
22. Shibata, N.: 'Current sense amplifiers for low-voltage memories', IEICE Trans. Electron., 1996, E79-C, (8), pp. 1120–1130
23. Chandra, V., Pietrzyk, C., Aitken, R.: 'On the efficacy of write-assist techniques in low voltage Nano-scale SRAMs', 978-3-9810801-6-2/DATE10 # 2010 EDAA

24. Shibata, N., Watanabe, M., Sato, Y., Ishihara, T., Komine, Y.: 'A 2-V 300-MHz 1-Mb current-sensed double-density SRAM for low-power CMOS/SIMOX ASICs', IEEE J. Solid-State Circuits, 2001, 36, (10), pp. 1524–1537
25. Shibata, N., Goto, Y., Date, S.: 'High-performance memory macro-cells with row and column sliceable architecture', IEICE Trans. Electron., 1993, E76-C, (11), pp. 1641–1648
26. Mukhopadhya, S., Rao, R.M., Kim, J.-J., Chuang, C.-T.: 'SRAM write-ability improvement with transient negative bit-line voltage', IEEE Trans. VLSI Syst., 2011, 1, pp. 24–32
27. Yamaoka, M., Osada, K., Ishibashi, K.: '0.4-V logic library friendly SRAM array using rectangular-diffusion cell and delta-boosted-array voltage scheme'. Symp. VLSI Circuits Digital Technical Papers, June 2002, pp. 170–173
28. A. Goel R.K. Sharma A.K. Gupta ; Process variations aware area efficient negative bit-line voltage scheme for improving write ability of SRAM in nanometer technologies; IET Circuits Devices Syst., 2012, Vol. 6, Iss. 1, pp. 45–51 45 doi: 10.1049/iet-cds.2011.0036

