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Novel Ultra Low Power Multi-threshold CMOS Technology

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Abstract*—A 1-V high-speed and low-power digital circuit technology with 0.5-pm multithreshold CMOS (MT-CMOS) is proposed. This technology applies both low-threshold voltage and high-threshold voltage MOSFETs in one LSI. Low-threshold voltage MOSFETs enhances speed performance at a supply voltage of 1 V or less. High-threshold voltage MOSFETs suppresses the stand-by leakage current during the sleep period. The technology has achieved logic gate characteristics of 1.7-ns propagation delay time and 0.3-pWIMHzIgate power dissipation. To demonstrate its effectiveness, a standard cell based PLL-LSI was designed as a carrying vehicle. An 18-MHz operation at 1 V was obtained using a 0.5-pm MT-CMOS process.

***Index Terms*—Ground bounce, leakage power, low power, multi threshold voltage.**

I. INTRODUCTION

Lowering the supply voltage is the most effective way to achieve low-power performance because power dissipation in digital CMOS circuits is approximately proportional to the square of the supply voltage. From the point of view of applications to battery-powered mobile equipment, the supply voltage should be set at 1 V [1]. I-V operation enables direct battery drive by a single Ni-Cd or Ni-H battery cell even taking the cell's discharge characteristic into account. This provides the smallest size and lightest weight equipment and eliminates the need for a power wasting de-to-de voltage converter.

However, it is generally rather difficult to reduce the supply voltage to 1 V. The drastic degradation in speed is the largest problem. Although several studies of high-speed 1-V operating DRAM's have been reported [3], [4], they seem difficult to apply to general logic circuits because they assume stand-by node voltages throughout the entire circuit are predictable in memory LSI's, and utilization of the conventional layout CAD tool is thought to be difficult. Therefore, the development of novel circuit technology that achieves high-speed operation at a low voltage of 1 V with only a single battery drive and can be easily applied to random logic circuits is the key to developing the LSI designs for mobile equipment in the multimedia era.

This paper proposes just such a new 1-V high-speed circuit technology that is applicable to all digital CMOS circuits [5]. We call it multithreshold-voltage CMOS (MTCMOS). Its unique feature is that it uses both high- and low-threshold voltage MOSFET's in a single chip. In the next section, key issues in low-voltage operation are discussed.

High-speed computation has thus become the expected norm from the average user, instead of being the province of the few with access to a powerful mainframe. Likewise, another significant change in the attitude of users is the desire to have access to this computation at any location, without the need to be physically tethered to a wired network. The requirement of portability thus places severe restrictions on size, weight, and power. Power is particularly important since conventional nickel cadmium battery technology only provides 20 W . h of energy for each pound of weight [I]. Improvements in battery technology are being made, but it is unlikely that

a dramatic solution to the power problem is forthcoming; it is projected that only a 30% improvement in battery performance will be obtained over the next five years [2]. Although the traditional mainstay of portable digital applications has been in low-power, low-throughput uses such as wristwatches and pocket calculators, there are an ever-increasing number of portable applications requiring low power and high throughput. For example, notebook and laptop computers, representing the fastest growing segment of the computer industry, are demanding the same computation capabilities as found in desktop ma- chines. Equally demanding are developments in personal communications services (PCS's), such as the current generation of digital cellular telephony networks which employ complex speech compression algorithms and so- phisticated radio modems in a pocket-sized device. Even more dramatic are the proposed future PCS applications, with universal portable multimedia access supporting full-motion digital video and control via speech recognition [3J. In these applications, not only will voice be trans- mitted via wireless inks, but data as well. This will facil- itate new services such as multimedia database access (video and audio in addition to text) and supercomputing for simulation and design, through an intelligent network which allows communication with these services or other people at any place and time. Power for video compres- sion and decompression and for speech recognition must be added to the portable unit to support these services- on top of

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the already lean power budget for the analog transceiver and speech encoding. Indeed, it is apparent that portability can no longer be associated with low throughput; instead, vastly increased capabilities, ac- tually in excess of that demanded of fixed workstations, must be placed in a low-power portable environment.

Even when power is available in nonportable applica- tions, the issue of low-power design is becoming critical. Up until now, this power consumption has not been of great concern, since large packages, cooling fins, and fans have been capable of dissipating the generated heat. How- ever, as the density and size of the chips and systems continue to increase, the difficulty in providing adequate cooling might either add significant cost to the system or provide a limit on the amount of functionality that can be provided.

II. CIRCUIT DESIGN AND TECHNOLOGY CONSIDERATIONS

There are three major sources of power dissipation in digital CMOS circuits, which are summarized in the following equation:

$$P_{\text{total}} = p_t\,(C_L \cdot V \cdot V_{dd} \cdot f_{\text{clk}}) + I_{sc} \cdot V_{dd} + I_{\text{leakage}} \cdot V_{dd}.$$

The first term represents the switching component of power, where C, is the loading capacitance, f c l k is the clock frequency, and *pt* is the probability that a power consuming transition occurs (the activity factor). In most cases, the voltage swing **I/** is the same as the supply voltage *Vdd;* however, in some logic circuits, such as in single- gate pass-transistor implementations, the voltage swing on some internal nodes may be slightly less.

The second term is due to the direct-path short circuit current which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground [9], [101. Finally, leakage current leakage, which can arise from substrate injection and sub threshold effects, is primarily determined by fabrication technology considerations (see Section IIIC). The dominant term in a "well-designed" circuit is the switching component, and low-power design thus becomes the task of minimizing while retaining the required functionality.

The power-delay product can be interpreted as the amount of energy expended in each switching event (or transition) and is thus particularly useful in comparing the power dissipation of various circuit styles. If it is assumed that only the switching component of the power dissipation is important, then it is given by transistor.

III. MTCMOS CIRCUIT TECHNOLOGY

A. Basic Circuit Scheme

The new MTCMOS circuit technology is proposed to satisfy both requirements of lowering the threshold voltage of a MOSFET and reducing stand-by current, both of which are necessary to obtain high-speed low-power performance at a *Vdd* of I V. This technology has two main features. One is that N-channel and P-channel MOSFET's with two different thresh- old voltages are employed in a single chip. The other one is two operational modes, "active" and "sleep," for efficient power management.

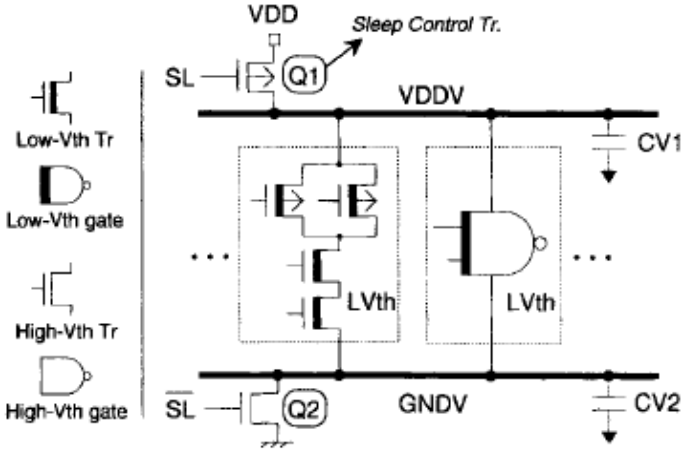

Fig. 3 shows the basic MTCMOS circuit.

The logic gate is composed of MOSFET's with a low threshold voltage of about 0.2-0.3 V. Its power terminals are not connected directly to the power supply lines VDD and GND, but rather to the "virtual" power supply lines VDDV and GNDV. The real and virtual power lines are linked by MOSFET's QI and Q2. These have a high threshold voltage of about 0.5-0.6 V and serve as sleep control transistors. Signals SL and *SL,* which are connected to the gates of QI and Q2, respectively, are used for active/sleep mode control. Circuit operation in each mode at a supply voltage of I V is described below.

In the active mode, when SL is set low, QI and Q2 are turned on and their on-resistance is so small that VDDV and GNDV function as real power lines. Therefore, the NAND gate operates normally and at a high speed because the *vth* of 0.3 V is low enough relative to the supply voltage of 1 V. In the sleep mode, when SL is set high, Ql and Q2 are turned off so that the virtual lines VDDV and GNDV are assumed to be floating. The relatively large leakage current,

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determined by the subthreshold characteristics of low-*vth* MOSFET's, is almost completely suppressed by Ql and Q2 since they have a high *vth* and thus a much lower leakage current. Therefore, power consumption during the stand-by period can be dramatically reduced by the sleep control. It should be pointed out that two other factors affect the speed performance of an MTCMOS circuit. One is the size of the sleep control transistors Ql and Q2, and the other is the capacitances *CV1* and *CV2* of the virtual power lines.

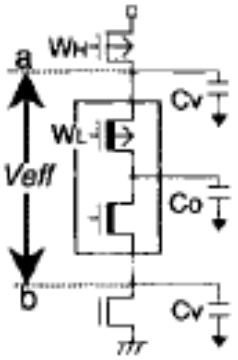

Fig. 4 Simulation circuit model.

Ql and Q2 supply current to the virtual lines. The larger their gate widths are designed, the smaller the on-resistance becomes. *CV1* and *CV2* also act as temporary supply sources to internal logic gates. Thus, the voltage rise in GNDV and drop in VDDV caused by the switching of the internal logic gate are suppressed by setting them large enough to maintain high-speed performance. To confirm the effects, simulations were carried out. Fig. 4 shows the gate delay time *tpd* and effective supply voltage *VeJ J* dependence on the normalized gate width of sleep control transistors *WH jW L* along with the simple single MTCMOS circuit model used for simulations, where *VeJ J* is defined as the minimum value of spontaneous voltage difference between VDDV and GNDV (between node a and b in this simulation). It is clear that larger *Cv*, virtual line capacitance, and *WH ,* sleep control transistor width, maintain the effective supply voltage *VeJ J* for the internal logic gates and enhance the speed performance. For instance, a *WH jWL* of 5 and *Cv jCo* of 5 keep the decrease in *VeJ J* within 10% of *Vdd* and the degradation in gate delay time within 15% compared to a pure low-*vth* CMOS. The area penalty for the wider gate transistors is relatively small because they are shared by all the logic gates on a chip. As for *Cv,* the above condition is generally met in an actual LSI because *Cv* includes the source capacitances of all the logic gates connected to virtual power lines and wiring capacitances. Therefore, nothing extra need be added.

B. Electrical Performance

The measured MTCMOS logic gate delay time is shown in Fig. 5(a) as a function of supply voltage. Data for the conventional full high-*vth* and full low-*vth* CMOS logic gates are also plotted for comparison. It is obvious that the voltage dependence of an MTCMOS gate delay is much smaller than that of a conventional CMOS gate with high-*vth* and that the MTCMOS gate operates almost as fast as the full low-*vth* gate. At a l-V power supply, the MTCMOS gate delay time is reduced by 70% as compared with the conventional CMOS gate with high-*vth.* The dependence of normalized power- delay product (NPDP) on supply voltage is shown in Fig. 5(b).

C. *Design of Flip-Flop Circuit*

Special attention must be paid to the MTCMOS design of latch or flip-flop circuits that have memory functions. This is because memorized data in latch or flip-flop circuits must be retained even in the sleep mode when virtual power lines are floating to cut leakage current completely. The proposed MTCMOS latch circuit is shown in Fig. 6(a), which is used for flip-flop circuits.

1) A conventional inverter G2 and a newly added one G3 are composed of high-Vth MOSFET's. They are connected directly to the true power supply lines VDD and GND. The latch path consists of G2 and *G3,* which are always provided with power. Therefore, data can be retained even in the sleep mode, when the clock signal CLK is fixed by using the sleep control signal SL. G3 is designed to be smaller to suppress both the increases in the gate delay time and the area.

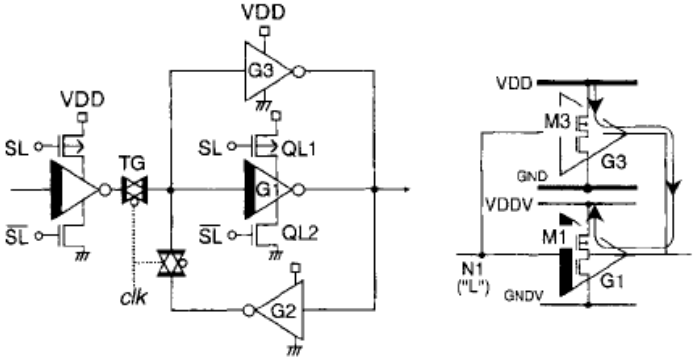

Fig. 2. MTCMOS Latch circuit.

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2) As for the forward path, the inverter Gland the CMOS-type transmission gate TG are composed of low-*Vth* MOS- FET's. This makes high-speed operation possible at 1-V power supply. This circuit also includes local sleep control transistors QL1 and QL2 with high- *Vth*. The reason for including them can be understood with Fig. 6(b), where a node N I is assumed to maintain a "low" state in the sleep mode. If G 1 were connected directly to the virtual power line VDDV, as shown in this figure, VDD and VDDV would be short through M I and M3, so that stand-by current would be increased in the sleep mode. Therefore, QLl and QL2 are indispensable for completely cutting the leakage current path. Fig. 7 shows the simulation results for the delay time of the MTCMOS latch circuit. They confirm that the delay time is reduced by 50% at I V compared with that of the conventional circuit with high- *Vth*. Furthermore, the stand-by current in the sleep mode was also confirmed to be almost as low as that of the high- *Vth* circuit.

IV. SIMULATION RESULTS

To confirm the effectiveness of MTCMOS circuit technology, a PLL LSI using new MTCMOS standard cells was designed and fabricated. Conventional *0.5-p,m* CMOS process technology for 3.3-V operation with single-poly silicon and double-metal layers was used. MOSFET's with different *Vih*'s in the same well were formed by optimizing the impurity concentration in the well and controlling the channel doses with two additional masks, which minimizes the increase in the number of process steps.

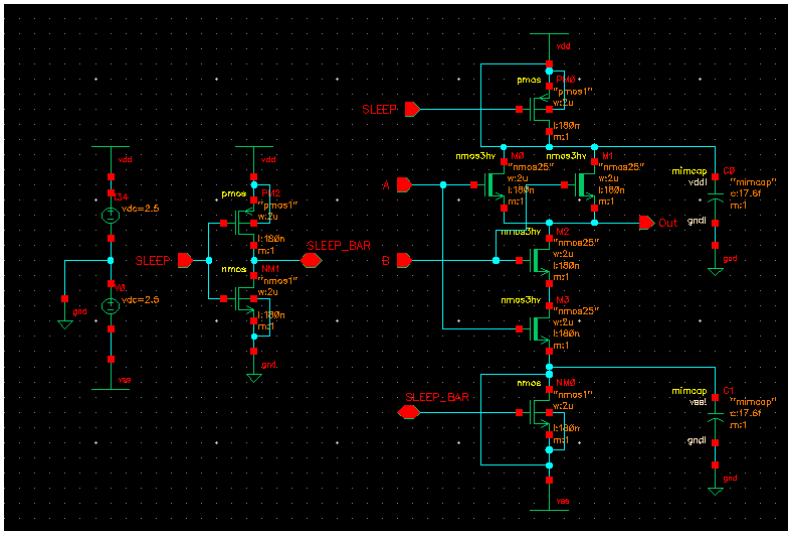

Fig. 2. MTCMOS circuit scheme.

One of the key device parameters and characteristics are summarized in Table II. The gate length of the low-*Vih* MOSFET is 0.65um which is 0.1um longer than that of the high-Vih ones. This is preferable to suppress variations in the threshold voltage due to short- channel effects. The gate oxide thickness is 110 A for both types of MOSFET's. The low-Vth's are 0.25 V for N-channel and -0.35 V for P-channel MOSFET's.

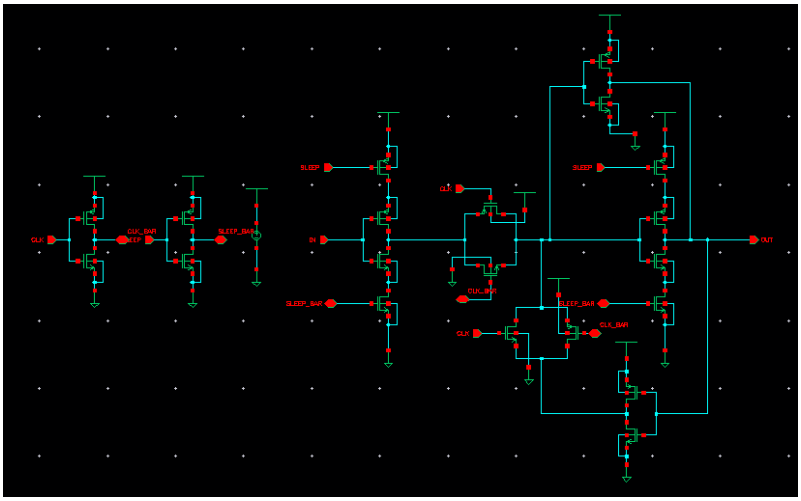

Fig. 3. MTCMOS latch circuit.

A microphotograph of the PLL chip is shown in Fig. 11. This chip consists of about 5 K gates, including the automatic frequency control circuit and the intermittent operation controller [8]. The whole chip is 4 x 5 mm", and the digital core is about 2 x 2 mm", the area penalty factors in this study.

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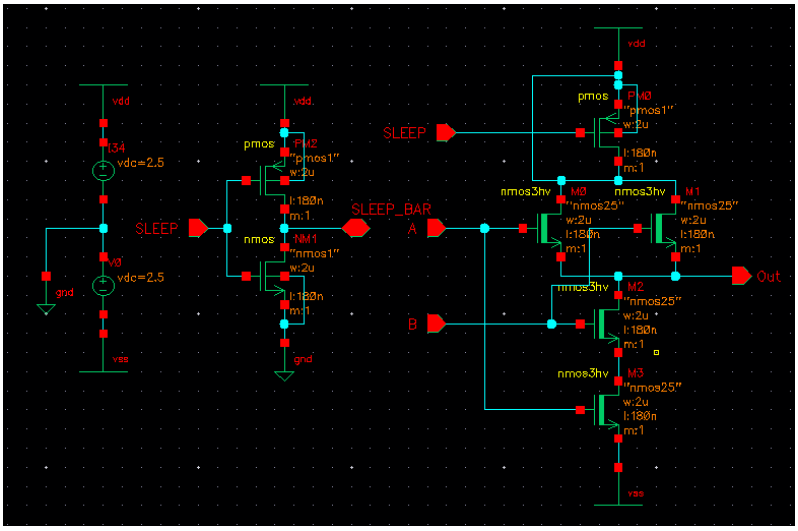

Fig. 4. Simulation circuit A.

An MTCMOS combinational circuit cell has an area about 10% larger than a conventional cell does owing to the insertion of virtual supply lines and the sleep control line. A sequential circuit cell, such as an MTCMOS OFF with clear, needs an area about twice that of a conventional cell in order to store data even in the sleep period. The area increase for the whole digital core, however, is only 30% in spite of the fact that the OFF's occupy a relatively large part (about 50%) of the total gate counts.

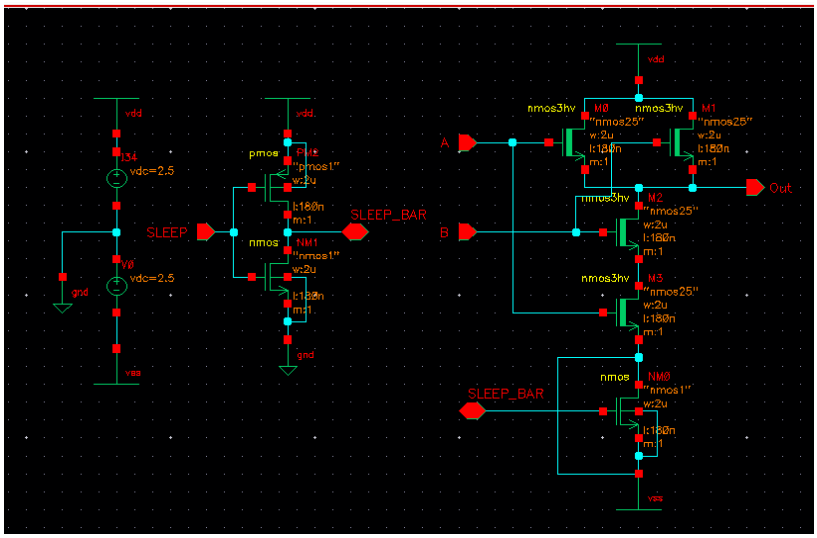

Fig. 5. Simulation circuit B.

This is because the channel area is almost unchanged. Moreover, because all OFF's in an actual LSI aren't expected to hold the date during sleep period, the area penalty can be further reduced by appropriately combining the use of a conventional OFF and the OFF with a special memory function.

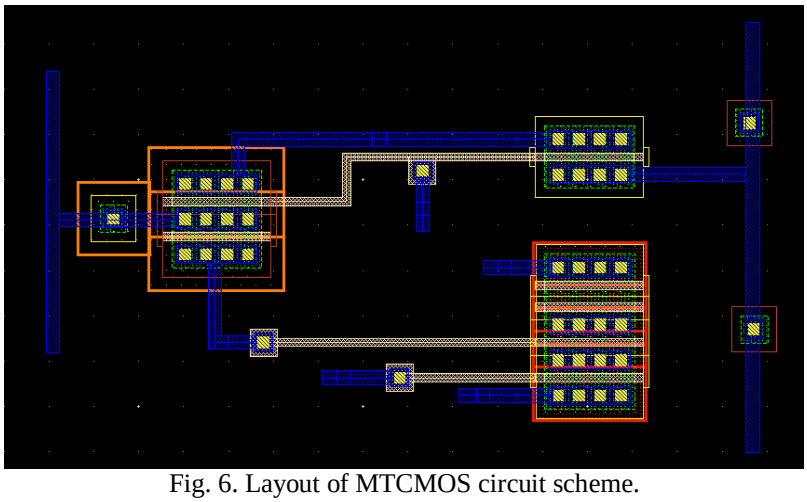

Fig. 6. Layout of MTCMOS circuit scheme.

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Fig. 12 shows the measured operation frequency as a function of supply voltage. At 1 V, the chip operates at 18 MHz which is sufficient for many applications. Fig. 13 shows the power dissipation in the digital core as a function of supply voltage at an operation frequency of 12.8 MHz. The power dissipation of the conventional 5-V operation PLL is also plotted for comparison. At 1 V, power dissipation is drastically reduced to below *1/20* compared with that of the conventional LSI operated at 5 V. Fig. 14 shows another aspect of the power performance-the operating current versus the operating frequency for the worst case at a supply voltage of 1.2 V. Although the operating current is proportional to the frequency in the region over 1 MHz, it becomes almost constant in the low-frequency region. This is due to the leakage current caused by using low-Vih MOSFET's.

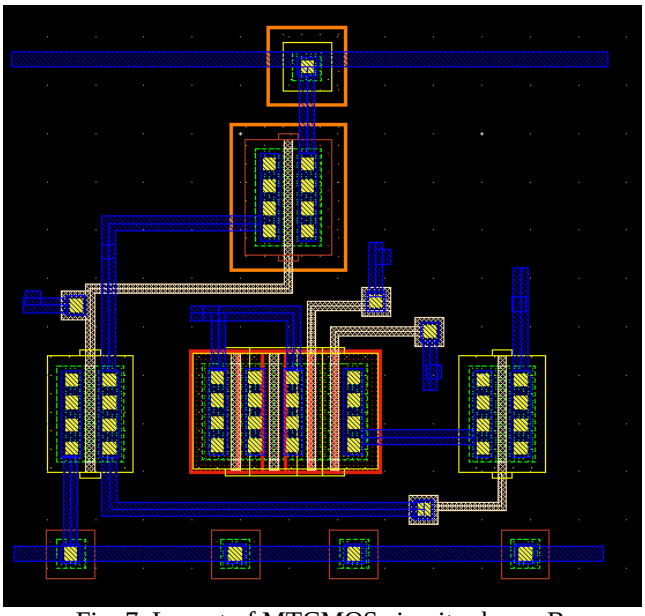

Fig. 7. Layout of MTCMOS circuit scheme B.

In the active mode, the leakage current of about 30 in this chip is negligible because it is less than the dynamic current consumption at a desired operating frequency of over 10 MHz. In the sleep mode, on the other hand, the current is dramatically reduced to below 50 nA, so that low stand-by characteristics can be obtained.

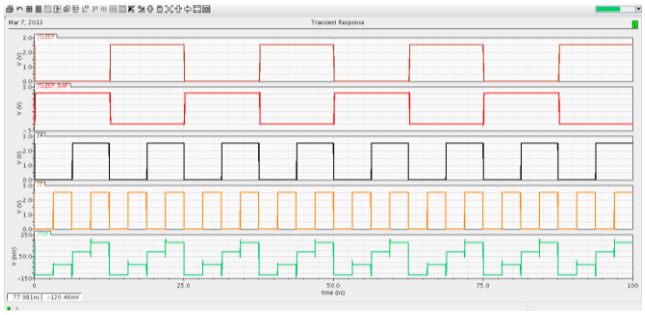

Fig. 8. Waveforms of MTCMOS circuit scheme

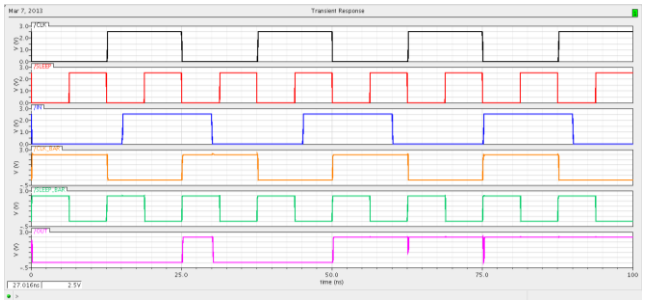

Fig. 9. Waveforms of MTCMOS latch circuit.

The MT-CMOS standard cell library was developed to simplify ASIC design. Figure 4 shows the MT-CMOS standard cell based layout scheme. One feature is that the virtual power supply lines (VDDV and GNDV) and the mode control signal line (SL) are buried in each cell. Another is that high-Vth MOSFETs Q 1 and Q2 are buried in the power supply cell which provides the area for connecting power supply lines to each other in x and y directions. Power supply cells are placed on both sides of the cell based core.

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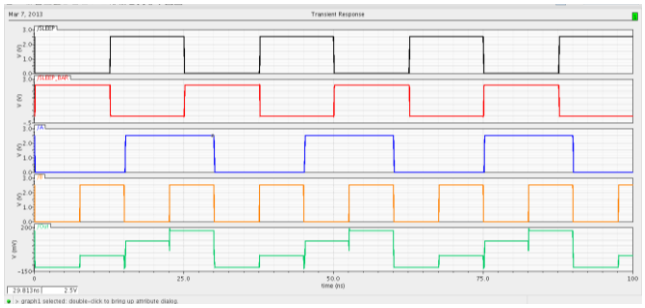

Fig. 10. Waveforms of Simulation circuit A.

This layout scheme allows VDDV, GNDV ,SL lines, and Ql and Q2 to be connected automatically throughout the chip with a minimum increase in chip area. Therefore, conventional CAD tools can be easily used to layout MT-CMOS LSIs. The size of the high-Vth MOSFETs QI and Q2,through which charge is supplied to VDDV and GNDV, also affects the speed performance of LSIs. It should be fixed by considering the operation of each LSI and the total number of cells laid-out, Here, the poly-gate width of Ql and Q2 was set to be 10 times larger than that of the logic cells, which is large enough to suppress the voltage bounce of VDDV and GNDV caused by intemal logic gate switching.

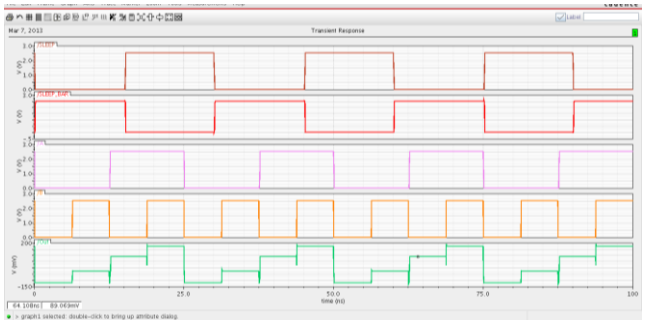

Fig. 11. Waveforms of Simulation circuit A

V. CONCLUSION

To achieve 1-V high-speed and low-power LSI operation, a new multi-threshold CMOS (MT-CMOS) circuit technology was developed. By using MOSFXTs with both high-threshold voltage and low-threshold voltage, high-speed and low leakage current features have been achieved even in I-V operation. To demonstrate the effectiveness of the technology, a standard cell based PLLLSI was designed as a carrying vehicle with the 0.5-pm MT-CMOS process. High-speed operation of 18 MHz at 1 V was successfully obtained. Multi threshold-voltage CMOS (MTCMOS) circuit technology has been proposed as a way to achieve a 1-V supply voltage high-speed and low-power LSI operation. This technology uses MOSFET's with two different threshold voltages on a single chip and introduces a sleep control scheme for efficient power management.

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