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A Novel Implementation of Low Power Universal Shift Register

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Abstract— Low power is a challenging work in digital design .In digital circuits, a shift register or a counter is a cascade of flip flops, and also they form a sequential logic. Implementing power optimization on all the components of the shift registers is a choice. Shift registers comprises one of the most basic operational unit in any processor and multipliers to process the output of the systems. This paper mainly concentrates on power reduction of the digital components by introducing a novel architecture. This proposed architecture eliminates the conducting path in between voltage rail to ground rail during state transitions by providing high resistance path, so that the short circuit current in between rails can be reduced which in turn causes drastically reduction in power consumption. These different circuit parameters are evaluated with TANNER 13.1 using IBM SCN CMOS 250nm technology at room temperature. The simulation results indicate that the proposed architecture has reduced 40% of power dissipation when compared with that of conventional Architectures.

Keywords— USR, CMOS, LCT, etc.

I. INTRODUCTION

Our living criterion has been enhanced with the advancements in the Integrated circuit technology. The main parameters for a design engineer in VLSI are area, performance, cost and reliability. However, in recent years much importance and focus is given to the reduction in power consumption rather than area and speed considerations. There are many factors responsible for the evolution of this trend. The Low power consumption factor is considered as the primary driving factor which has been a remarkable success in the growth of personal computing devices like portable desktops, audio and video-based multimedia products, wireless communications systems like personal digital assistants and personal communicators. Such devices demand high- speed computation and complex functionality with low power consumption. Therefore the building of Low Power VLSI systems has been emerged as they are very high in demand because of the rapid growth in technologies regarding to mobile communications and computations.

The battery technology does not advance at the same rate as the microelectronics technology. There is a limited amount of power available for the mobile systems. So designers are faced with more constraints: high speed, high throughput, small silicon area, and at the same time, low-power consumption [1]. The shift register is the core unit in DSP and ASIC applications where this is used in multiplication, shifting, and counting purposes. A shift register can perform a variety of arithmetic and logical operations. Since the architecture of shift register has several implications on power consumption, delay, and area, the manner in which these operations can be organized is a problem. In this paper, we are mainly concerned with the power consumption, its performance in terms of delay and transistor count of the shift register. Hence proper choice of shift register architecture is needed when the design for low power consumption is targeted.

II. LOW POWER

Power can be minimized at either system level or architecture level or algorithm level or microarchitecture level or gate level or circuit level. Here, we made an attempt to reduce the power at circuit level. It is not a straight forward task to calculate power of a system because the power calculation involves all the IC design stages to be considered, beginning with the system behavioral description and ending with the fabrication and packaging process. In some of these stages there are guidelines that are clear and there are steps to follow that reduce power consumption, such as decreasing the power-supply voltage. While in other stages there are no clear steps to follow and hence statistical or probabilistic heuristic methods are used. But basically in a CMOS circuit, the majority of energy dissipation is given by

$$\text{Energy} = \sum_{N} \frac{1}{2} * CV^2T$$

Where N number of nodes
T number of transitions

Here three factors that can be reduced to achieve low energy per addition are the number of nodes, the nodal capacitance, the power supply voltage and the number of transitions on each node. There are three major components of

power dissipation in CMOS circuits[2]:

1) Switching Power: Power consumed by the circuit node capacitances during transistor switching.

2) Short Circuit Power: Power consumed because of the current flowing from power supply to ground during transistor switching.

3) Static Power: Due to leakage and static currents

The first two components are referred to as dynamic power. Dynamic power constitutes the majority of the power dissipated in CMOS VLSI circuits. T is the power dissipated during charging or discharging the load capacitances of a given circuit. It depends on the input pattern that will either cause the transistors to switch (consume dynamic power) or not to switch(no dynamic power consumed)at every clock cycle. It is given by the following

$$P_{avg} = P_{dynamic} + P_{short-circuit} + P_{static}$$

$$P_{avg} = V_{DD} * f_{clk} * \sum_i (V_{iswing} * C_{iload} * \propto_i) + \quad V_{DD} * \sum_i (I_{isc} + V_{DD} * I) .$$

Where f_{clk} denotes the system clock frequency, V_{I}swing is the voltage swing at node *I* (ideally equal to V_{DD}),C_{i}load is the load capacitance at node *I* ,*ai* is the activity factor at node *i*, and I_{i}sc and *I*are the short circuit and leakage currents, respectively. The dominant term in power dissipation of CMOS circuits is the power required to charge or discharges the capacitance in the circuit. Thus by reducing capacitance we can decrease the circuit delay and power dissipation. Capacitance is in turn a function of logic cells being used in the design.

III. UNIVERSAL SHIFT REGISTER

In digital circuits, a shift register is a cascade of flip flops, sharing the same clock in which the output of each flip-flop is connected to the data input of the next flip-flop in a chain resulting in a circuit that shifts the bit array stored in it by one position. At each transition of the clock input, the data at the input as well as the output shifts by one position. The architecture of a shift register can be designed using basic gates such as AND, OR, NOT and XOR. A digital signal or waveform with discrete delay can be produced using shift registers. If 'n' is the number of shift register stages then repeating square wave is delayed by 'n' discrete clock times. In the past some hundred stages of shift registers were used as a digital memory. This obsolete application is reminiscent of the acoustic mercury delay lines used as early computer memory. In Serial data transmission, for the conversion of parallel from to serial form, shift registers were used over a distance of few kilo meters. Many slow parallel data lines are replaced with a single serial high speed circuit in serial data communications. Serial data over shorter distances (tens of centimeters), uses shift registers to get data into and out of the microprocessors. Numerous peripherals, including analog to digital converters, digital to analog converters, display drivers, and memory, uses shift registers to reduce the amount of wiring on PCB's.

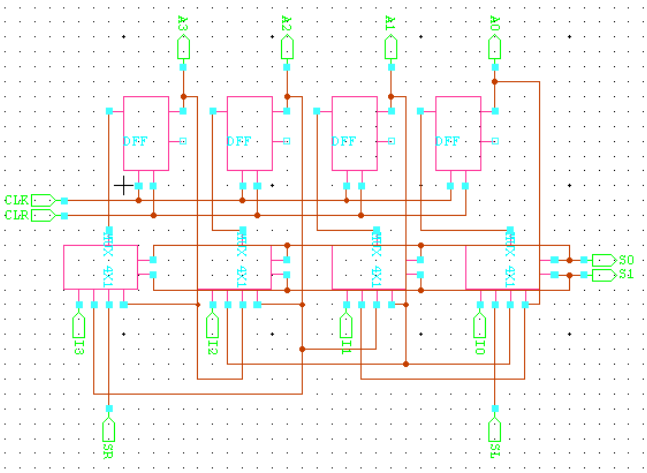

Fig. 1 Block Diagram Representation of USR

A universal shift register can transfer data in three different modes. It can act like a parallel register where it can load and transmit data in parallel. In shift register mode it can load and transmit data in serial order, through left shift or right shift. And further the universal shift register can combine the capabilities of both parallel and shift registers to perform the tasks that neither basic types of register can perform on its own. For instance, on a particular job, a universal register can load data in series and then transmits data in parallel. In computers, these Universal shift registers, are used as memory elements. For efficient storage of large amounts of data their might be other types of memory devices, but from the view of a digital system perspective, a computer memory means a combination of registers. Also, all the operations in a digital system are performed on registers. Some of the Examples under such operations are multiplication, division, and data transfer. In order for the universal shift register to operate in a specific mode, it must first select the mode of operation. For this purpose a set of two selector switches, S1 and S0 are used. In this paper, we are designing a Universal Shift Register using the proposed architecture and concentrating up on its effects on power consumption and its area. Therefore, we are able to design a universal shift register that is capable of performing all the shift operations.

IV. CMOS LOGIC USR

The most widely used logic style is static complementary CMOS. Primary advantage of the CMOS structure is robustness (i.e., low sensitivity to noise), good performance, and low power consumption with no static power dissipation. The complementary CMOS circuit style falls under a broad class of logic circuits called static circuits in which at every point in time (except during the switching transients), each gate output is connected to either VDD or Vss via a low-resistance path.

A static CMOS gate is a combination of two networks, called the pull-up network(PUN) and the pull-down network (PDN). The figure shows a generic N input logic gate where all inputs are distributed to both the pull-up and pull-down networks**.** The function of the PUN is to provide a connection between the output and VDD anytime the output of the logic gate is meant to be 1 (based on the inputs). Similarly, the function of the PDN is to connect the output to VSS when the output of the logic gate is meant to be 0.The PUN and PDN networks are constructed in a mutually exclusive fashion such that one and only one of the networks are conducting in steady state. In this way, once the transients have settled, a path always exists between VDD and the output F, realizing a high output ("one") or alternatively, between VSS and F for a low output ("zero").The PDN is constructed using NMOS devices, while PMOS transistors are used in the PUN. The primary reason for this choice is that NMOS transistors produce "strong zeros," and PMOS devices generate "strong ones". A parallel connection of transistors in the pull-up network corresponds to a series connection of the corresponding devices in the pull-down network and vice versa.

CMOS logic gates use complementary arrangements of N-channel and P-channel Field effect transistors. CMOS almost uses no power in the static state (i.e. when inputs are not changing). In a steady 1 or 0 state, a CMOS gate draws no current other than leakage current. When the gate switches states, current is drawn from the power supply to charge the capacitance at the output of the gate. CMOS devices were well-adapted to battery-operated systems with simple power supplies. CMOS gates can also tolerate much wider voltage ranges than TTL gates because the logic thresholds are (approximately) proportional to power supply voltage, and not the fixed levels required by bipolar circuits. The extremely small capacitance of the on-chip wiring, caused an increase in performance by several orders of magnitude

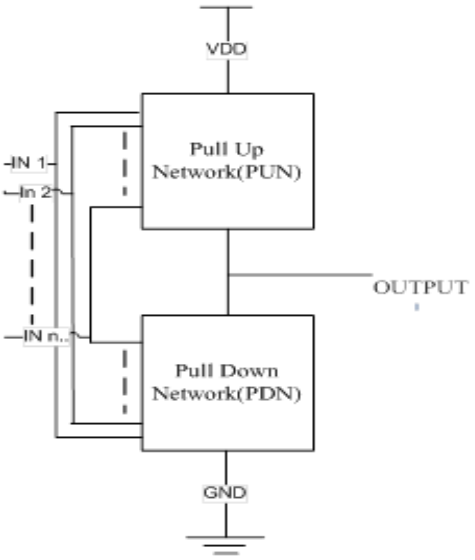

Fig. 2 Block Diagram Representation for CMOS Logic

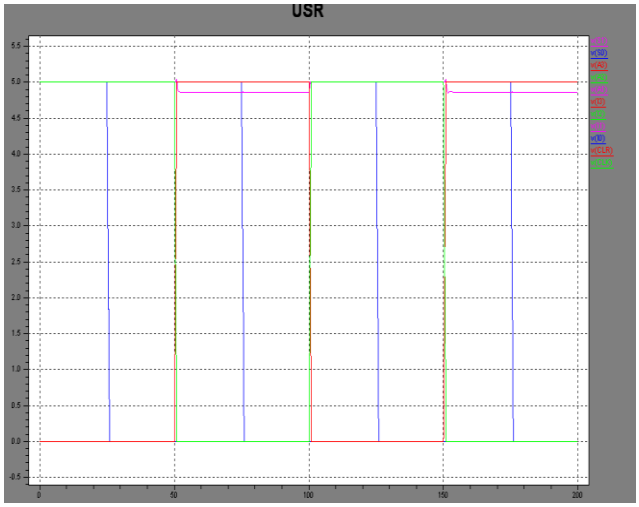

Fig. 3 Simulated Results of CMOS USR Circuit

V. PROPOSED ARCHITECTURE

One leakage control transistor (a p-type)is introduced within the logic gate for which the gate terminal of leakage control transistor (LCT) is controlled by the source of the transistor. In this arrangement, the LCTs is always "near its cutoff voltage" for any input combination. This increases the resistance of the path from Vdd to ground, leading to significant decrease in leakage currents. The gate-level net list of the given circuit is first converted into a static CMOS complex gate implementation and then LCTs are introduced to obtain a leakage-controlled circuit. The significant feature of LCT is that it works effectively in both active and idle states of the circuit, resulting in better leakage reduction the basic idea behind the approach for reduction of leakage power is the effective stacking of transistors in the path from supply voltage to ground.

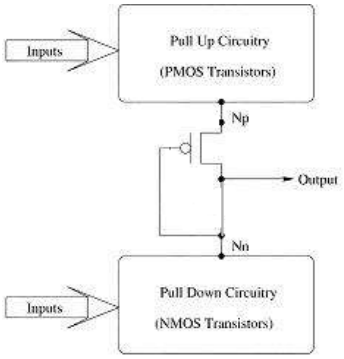

Fig. 4 proposed Architecture Representation.

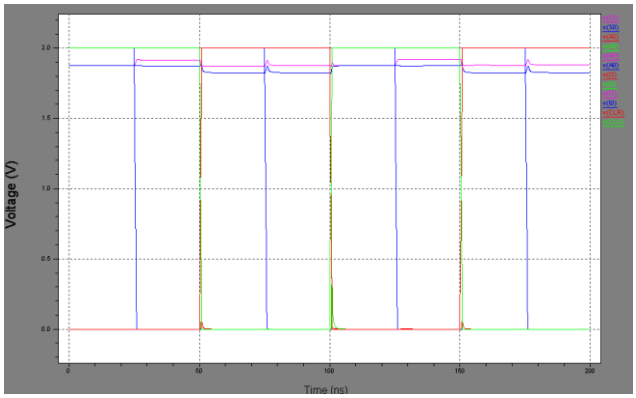

Fig 5 : Simulated Results of Proposed USR

VI. RESULT ANALYSIS

We have performed the simulator of the above USR circuits by using TANNER in 250 nm CMOS technology.The supply voltage we have considered is 1.8 V.The output of different functional waveforms as shown in above figures.Actually we have not considered the environment setup required for the circuits to test driving capability and loading effect.We look for the low power dissipated type of USR architecture.Here we are giving the details of transistor count,Leakage Current and the power dissipated for each mode of circuit..

Table 1: Comparison Results of Different USR Architectures

	P_d (W)	# Tr	I_l (A)	$Max\ P_d$ (W)
CONVENTIONAL USR	5.12e-003	272	1.70e-003	2.97e-002
PROPOSED USR	1.26e-004	340	0.42e-003	5.62e-003

VII. CONCLUSIONS

In this paper the comparison of conventional Universal Shift register with Proposed Universal Shift register was carried out by taking the power dissipation, transistor count, leakage current and maximum power dissipation used in account. The SPICE simulation result shows that the Proposed USR architecture is best as far as the power dissipation and leakage current is concerned. But when the turn time transistor count comes it has been seen that the conventional logic.

The power dissipated in the proposed universal shift register architecture is 40%below that of conventional CMOS Universal shift register and the leakage of Proposed USR is almost 75%less when compared with Conventional CMOS architecture. So, In future it can be further extendable to reduce the number of transistor with low power. It can be implemented for multi bit USR which is required for future generation for higher data processing.

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