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Design of VHF Radar Transmit Pulse Generator by Using Direct Digital Synthesizer (DDSAD9856) for Pilot Active Array Radar Application

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Abstract— Traditional designs of high bandwidth frequency synthesizers employ the use of a phase-locked-loop (PLL). A direct digital synthesizer (DDS) provides many significant advantages over the PLL approaches There are a many practical applications for precision signal sources. For this, it was created the Direct Digital Synthesis (DDS), that can generate signals with high frequency resolution and fast frequency switching speeds by using digital control Fast settling time, sub-Hertz frequency resolution, continuous-phase switching response and low phase noise are features easily obtainable in the DDS systems. Direct digital synthesizers are used for constructing digital down- and up-converters, demodulators, and implementing several types of modulation schemes, including PSK (phase shift keying), FSK (frequency shift keying) and MSK (minimum shift keying). This paper will describe theoretically this subject and presents a practical implementation of a circuit with Integrated Circuit (CMOS) Technology.

Keywords— DDS, System clock, Sampling and Quantizing theorems.

INTRODUCTION

Direct digital synthesis (DDS) is a method of producing an analog waveform—usually a sine wave by generating a time-varying signal in digital form and then performing a digital-to-analog conversion, Because operations within a DDS device are primarily digital, it can offer fast switching between output frequencies, fine frequency resolution, and operation over a broad spectrum of frequencies. The direct digital synthesis structure (DDS) is a system that generates several output signals, with different frequencies below a maximum value. It is based on the principle that an analog waveform can be generated by using its samples. The DDS technique is limited by the Nyquist criteria and the sampling theorem . [1]. It is an important signal generating technique for frequencies below 200MHz,limited by the DDS performance [2]. During the generation process, it is possible to modify the phase, frequency and amplitude characteristics of the synthesized output signal.

DDS PERFORMANCE

By comparing DDS structure with the phase locked loop (PLL) synthesizer, the most used type during last years, DDS does not have a tuning process as the big advantage. DDS circuit presents the desired output signal, with locked performance and digital precision. That DDS inherent characteristic property assures a construction high repeatability, with great precision and very good performance. These are very important factors in production of components, subsystems and equipment.

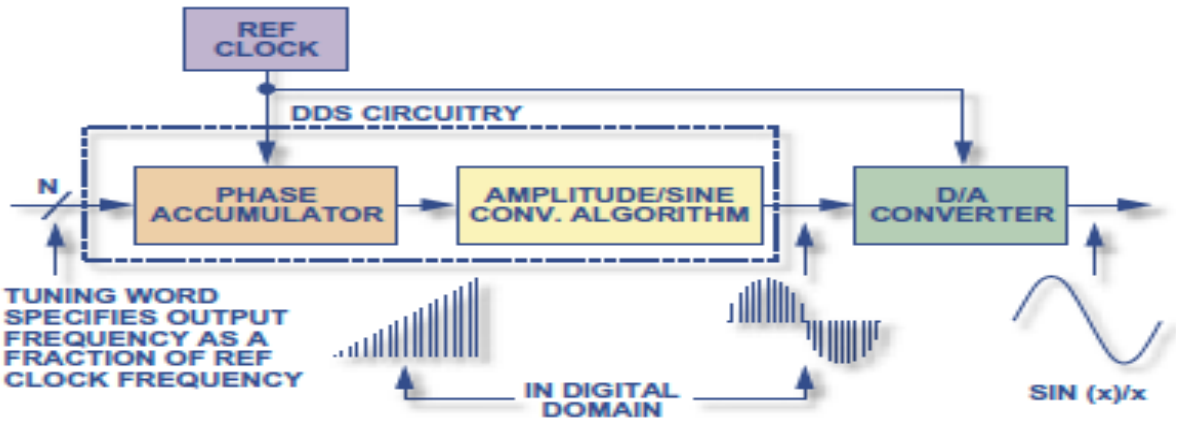

Fig. 1 Block Diagram of a Direct Digital Synthesis Structure (DDS).

DDS basic block diagram is presented in Fig. 1 and each one of its parts will be explained. The first one is its main components are a phase accumulator, a means of phase to-amplitude conversion (often a sine look-up table), and a DAC. A DDS produces a sine wave at a given frequency. The frequency depends on two variables, the reference-clock frequency and the binary number programmed into the frequency register (tuning word).The binary number in the frequency register provides the main input to the phase accumulator. If a sine look-up table is used, the phase accumulator computes a phase (angle)address for the look-up table, which outputs the digital value of amplitude—corresponding to the sine of that phase angle—to the DAC. The DAC, in turn, converts that number to a corresponding value of analog voltage or current. To generate a fixed-frequency sine wave, a constant value (the phase increment—which is determined by the binary number)is added to the phase accumulator with each clock cycle. If the phase increment is large, the phase accumulator will step quickly through the sine look-up table and thus generate a high frequency sine wave. If the phase increment is small, the phase accumulator will take many more steps, accordingly generating a slower waveform.

COMPONENT PARTS AND PERFORMANCE DESCRIPTION

The digital-to-analog converter device converts the generated digital signal by the LUT to its sample-and- hold form. It is implemented by using a D/A converter, whose function is a very critical part in DDS structure [4]. Next part is the filter that interpolates and filter the signal delivered by the converter D/A. The filter removes the images frequencies

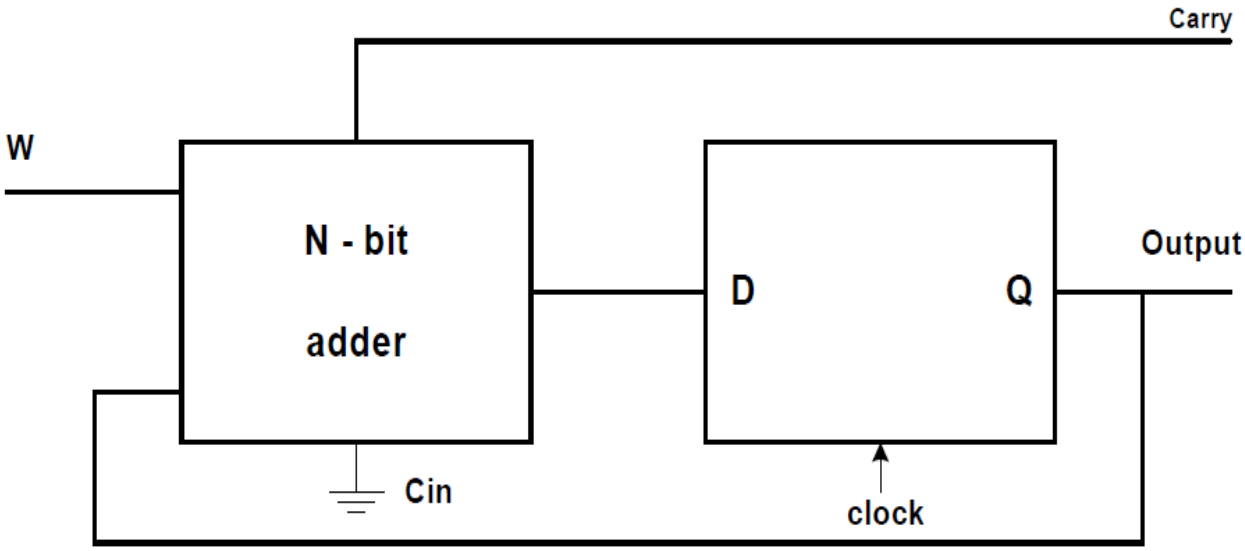

figure. 2 Basic implementation of an accumulator.

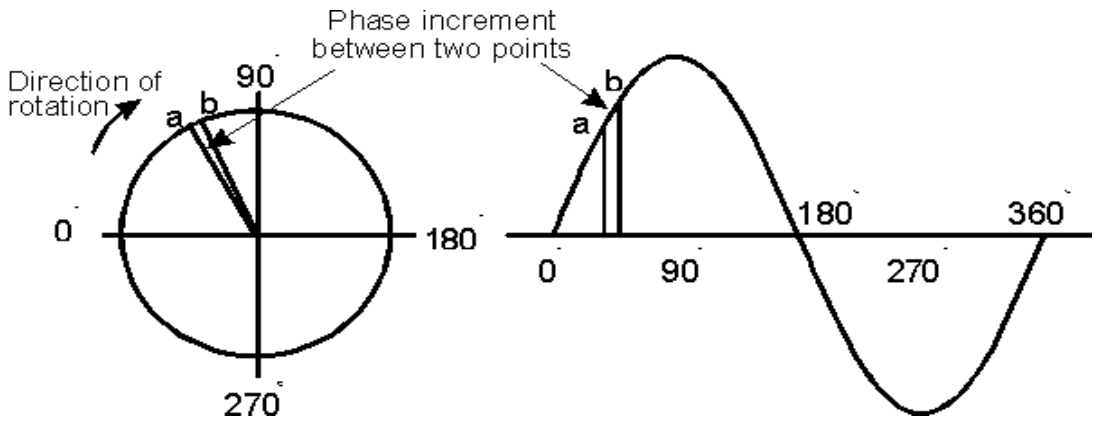

figure. 3 Relation between the phase and the amplitude.

Fig. 4 Digital Phase Wheel

IMPLEMENTATION BY USING CMOS

The implementation of digital functional blocks makes it possible to achieve a high degree of system integration. Recent advances in IC fabrication technology, particularly CMOS, coupled with advanced DSP algorithms and architectures are providing possible single-chip DDS solutions to complex communication and signal processing subsystems as modulators, demodulators, local oscillators (LOs), programmable clock generators, and chirp generators

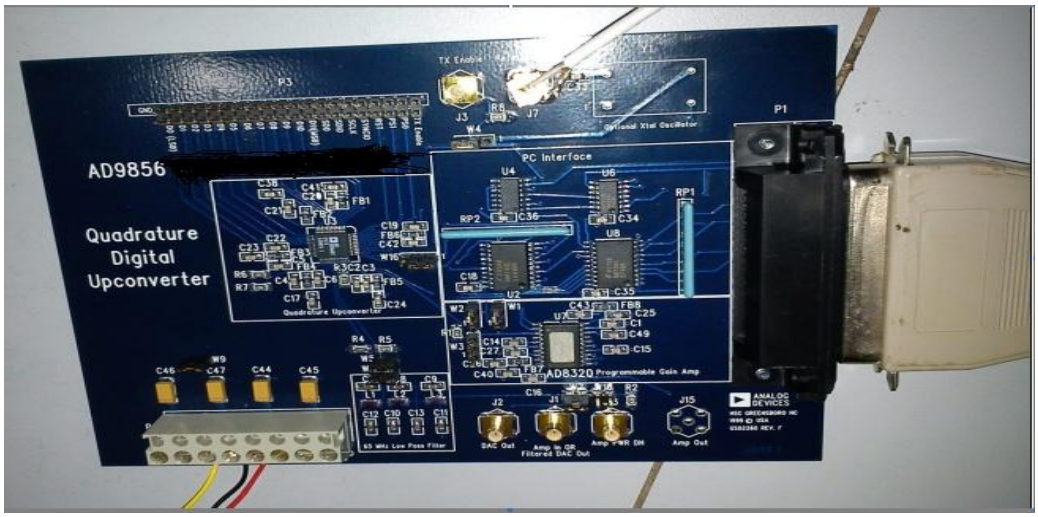

Figure 5 .DDS AD9856 Printed Circuit Board

Figure 6 Input 13.25 MHz to Output 53 MHz Generating Setup using DDS AD9856 Printed Circuit Board

Calculating the Frequency Tuning Word (FTW) for 53MHz Output
The equation relating output frequency of the DDS AD9856 Digital Modulator to the frequency tuning word (FTWORD) and the system clock (SYSCLK) is given as:

A_out = (FTWORD x SYSCLK)/2^32

Where A_out and SYSCLK frequencies are in Hz and FTWORD is a decimal number from 0 to 4,294,967,296 (2^31).

Find the Frequency Tuning Word (FTW) for

A_OUT = 53 MHz and SYSCLK = 13.25 MHz

If A_OUT = 53 MHz and SYSCLK = 13.25 MHz

Then, By Substituting A_Out , SYSCLK in the above Equation we get

Frequency Tuning Word (FTW) = 400000000 (hex) this hex value is converted in to the binary form.

LABORATORY MEASUREMENTS AND RESULTS

To evaluate the performance of the circuit, several important parameters measurements were made in laboratory, with help of a digital oscilloscope, a spectrum analyzer, a bias source adjusted to 3.3V voltage and a clock source (Fig. 6 and Fig. 7). The design characteristics were: 13.5MHz clock master, 10 bits phase increment, 10 bits phase accumulator, 10 bits ROM address, 10 bits D/A converter. Results obtained were: 53MHz output frequency, 6MHz maximum output frequency, 3.5V output signal amplitude:, 15.6kHz frequency resolution by each step. By adjusting the increment of phase in the accumulator input it can be can saw, in oscilloscope or in spectrum analyzer, the changes of the output signal frequency, with digital precision of 15.6kHz by step, given by the number of bits of the phase accumulator. As high the synthesized signal frequency and as closer of limit given by Nyquist criteria, a worse output signal-to-noise relation is obtained. In this case, the output signal filtering will be a more difficult process also. With help of the obtained measurements it can be saw that the frequency must be synthesized until37.5% of clock master, and that is too close of the stipulated theoretical value.

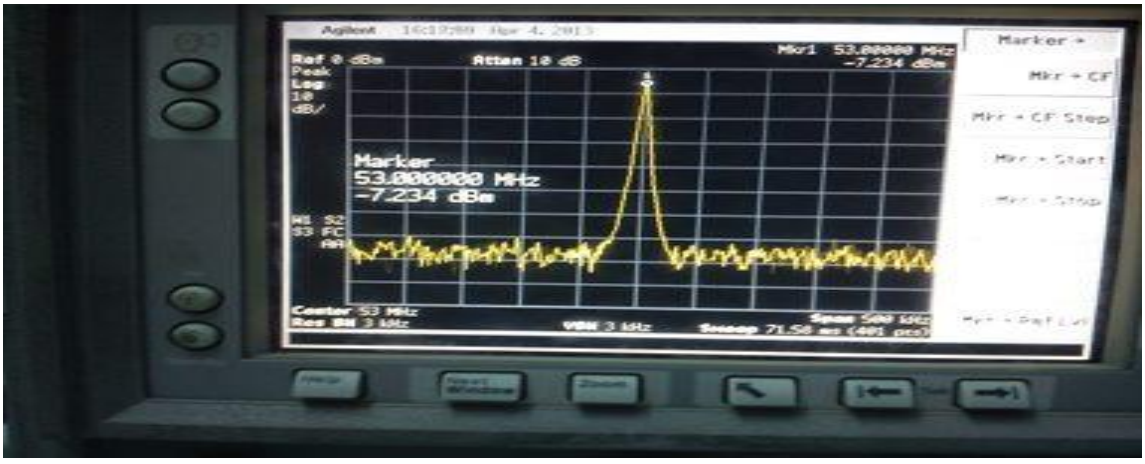

Figure.7 Frequency Domain Output Signal As Shown By Spectrum Analyzer

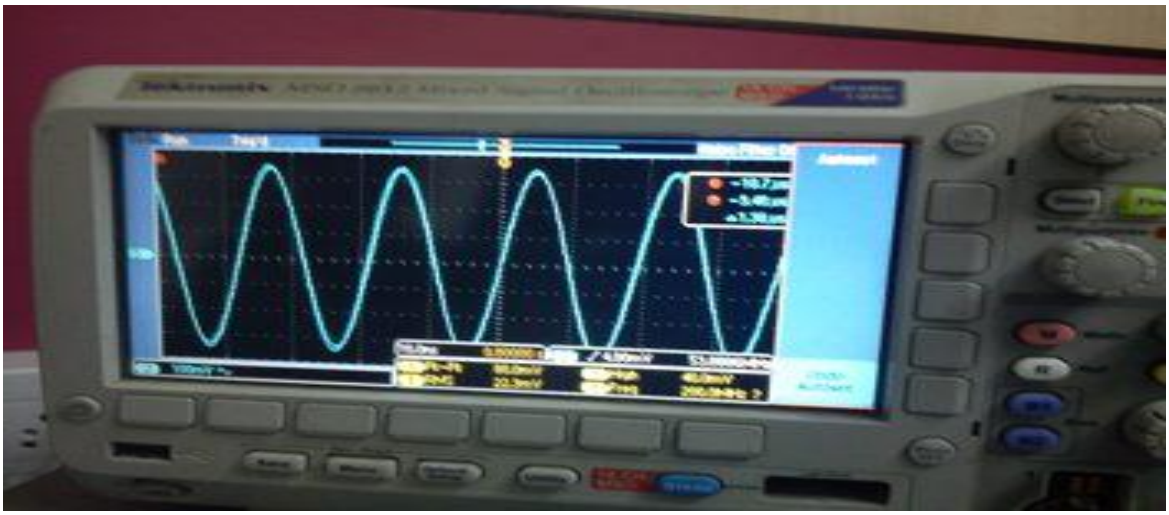

Figure. 8 Time Domain output signal as shown by digital oscilloscope.

Conclusion

The purpose of this article is to show how to make a direct digital synthesizer using the CMOS structure and the how easy it can bring to a project flexibility change. This characteristic can be observed in a FSK modulation without changing the circuit hardware shown in Fig. 5. It is important to point that DDS technology nowadays has a limitation to 400MHz frequency synthesis. This is due the fact that the analog components can not work with clock master upper than 1GHz. Because the digital signal Nyquist limitation and the quality of real components the maximum value is fixed just 40% of 1GHz.

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