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Performance Optimization of Folded Cascode OTA Using an Evolutionary Algorithm

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Abstract— In this paper we propose a simulation based approach for optimizing the performance of folded cascade OTA by use of particle swarm optimization algorithm. There are some trade-offs between Gain, BW, PM, CMRR and PSRR in OTA design which force the designer to accomplish such a long time complicated work to optimize the circuit. In this work the usage of PSO algorithm in automated optimization of FCOTA has been investigated. The PSO algorithm is implemented in MATLAB which has been linked with an electrical simulator, HSPICE. It gets a netlist as its input while the output is active devices sizes and passive values. Obtained results which compared with three other works prove the effectiveness of this approach.

Keywords—folded cascode OTA; PSO; circuit design optimization; evolutionary algorithm;CMOS.

I. INTRODUCTION

Nowadays, due to increasing demand for system on chip (SoC) productions, high performance analog integrated circuit design such as operational transconductance amplifier (OTA) in CMOS technology becomes more important. The OTA is well known for its high bandwidth in open-loop configuration [1], which makes it proper for widespread application such as xDSL, 802.11 a/g WLANs, WiMax and DVB [2,3].

The OTA should provide sufficient tranceconductance gain with acceptable linearity and power consumption. Moreover, a proper phase margin which guarantees the stability is needed. Also, CMRR and PSRR are two important specifications of an OTA. Therefore there are some tradeoffs between BW, PM, CMRR, PSRR, gain, linearity and power consumption in OTA design [4].

Designers must continuously and repeatedly tune the designed circuit elements such as active devices parameters and sizes, passive devices parameters, biasing conditions, etc and perform a circuit simulation using an electric computer-aided design (ECAD) software, to achieve the best performance of the designed circuit. It is in general a long time, high complexity and complicated work. A proper optimization technique can be used to overcome this problem.

The design flow for analog circuits consists of a series of design steps from the system level to the device level [15, 16]. Most important steps between these hierarchical levels are topology selection, circuit sizing and design verification. Basically, the optimization is accomplished in the circuit sizing level that receives a topology description, a set of performance specifications and technology parameters and produces a sizing solution for the described topology.

Two approaches are developed for circuit sizing: equation-based and simulation-based. In equation-based methods, the performance evaluator is based on equations describing the behaviour of the circuit. However, the simplifications and approximations required in deriving equations cause low accuracy and incompleteness in equation-based methods [19].

Unlike equation-based methods, simulation-based approaches use a simulator, usually the ubiquitous SPICE program, as a performance evaluator. Using spice for evaluation guarantees that the design solution obtained is highly accurate. Additionally, manual derivation of performance equations is not required. GA and ES are the most popular evolutionary algorithms used in circuit sizing [17, 18, 14]; but their ability and efficiency in search and convergence to global optimum have been criticized, especially when the problem has multiple local optimum.

Particle swarm optimization is a new and robust evolutionary optimization method which has an extra ability in solving continues nonlinear optimization problems.

In this work we present a simulation based approach for optimizing the performance of folded cascade OTA using particle swarm optimization algorithm. This algorithm has been implemented in MATLAB [5]. Hence, a proper link between MATLAB and HSPICE [6], an electrical simulator for performance evaluation of circuit, has been established.

This paper is organized as follows: in Section II, the particle swarm optimization concept is explained. The OTA circuit and specifications is described In Section III. In Section IV, we propose the method of optimizing OTA design using PSO and achieved results. Finally, the conclusions are presented in section V.

II. PARTICLE SWARM OPTIMIZATION

Particle swarm optimization (PSO), first introduced by Kennedy and Ebehart [7], is an evolutionary computation method based on the social behaviour and movement of swarm searching for the optimal and best location in a multidimensional search space and has been found to be robust in solving continues nonlinear optimization problems [8].

This approach simulates the social behaviour of bird flocking or fish schooling model. Potential solutions of optimization problem are called particles. Each *particle position* is represented by a d-dimensional vector and denoted as $X_i=[x_{i1},x_{i2}, \ldots, x_{id}]$ and is randomly initialized . The set of n particle in the swarm are called *population*: $X=[X_1, X2,\ldots,X_n]$. Each particle is assumed to move around in the so called multidimensional space to reach the best position which has the best fitness value. In each iteration of simulation the fitness function for each particle is evaluated to updates the *best previous position*: $PB_i= [pb_{i1}, pb_{i2},\ldots, pb_{id}]$, which is the location of the best fitness value obtained so far by the particle.. The best position among the population is called *global best position* and described as $GB_i= [gb_1, gb_2,\ldots, gb_d]$.

The rate of position change for each particle is called particle velocity: $V_i = [v_{i1}v_{i2}, \ldots , v_{id}]$. each particle would like to return to its own optimum point, so the velocity has a term proportional to (pb_i-x_i), it would like to follow overall best global optimum point too, so a term proportional to $(gb-x_i)$ is added to velocity. Therefore:

$$v_{id}^{k+1} = wv_{id}^{k} + c_1\, rand_1^{k}\ (pb_{id} - x_i^{k}) + c_2\, rand_2^{k}\ (gb_d^{k} - x_{id}^{k}) \quad (1)$$

Where *w* is intera weight parameter which controls the trade off between the global and the local search capabilities of the swarm. c_1 and c_2 are acceleration factors and indicate the relative attraction toward *pb* and *gb* respectively. $rand_1$ and $rand_2$ are two random numbers uniformly distributed between 0 and 1, which indicate the craziness of particles[8]. *k* is the iteration number. The new position of i-th particle is then determined by:

$$x_{id}^{k+1} = x_{id}^{k} + v_{id}^{k+1} \quad (2)$$

Generally PSO has the advantage of being very simple in concept, easy to implement and computationally efficient algorithm. Since updates in algorithm consist of simple adding and multiplication operators and no derivation operation is included, computation time is dramatically decreased compared to other heuristic algorithms. In order to avoid premature convergence, PSO utilizes a distinctive feature of controlling a balance between global and local exploration of the search space which prevents from being stacked to local minima [9].

III. THE OTA CIRCUIT AND SPECIFICATIONS

An ideal transconductance amplifier is an infinite bandwidth voltage-controlled current source, with an infinite input and output impedance which used to drive small capacitive loads at high frequencies [10].

The circuit schematic of the folded-cascode OTA is shown in Fig. 1. It consists of two stages: the first one is an NMOS differential pair as input stage; and the second stage is a cascode output stage. The folded cascode architecture is used in order to increase the DC gain, common mode rejection ratio and the output resistance.

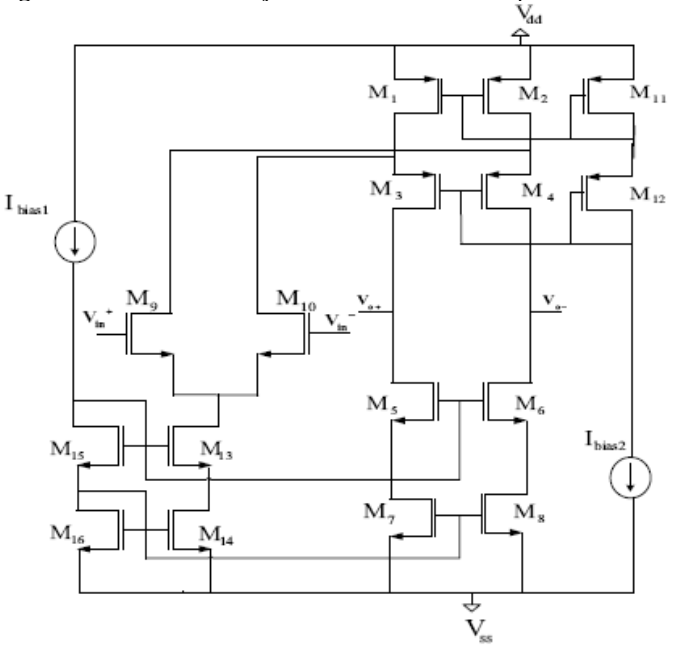

Fig. 1 A folded cascade OTA architecture

The performance specifications of circuit are tabulated in table 1. These specifications are expressed as functions of design parameters such as transistor sizes, passive values and bias conditions which must be optimized during the optimization process discussed in next section.

TABLE I
PERFORMANCE SPECIFICATIONS OF CIRCUIT

No	Specifications	Constrains	Unit
1	DC gain	> 80	db

2	Unity-gain frequency	> 200	MHz
3	CMRR	> 70	db
4	PSRR	> 70	db
5	Slew rate	> 100	V/□s
6	Phase margin	> 50	°
7	Power consumption	< 3	mw

IV. OPTIMIZATION SYSTEM

The purpose of optimization is to achieve the optimal size of MOS transistors (channel length and width) and bias currents of OTA circuit, in order to meet the desired specifications, which expressed in last section. For this purpose; a PSO algorithm was written in MATLAB which has been linked with an electrical simulator, HSPICE, as its performance evaluator.

The system platform is illustrated in Fig. 2.

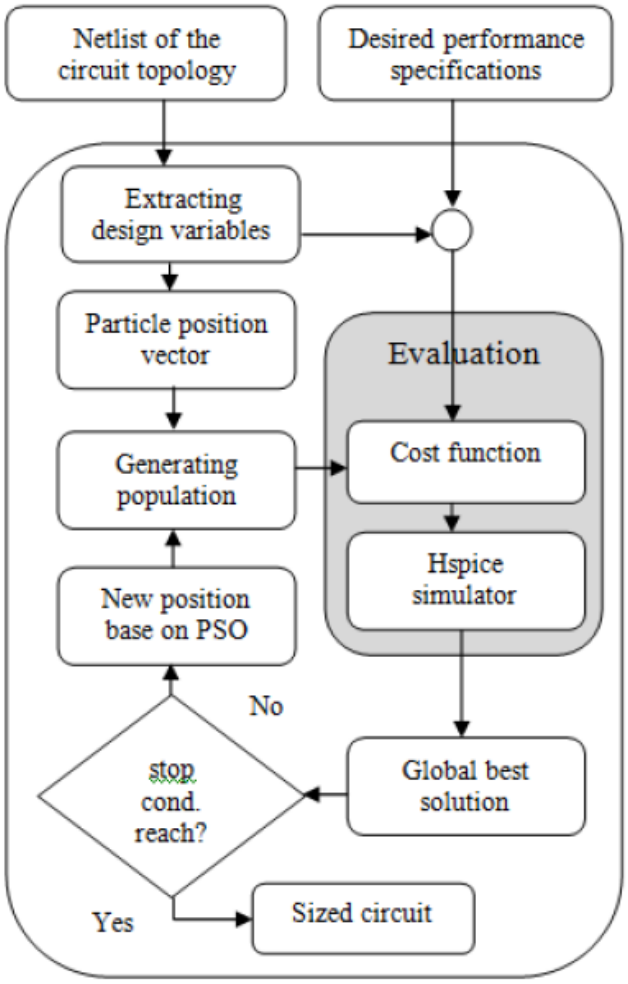

Fig. 2 The system platform

The system gets a spice netlist of OTA circuit as its inputs. Optimization is executed on a vector of design variables of circuit extracted from the netlist. In fact, the particle position vector is the channel length (L) and width (W) of MOS transistors and bias currents. At first, each particle (i-th particle) position vector is randomly initialized. In each iteration, the algorithm runs the HSPICE for each particle and evaluates a cost function (CF), described in (3):

$$CF = \prod e^{\alpha_i D_i} \quad , \alpha_i \leq 1 \qquad (3)$$

Which D_i s are the design specifications and α_i s are the importance factors that say which specification has more importance for designer regarding to different especial applications of OTA. Therefore, PB and GB are showing the minimum *CF* for best previous position and global best position respectively that each particle attempts to reach them. At the end of each iteration, GB gives the best solution of the population.

The end of the optimization process happens when a stop condition is satisfied. The stop condition can be a maximum number of iterations or the minimum variation of the cost function value (evaluation function).

V. RESULTS AND DISCUSSION

We have simulated the FCOTA using CMOS TSMC parameters for 0.35 µm mixed signal and BSIM30 version 3.1 [11]. Experiments are conducted in a Pentium IV, 2.4GHz, 4GB RAM with Windows XP Professional OS. The code is developed and implemented in MATLAB 2009a and simulations are performed in HSPICE A-2007.09.

The MOSFETS sizes obtained after optimization are presented in table 2 and the results of performance optimization of folded cascode OTA in comparison with three other works [12, 13, 14], are listed in table 3. Spice simulation results of the gain, CMRR and PSRR are depicted in fig. 2, 3 and 4 respectively.

TABLE II
OPTIMAL DEVICE SIZING

Specifications	**values**
Technology	0.35 µm AMS
Voltage supply	1.8
$(W/L)_1$	50.00/1.00
$(W/L)_3$	33.00/1.00
$(W/L)_5$	50.00/1.00
$(W/L)_9$	50.00/1.00

This comparative study shows that the PSO gives better results than the gm/Id methodology [12, 13]. The efficiency and the convergence of PSO in comparison with other evolutionary technique (SACSES [14]) can be clearly seen, especially, when we deal with more complexes optimization problems containing more variables and constraints. According to the results presented at Fig. 3, 4 and 5, we notice that simulation results are in good agreement with those obtained using PSO.

TABLE III
OPTIMIZATION RESULTS AND COMPARISON

Specifications	**This work**	**[12]**	**[13]**	**[14]**
DC gain	84.33	82.89	77.53	75.5
Unity-gain frequency	543.3	533.55	430	110
CMRR	95.6	93.56	114	94
PSRR	84.37	73.23	46.5	
Slew rate	534		196	60.9
Phase margin	51.34	43	58	69
Power consumption	1.2		6.6	1.9

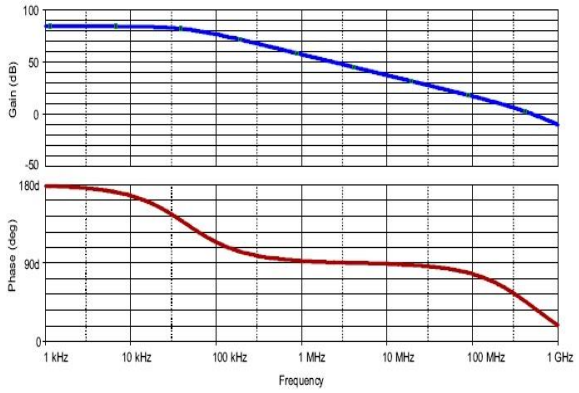

Fig. 3 Gain and phase of FC OTA vs. frequency

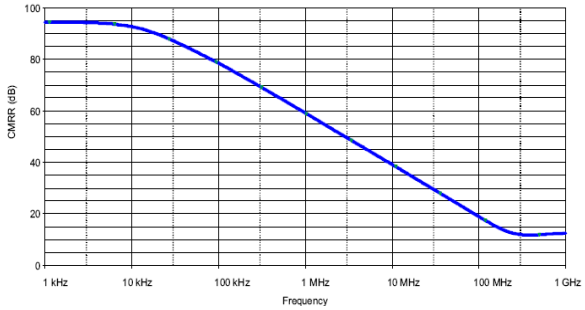

Fig. 4 CMRR of FC OTA vs. frequency

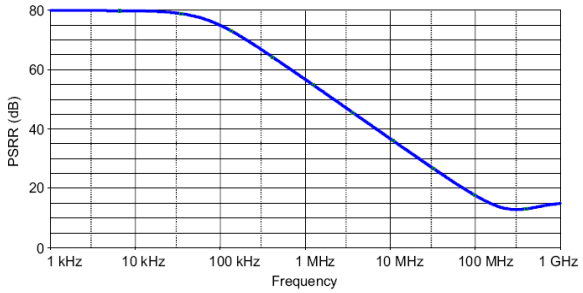

Fig. 5 PSRR of FC OTA vs. frequency

VI. CONCLUSIONS

In this paper, a PSO based approach for optimal design of folded cascode OTA circuit has been reported. Electrical specifications of the FC OTA circuit considered in the optimization process are the gain, unity gain frequency, common mode rejection ratio, power supply rejection ratio, slew rate, phase margin and power consumption. The results of this work indicate the effectiveness of this optimization approach that is a time consuming method.

We note that this approach can also be applied to optimize other circuit and can be embedded into any electronic CAD software which improves the process of design and fabrication.

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