Volume 3, Issue 5, May 2013 ISSN: 2277 128X
International Journal of Advanced Research in Computer Science and Software Engineering
Research Paper
Available online at: www.ijarcsse.com

A NEW APPROACH FOR Leakage Power Reduction Techniques in Deep Submicron Technologies in CMOS CIRCUIT for VLSI Applications

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Abstract— -In CMOS circuits, the reduction of the threshold voltage due to voltage scaling leads to increase in sub threshold leakage current and hence, static power dissipation. For the most recent CMOS feature sizes (e.g., 45nm and 65nm), leakage power dissipation has become an overriding concern for VLSI circuit designers. ITRS reports that leakage power dissipation may come to dominate total power consumption [1]. In the nanometer technology regime, power dissipation and process parameter variations have emerged as major design considerations. These problems continue to grow with leakage power becoming a dominant form of power consumption. Leakage power dissipation is projected to grow exponentially in the next decade according to the International Technology Roadmap for Semiconductors (ITRS). This directly affects portable battery operated devices such as cellular phones and PDAs since they have long idle times. Several techniques at circuit level and process level are used to efficiently minimize leakage current which lead to minimize the power loss and prolong the battery life in idle mode. A novel approach, named "Zigzag with keeper," was proposed at circuit level for the reduction of power dissipation. Zigzag with keeper incorporate the traditional zigzag approach and sleep keeper approach which use the sleep transistor plus two additional transistors driven by already calculated output which retain the state of the circuit during the sleep mode while maintaining the state or state retention.

Keywords— Power, Sub-threshold Leakage, Gate oxide Tunneling Leakage, Zigzag with keeper.

1. INTRODUCTION

Power consumption is one of the top issues of VLSI circuit design, for which CMOS is the primary technology. Today's focus on low power is not only because of the recent growing demands of mobile applications. Even before the mobile era, power consumption has been a fundamental problem. To solve the power dissipation problem, many researchers have proposed different ideas from the device level to the architectural level and above. However, there is no universal way to avoid tradeoffs between power, delay and area and thus, designers are required to choose appropriate techniques that satisfy application and product needs. In order to achieve high density and high performance, CMOS technology feature size and threshold voltage have been scaling down for decades. Because of this technology trend, transistor leakage power has increased exponentially. As the feature size becomes smaller, shorter channel lengths result in increased sub-threshold leakage current through a transistor when it is off. Low threshold voltage also results in increased sub-threshold leakage current because transistors cannot be turned off completely. For these reasons, static power consumption, i.e., leakage power dissipation, has become a significant portion of total power consumption for current and future silicon technologies. There are several VLSI techniques to reduce leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limit the application of each technique. We propose a new approach, thus providing a new choice to low-leakage power VLSI designers. Previous techniques are summarized and compared with our new approach presented in this paper. Generally static leakage power consists of gate oxide leakage and sub-threshold leakage [2]. Currently sub-threshold leakage seems to be the main contribution factor as compare to all type of leakage power [8].

Sub-threshold leakage current flows between the source and drain of an MOS transistor when the gate voltage is less than the threshold voltage shown in figure 2.1. Sub-threshold indicates how effectively a transistor can be turned off when gate voltage is below the threshold voltage. Reverse biasing substrate to source junction increases threshold voltage thereby reducing the sub-threshold current. In short channel devices, the depleted source and drain regions interact with each other reducing the potential barrier, thereby reducing the threshold voltage which increases the sub-threshold leakage current. Sub-threshold current is given by the equation

$$I_{ds} = \mu_{O*} \ C_{OX*} \ W/L_* \ (m-1)_* \ (V_{th})^2 * e^{\frac{Vgs-Vth}{(m-Vt)}} * (1-e^{-Vds/Vt})$$

Where $m = 1 + C_{dm}/C_{ox}$, m is the sub-threshold swing co-efficient, C_{dm} is capacitance of the depletion layer, C_{ox} is the capacitance of the oxide layer, μ_0 is the mobility, V_{th} is the threshold voltage, V_{gs} is the gate to source voltage, V_{ds} is the drain to source voltage and V_t is the thermal voltage. ***Gate Oxide Tunneling*** **Leakage,** scaling down the gate oxide

thickness increases electric field across the gate. The high electric field causes electrons to tunnel from gate to substrate and substrate to gate resulting in gate oxide leakage current. In any case aim of this thesis is reducing the sub-threshold leakage. According to technology trend for the high density the transistor size should be scale down and for high performance the threshold voltage (V_{th}) scaling down. In the case of sub-threshold leakage if scaling down of V_{th}, the leakage power increase exponentially as V_{th} decrease and the short channel effect the channel controlled by drain. But in case of gate oxide leakage gate tunneling due to thin oxide and high k-dielectric could be possible solution and another motivation leakage power reduction technique can potentially increase the battery life. With application of dual threshold voltage (V_{th}) techniques the sleep, zigzag and sleepy stack approaches result in orders of magnitude sub-threshold leakage power reduction.

The major advantage of the zigzag with keeper approach over the sleepy keeper and zigzag approaches is that the zigzag with keeper approach saves exact logic state. Our main aim of getting advantage as compare to sleep, stack, leakage feedback, sleepy stack, and sleepy keeper with zigzag with keeper approach is to reduce power dissipation. For comparing the power dissipation of different existing approach and process technologies MICROWIND software is used.

2. BACKGROUND WORK

This chapter reviews the previously proposed circuit level approach. In order to compare with the zigzag with keeper approach, this section explains several previous leakage reduction approaches: sleep, stack, sleepy stack, and leakage feedback, zigzag and sleep keeper.

2.1 BASE APPROACH

It is a traditional approach. All the schematic and layout are designed by using MICROWIND software. First of all we explain the transistor size that means transistor size are specified ratio of W/L. In this software the smallest possible transistor size is 45nm means 50nm technology having the width is 0.5µm and length is 0.05µm .The ratio of W/L indicates aspect ratio of transistor. In all the approach, transistor are placed between two parallel rows continuous V_{dd} and G_{nd} .Base approach is generally indicates conventional CMOS transistor. In the base approach pull-up network and pull-down network are used using few transistors. The pull-up network is called a P-MOS transistor and pull-down network is called as N-MOS transistor. Using a MICROWIND software tool we will get power dissipation at different technologies such as 45nm, 65nm, 90nm, 120nm. It is a basic fundamental approach that is used in generally all techniques.

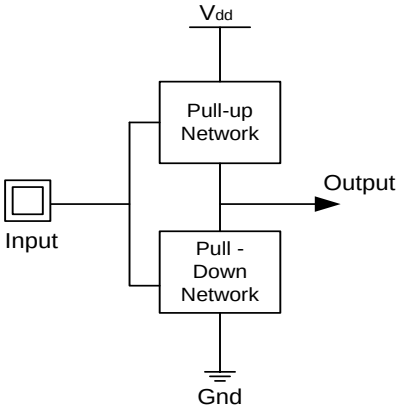


Fig.1: Base Approach

2.2 SLEEP APPROACH

The most well-known traditional approach is the sleep approach [2][3]. In the sleep approach, both (i) an additional "sleep" PMOS transistor is placed between V_{dd} and the pull-up network of a circuit and (ii) an additional "sleep" NMOS transistor is placed between the pull-down network and G_{nd}.

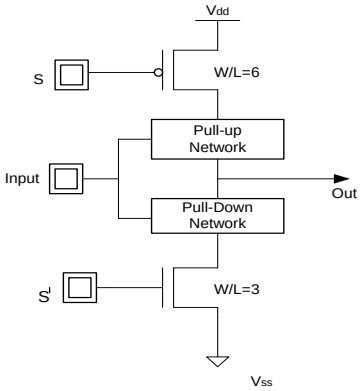


Fig.2. Sleep Approach

These sleep transistors turn off the circuit by cutting off the power rails. Figure 2 shows its structure. The sleep transistors are turned on when the circuit is active and turned off when the circuit is idle. By cutting off the power source, this technique can reduce leakage power effectively. However, output will be floating after sleep mode, so the technique results in destruction of state plus a floating output voltage. State-destructive techniques cut off transistor (pull-up or pull-down or both) networks from supply voltage or ground using sleep transistor. These types of techniques are also called gated-V_{dd} and gated- G_{nd} (note that a gated clock is generally used for dynamic power reduction).

Furthermore, the pull-up and pull-down networks will have floating values and thus will lose state during sleep mode. These floating values significantly impact the wake up time and energy of the sleep technique due to the requirement to recharge transistors which lost state during sleep (this issue is nontrivial, especially for registers and flip-flops). Using a MICROWIND software tool we get power dissipation at different technologies such as 45nm, 65nm, 90nm, 120nm.Figure 1 shows its structure. The sleep transistors are turned on when the circuit is active and turned off when the circuit is idle. By cutting off the power source, this technique can reduce leakage power effectively. However, output will be floating after sleep mode, so the technique results in destruction of state plus a floating output voltage.

2.3 ZIGZAG APPROACH

The zigzag technique in Figure 3 uses one sleep transistor in each logic stage either in the pull-up or pull-down network according a particular input pattern [4]. Input vector that can achieve the lowest possible leakage power consumption. Then, we either assign a sleep transistor to the pull-down network if the output is '1' or else assign a sleep transistor to the pull-up network if the output is '0.' For Figure 3, we assume that the output of the first stage is '1' and the output of the second stage is '0' when minimum leakage inputs are asserted. Therefore, we apply a pull-down sleep transistor for the first stage and a pull-up sleep transistor for the second stage. Similar to the sleep transistor technique, we size the sleep transistors to the size of the largest transistor in the network (pull-up or pull-down) connected to the sleep transistor. If dual-Vth values are available, high-Vth transistors are use for the sleep transistors. To reduce the wake-up cost of the sleep transistor technique, the zigzag technique is introduced. The zigzag technique reduces the wake-up overhead by choosing a particular circuit state (e.g., corresponding to a "reset") and then, for the exact circuit state chosen, turning off the pull-down network for each gate whose output is high while conversely turning off the pull-up network for each gate whose output is low. By applying, prior to going to sleep, the particular input pattern chosen prior to chip fabrication, the zigzag technique can prevent floating.

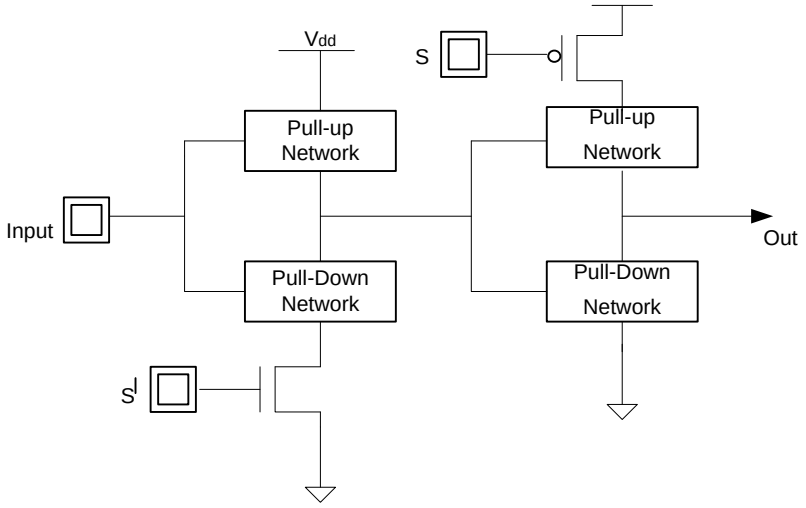


Fig.3. Zigzag Approach

Although the zigzag technique retains the particular state chosen prior to chip fabrication, any other arbitrary state during regular operation is lost in power-down mode. Although the zigzag technique can reduce wake-up cost, the zigzag technique still loses state. Thus, any particular state (from prior to going to sleep) which is needed upon wakeup must be regenerated somehow. Also, the zigzag technique may need extra circuitry to generate a specific input vector (in case reset values are not used for the sleep mode input vector).In this approach MICROWIND software are used for analysis of the power dissipation with the help of layout and schematic using process technology such as 45nm, 65nm, 90nm, 120nm.

2.4 STACK APPROACH

Another technique for leakage power reduction is the stack approach, which forces a stack effect by breaking down an existing transistor into two half size transistors [5]. Shows 4 its structure. When the two transistors are turned off together, induced reverse bias between the two transistors results in sub threshold leakage current reduction. However, divided transistors increase delay significantly and could limit the usefulness of the approach. The sleepy stack approach combines the sleep and stack approaches.

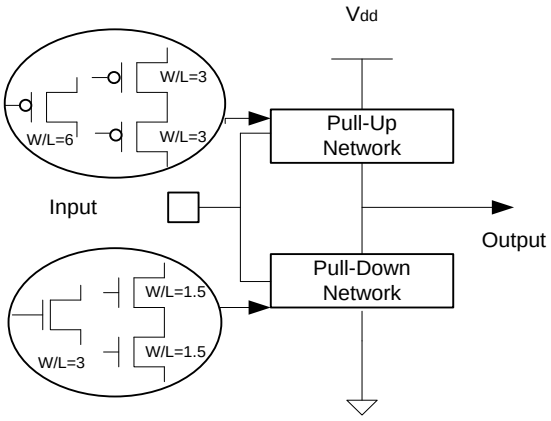


Fig.4 Stack Approach

2.5 SLEEPY STACK APPROACH

The sleepy stack technique divides existing transistors into two half size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors [5]. Figure 5 shows its structure. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Each sleep transistor, placed in parallel to the one of the stacked transistors, reduces resistance of the path, so delay is decreased during active mode. However, area penalty is a significant matter for this approach since every transistor is replaced by three transistors and since additional wires are added for S and S', which are sleep signals.

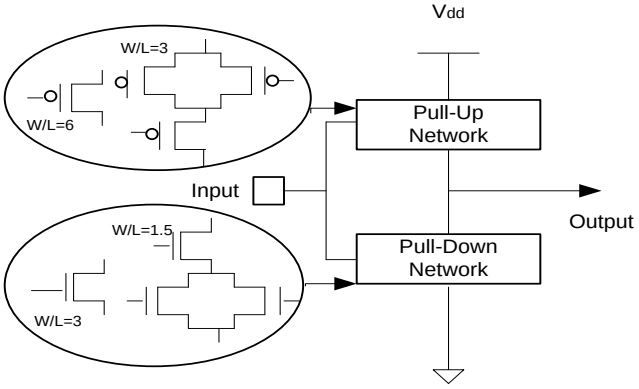


Fig.5. Sleepy Stack Approach

2.6 LEAKAGE FEEDBACK APPROACH

The leakage feedback approach is based on the sleep approach. However, the leakage feedback approach uses two additional transistors to maintain logic state during sleep mode, and the two transistors are driven by the output of an inverter which is driven by output of the circuit implemented utilizing leakage feedback [14]. As shown in Figure 6, a PMOS transistor is placed in parallel to the sleep transistor (S) and a NMOS transistor is placed in parallel to the sleep transistor (S'). The two transistors are driven by the output of the inverter which is driven by the output of the circuit. During sleep mode, sleep transistors are turned off and one of the transistors in parallel to the sleep transistors keep the connection with the appropriate power rail. For the sleep, zigzag, sleepy stack and leakage feedback approaches, dual Vth technology can be applied to obtain greater leakage power reduction. Since high-Vth results in less leakage but lowers performance, high-Vth is applied only to leakage reduction transistors, which are sleep transistors, and any transistors in parallel to the sleep transistors; on the other hand, low-Vth is applied to the remaining transistors to maintain logic performance [2]-[7]

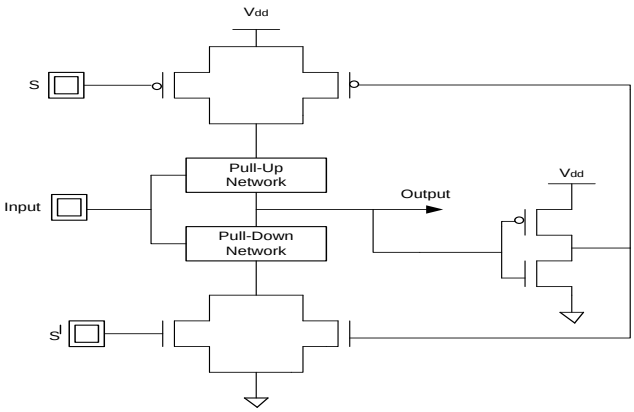


Fig.6. Leakage feedback approach

2.7 SLEEPY KEEPER APPROACH

In this section, we describe leakage reduction technique, which we call the "sleepy keeper" approach. This section explains the structure of the sleepy keeper approach [10] as well as how it operates. The basic problem with traditional CMOS is that the transistors are used only in their most efficient, and naturally inverting, way: namely, PMOS transistors connect to V_{dd} and NMOS transistors connect to G_{nd} .It is well known that PMOS transistors are not efficient at passing G_{nd} ; similarly, it is well known that NMOS transistors are not efficient at passing V_{dd} . However, to maintain a value of '1' in sleep mode, given that the '1' value has already been calculated, the sleepy keeper approach uses this output value of '1' and an NMOS transistor connected to V_{dd} to maintain output value equal to '1' when in sleep mode. As shown in Figure.7,

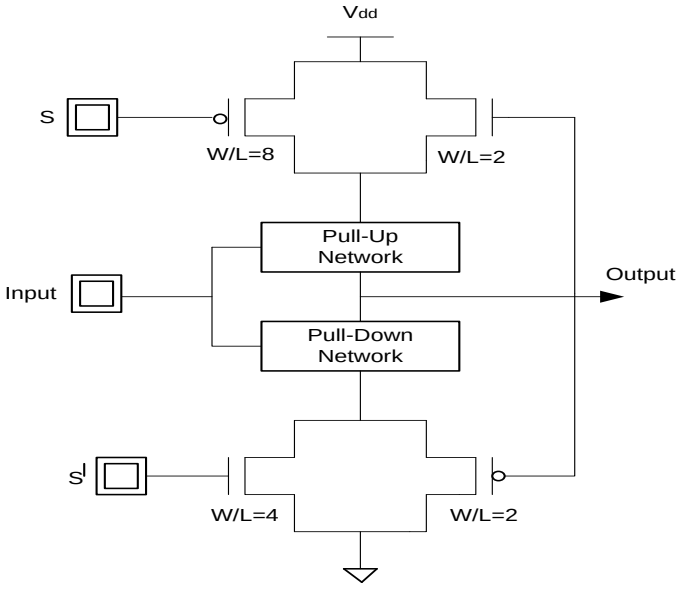


Fig.7. Sleepy Keeper Approach

3. Proposed Work

Zigzag With Keeper Structure

In this chapter, introducing new leakage power reduction technique named as "zigzag with keeper". Zigzag with keeper incorporates the traditional zigzag approach and sleep keeper approach which use the sleep transistor plus two additional transistors driven by already calculated output –which retain the state of the circuit during the sleep mode while maintaining the state or state retention. Therefore, far better than any prior approach known to this thesis, the zigzag with keeper technique can achieve ultra-low leakage power consumption while saving state. We first explain the structure of the zigzag with keeper technique using an inverter as shown in figure 4.1. Then we describe the details of zigzag with keeper operation in active mode and sleep mode.

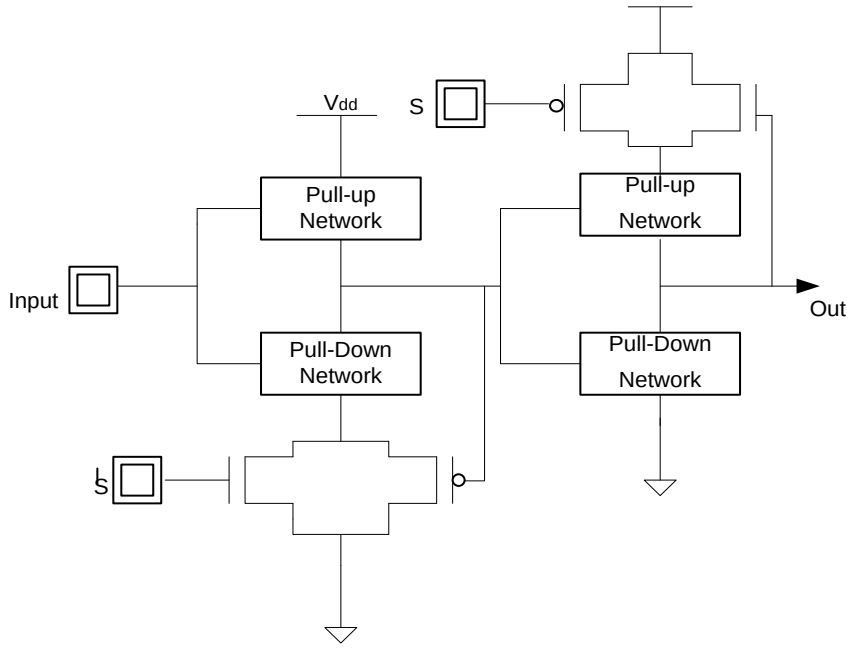


Fig.9. Zigzag with Keeper Approach

Zigzag With Keeper Operation

In case of base approach no direct path occur from power rail to ground because it is a inversely behave such as V_{dd} is connected to PMOS transistor and NMOS transistor is connected to ground and if the input = '0' then output ='1' means PMOS transistor is turned on and NMOS transistor is turned off similarly if the input ='1' then output = '0' means PMOS transistor is turned off and NMOS transistor is turned on. However, to maintain a value '1' in sleep mode. A variation of the sleep approach, the zigzag approach reduces wake up caused by sleep transistor. Sleep transistor is added in base approach according to given logic value. It may be logic '0' or '1' value at the input of base approach. If the input ='0' then output ='1'. In this case PMOS transistor (pull-up) is turned on and NMOS transistor (pull down) is turned off, so the sleep(S') NMOS transistor always add in turnoff side means connect between pull-down network and ground of the first chain inverter but maintaining a value '1' in sleep mode, additional PMOS transistor is added to parallel with sleep (S') NMOS transistor. For the second chain inverter if the input = '1' then output = '0'. In this case PMOS transistor (pull-up) is turned off and NMOS transistor (pull down) is turned on so the sleep(S) PMOS transistor always added in turn off side means connect between power rail and pull-up network but maintaining a value '0' in sleep mode, additional NMOS transistor is added to parallel with sleep(S)PMOS transistor. During the active mode (s=0 and s'=1), the sleep transistors are turned on so it is reducing delay and during the sleep mode (s=1 and s'=0), the sleep transistor are turned off so it is saved state. MICROWIND software is used for this approach to analysis of power dissipation at different technologies such as 45nm, 65nm, 90nm, and 120nm at a given power supply according to technologies.

4. Simulation Results

We estimates only the power dissipation for eight design approaches i.e. the base case, sleep, zigzag, stack, sleepy stack, leakage feedback and sleepy keeper approaches with newly proposed approaches named "Zigzag with keeper". To compare our Zigzag with keeper approach to the other considered approaches for four different technologies by using MICROWIND software. The simulations table for Power Dissipation is shown below.

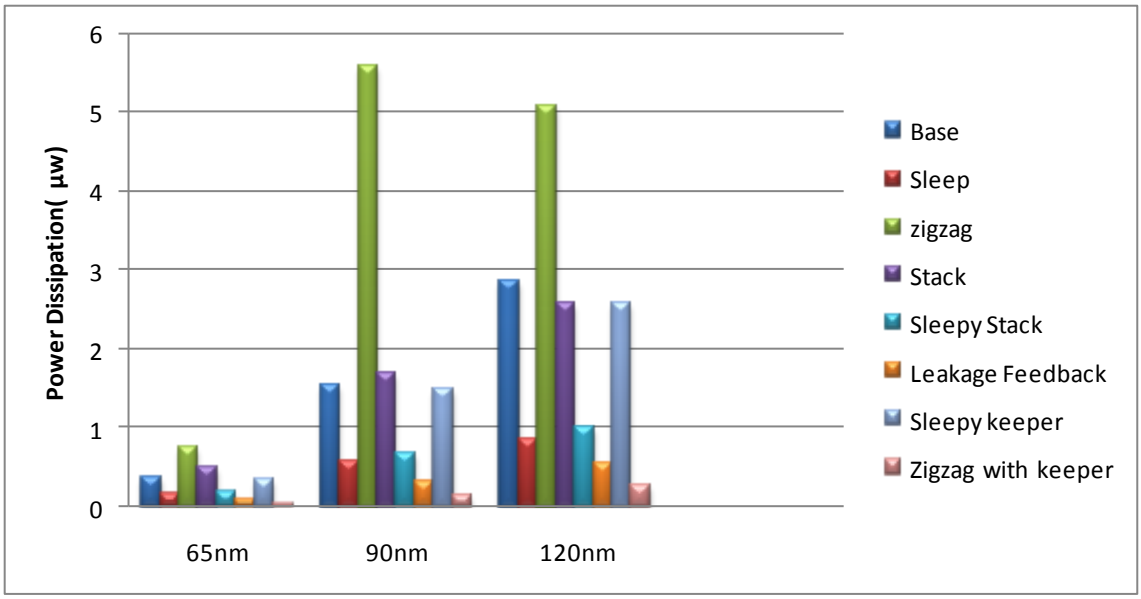
Simulation results for power dissipation

Techniques	45nm	65nm	90nm	120nm
Base case	0.086µw	0.373 µw	1.546 µw	2.859 µw
Sleep	0.040 µw	0.168 µw	0.573 µw	0.856 µw
Zigzag	0.168 µw	0.754 µw	5.579 µw	5.094 µw
Stack	0.118 µw	0.503 µw	1.689 µw	2.581 µw
Sleepy stack	0.045 µw	0.189 µw	0.664 µw	1.000 µw
Leakage Feedback	0.023 µw	0.099 µw	0.318 µw	0.560 µw
Sleepy keeper	0.085 µw	0.359 µw	1.495uw	2.567uw
Zigzag with keeper	0.011 µw	0.049 µw	0.155 µw	0.276 µw

Table.2 Power Dissipation (µw) among various approaches

Showing the simulation results of circuit with four different technology at a given standard power supply for all above discussed eight techniques i.e. base case, sleep, zigzag, stack, sleepy stack, leakage-feedback and sleepy keeper approaches with newly proposed approaches zigzag with keeper. The simulation result shows zigzag with keeper approach is having the least power dissipation as compared to all the discussed approach.

The power Dissipation is decreasing as the process technology scaled down. The result can be better explained in the form of graphs given below.



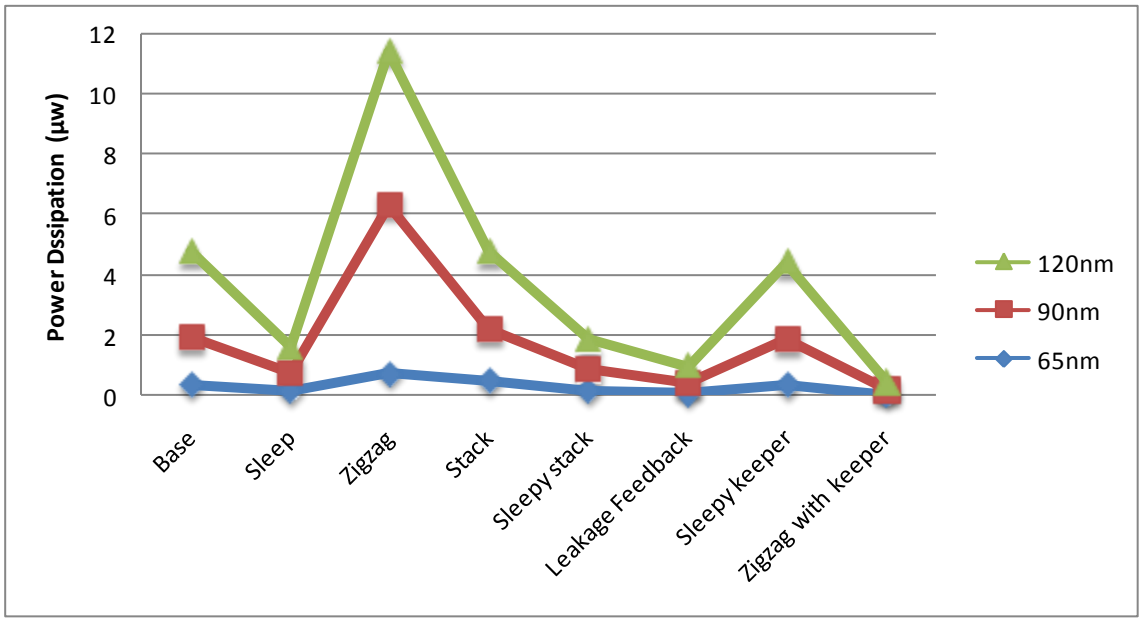


Fig.10. Power Dissipation Chart for Rest Technologies.

5. Conclusion

In nanometre scale CMOS technology, sub-threshold leakage power consumption is a great challenge. Although previous approaches are effective in some ways, no perfect solution for reducing power consumption is yet known. Therefore, designers choose techniques base upon technology and design criteria. Scaling down of device dimensions, supply voltage and threshold voltage for achieving high performance and low dynamic power dissipation has largely contributed to the increase in leakage power dissipation. We have presented an efficient design methodology for reducing the power dissipation in VLSI design.

The proposed technique in the thesis is "ZIGZAG WITH KEEPER "and comparing the power consumption with other existing techniques. The proposed technique is more effective in reducing power consumption. The result is simulated with MICROWIND software and compare at different technology 45nm, 65nm, 90nm and 120nm.

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