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Leakage Current Minimization in Domino Circuits Using Sleep Switch

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Abstract— ***A new circuit technique is proposed in this literature to simultaneously reduce sub-threshold leakage as well as gate-oxide leakage power consumption at high and low temperatures in footed domino logic circuits in ultra-deep submicron technology, as gate leakage is dominant for ultra thin gate insulating layer (i.e. tox > 20Å). Here we are using the dual threshold voltage technique to reduce the leakage current as well as propagation delay and sleep switches to further reduce leakage current. At 110ºC, proposed Circuit I & proposed Circuit II work improves 34%-70% as compared to multiple-Vt with low and high inputs. At room temperatures, proposed work improves 20%-57% as compared to multiple-Vt with low and high inputs.***

Keywords— Dual-Vt, Footed Domino logic, Gate-Oxide Leakage Current, Sub-threshold Leakage Current.

I. INTRODUCTION

For high-speed chip performance domino circuits are employed and can be classified into footerless and footed domino [1-3]. For better timing characteristics footed domino is used because here the footer transistor isolates the pull-down network (PDN) from ground preventing the change in the state of the dynamic node by PDN during precharge phase. In addition if the footer transistor is omitted, the footerless domino reduces both the circuit evaluation delay and the power consumption. . Having different characteristics, the footerless and footed domino based domino circuits both are extensively in high performance processors. For multistage domino circuits, the first stage is typically kept footed and others are footerless [3]. High leakage current in nanometer regime becomes a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length, and gate oxide thickness are reduced. Consequently, the identification and modeling of different leakage components is very important for estimation and reduction of leakage power, especially for low-power applications. Leakage power depends on gate length and oxide thickness and it varies exponentially with threshold voltage and other parameters. Reduction of supply voltages and threshold voltages for MOS transistors helps to reduce dynamic power dissipation but simultaneously leakage power increases. Leakage mechanism includes the following:

Subthreshold leakage current **(I_{sub})** in MOS transistors, which occurs when the gate voltage is below the threshold voltage and mainly, consists of diffusion current. Off-state leakage in present-day devices is usually dominated by this type of leakage. An effect called drain-induced barrier lowering (DIBL) takes place when a high-drain voltage is applied to a short channel device. The source injects carriers into the channel surface (independent of gate voltage). Narrow width of the transistor can also modulate the threshold voltage and the subthreshold current.

$$I_{sub} = \mu_0 . C_{ox} . \frac{W}{L} . V^2 . e^{1.8} . e^{\frac{(V_{gs} - V_T)}{nV}} \qquad (1.1)$$

where, μ_0 is the zero bias mobility, C_{ox} is the gate oxide capacitance, and (W/L) represents the width to the length ratio of the leaking MOS device. The variable V in equation 1.1 is the thermal voltage constant, and V_{gs} represents the gate to the source voltage. The parameter n in equation 1.1 is the sub-threshold swing coefficient given by $1 + (C_d/C_{ox})$ with C_d being the depletion layer capacitance of the source/drain junction. One important point about equation 1.1 is that the sub threshold leakage current is exponentially proportional to $(V_{gs}-V_T)$. Shorter channel length results in lower threshold voltages and increases subthreshold leakage. As temperature increases, subthreshold leakage is also increased. On the other hand, when the well-to-source junction of a MOSFET is reverse biased, there is a body effect that increases the threshold voltage and decreases subthreshold leakage.

Gate oxide tunneling current **(I_{gate})** in which tunneling of electrons that can result in leakage when there is a high electric field across a thin gate oxide layer. Electrons may tunnel into the conduction band of the oxide layer; this is called Fowler-Nordheim tunneling. In oxide layers less than 3-4 nm thick, there can also be direct tunneling through the silicon oxide layer. Mechanisms for direct tunneling include electron tunneling in the conduction band, electron tunneling in the valence band, and hole tunneling in the valence band.

Junction leakage that results from minority carrier diffusion and drift near the edge of depletion regions, and also from generation of electron hole pairs in the depletion regions of reverse-bias junctions. When both n regions and p regions are heavily doped, as is the case for some advanced MOSFETs, there is also junction leakage due to band-to-band tunneling (BTBT).

Hot-carrier injection occurs in short-channel transistors. Because of a strong electric field near the silicon/silicon oxide interface, electrons or holes can gain enough energy to cross the interface and enter the oxide layer. Injection of electrons is more likely to occur, since they have a lower effective mass and barrier height than holes.

Gate-induced drain leakage (GIDL), which is caused by high field effect in the drain junction of MOS transistors. In a negative- channel metal-oxide-semiconductor (NMOS) transistor, when the gate is biased to form accumulation layer in the silicon surface under the gate, the silicon surface has almost the same potential as the p-type substrate, and the surface acts like a p region more heavily doped than the substrate. When the gate is at zero or negative voltage and the drain is at the supply voltage level, there can be a dramatic increase of effects like avalanche multiplication and band-to-band tunneling. Minority carriers underneath the gate are swept to the substrate, completing the GIDL path. Thinner oxide and higher supply voltage increase GIDL.

Punch through leakage, which occurs when there is decreased separation between depletion regions at the drain-substrate and the source-substrate junctions. This occurs in short-channel devices, where this separation is relatively small. Increased reverse bias across the junctions further decreases the separation. When the depletion regions merge, majority carriers in the source enter into the substrate and get collected by the drain, and punch through takes place.

In this paper, we study the sources of leakage current in dual-threshold (dual-V_t) domino and show that I_{sub} and I_{gate} are actually a function of not only inputs applied but also dependent on the clock signal state. The remainder of the paper is organized as follows. In the next section Leakage current characteristic comparison of P-channel and N-channel devices. In Section 3 proposed I & proposed II low leakage domino circuit is explained. Simulation results are given in Section 4. Finally the conclusions are offered in Section 5.

II. Leakage current characteristic comparison of P-channel and N-channel devices

Maximum gate oxide leakage and sub threshold leakage currents produced by PMOS and NMOS is shown in Figure 1. In Figure 1(a) four components of I_{gate} are shown: Gate to channel tunneling current (I_{gc}), gate-to-source tunneling current (I_{gs}), gate-to-drain tunneling current (I_{gd}) and gate-to-body tunneling current (I_{gb}) [4]. $I_{gs\ and}$ I_{gd} are the edge tunneling currents from gate to source and drain terminals respectively, through the gate-to-source and gate-to-drain overlap areas. I_{gc} is shared between source and drain terminals [5]. I_{gb} is smaller than the other three components of gate tunneling current and it is typically several orders of magnitude.

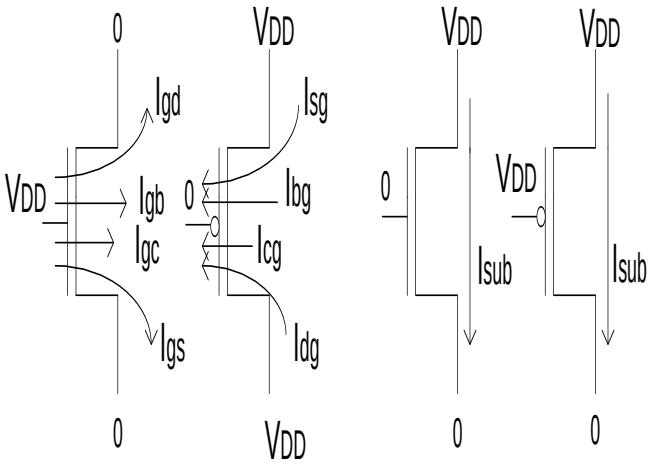

Fig.1.(a) Fig.1.(b)

Figure 1. State of maximum gate oxide and subthresold leakage current, in NMOS and PMOS transistors.(a) Maximum gate oxide leakage current state. (b) Maximum subthresold leakage current state.

As shown in Figure 1(a) maximum gate oxide leakage current flows when the transistor is turned ON and maximum potential difference between gate-to-source and gate-to-drain terminals. As shown in Figure 1(b) maximum sub threshold leakage current flows when the transistor is turned OFF and maximum the potential difference between source and drain terminals.

A comparison of normalized gate oxide and subthreshold leakage currents produced by NMOS and PMOS transistors for low-V_t and high-V_t in a 65nm dual-V_t CMOS technology is listed in Table 1. The data are measured for low and high die temperatures.

Table 1. Normalized gate oxide and subthreshold leakage currents for NMOS and PMOS (low-V_t and high-V_t) transistors at low and high die temperatures.

	NMOS Transistor		PMOS Transistor	
	Low-V_t	High-V_t	Low-V_t	High-V_t
I_{sub} (110^0C)	1.53	1.98	1.16	1
I_{gate} (110^0C)	.89	.098	.011	.0003
I_{sub} (25^0C)	1.18	1.41	1.17	1
I_{gate} (25^0C)	2.61	.29	.036	.0011

Transistor Length = 65nm, Width = 1µm, Low-V_t = 0.22V, High-V_t = 0.423V, V_{DD} = 1V. For each temperature, leakage currents are normalized by subthreshold leakage current produced by a high-V_t PMOS transistor.

Firstly, the I_{gate} produced by a low-V_t NMOS is 81x and 72.5x higher than the I_{gate} produced by a low-V_t PMOS at 110^0C and 25^0C respectively, as illustrated in Table 1. It shows that the probability of hole tunneling is much smaller than the probability of electron tunneling through the gate insulator. Therefore, the I_{gate} produced by a PMOS device is much smaller than the I_{gate} produced by a NMOS device with similar physical dimensions (width, length and t_{ox}) in a 65 nm technology and at the same potential difference across the gate insulator.

Secondly, the I_{gate} produced by a low-V_t NMOS is 9.1x at 110^0C and 9x at 25^0C higher than I_{gate} by a high-V_t NMOS transistor. Relatively higher gate tunneling barrier for the electrons is exploited in this paper by using a high-V_t NMOS transistor at the input of a domino circuits to reduce the gate oxide leakage current overhead of the proposed dual-V_t domino circuit technique.

III. Leakage Power Analysis of Domino Footed AND - OR circuit

Proposed Circuit-I

A high-V_t pMOS pull-up feedback transistor M8 is employed between the power supply and footer node (X) and its gate is connected to the dynamic node is shown in Fig.2. Keeper gate is directly connected to the output of the domino circuit. Removing the inverter between keeper and dynamic node reduces both leakage current and area. In the standby mode, clock is gated high, turning off the high-V_t pull up transistor M1. When all the inputs are low (CHIL), all the transistors of the pull down network are turned off, dynamic node is maintained high and output node of the circuit is low. High dynamic node turns off transistor (M8), creates a small voltage at node (X) nearly to $|V_{tp}|$ of high-V_t PMOS transistor. There is exponential reduction in the leakage current due to negative bulk to source voltage of the pull down network and increase in the threshold voltage of the pull down network. There is also exponential decrease in the subthreshold leakage current due to reduction of gate-to-source voltage. Leakage currents of the circuit are modeled as

$$I_{sub} = W_{PDN} \cdot J_{SPDN} + W_{M8} \cdot J_{SHP} + W_{M3} \cdot J_{SLP} \qquad (2.1)$$

$$I_{gate} = W_{PDN} \cdot J_{GRLN} + W_{M4} \cdot J_{GFHN} + W_{M5} \cdot J_{GFLN} + W_{M8} \cdot J_{GFHP} + W_{M3} \cdot J_{GFLP} + W_{M2} \cdot J_{GRHP} \qquad (2.2)$$

Where J_{SLP}, J_{SHP}, J_{GFLN}, J_{GFHN}, J_{GFLP}, J_{GFHP} and J_{GRLP} are subthreshold leakage current per width unit of low-V_t and high-V_t of pMOS, forward and reverse gate oxide leakage current density per width unit of low-V_t and high-V_t of nMOS and pMOS.

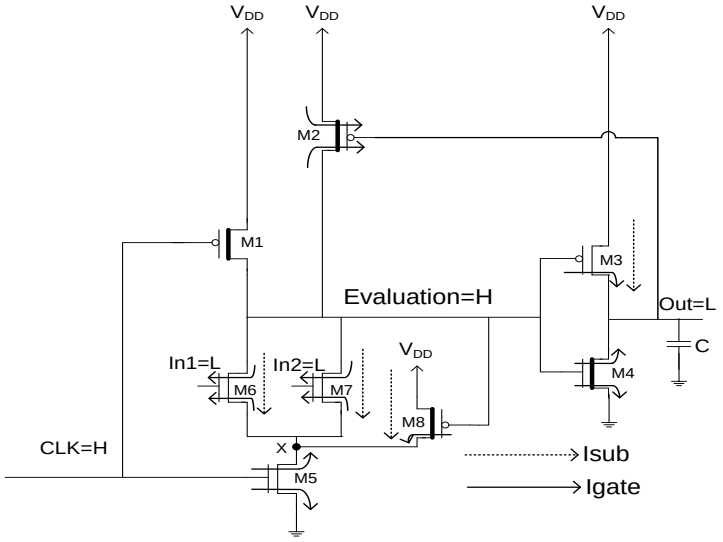

Figure. 2 Variation of subthreshold and gate oxide leakage current conduction path in proposed circuit1.

Proposed Circuit II

Three high-V_t sleep switch transistors M5, M7 and M8 are added to the standard dual-V_t footed domino gate to force the dynamic and output node into high voltage as shown in Fig.3. By adding the high-V_t transistor M5 in series with M4, speed of the circuit reduces. In active mode, sleep signal is set high and CLK2 is similar to CLK, sleep transistors M7 and M8 are cut-off and transistor M5 is ON. The proposed circuit works like standard dual-V_t footed domino gate.

In standby mode, CLK is gated high and CLK2 is gated low, M1 and M6 are cuts off. Sleep signal is set low voltage, sleep transistors M7 and M8 are turned ON and transistor M5 OFF. Sleep transistor M8 provides high voltage at output node. A high-V_t NMOS sleep transistor M5 is employed in series with M4 in order to eliminate the static DC current path through M8 and M4. A high-V_t PMOS sleep transistor M7 is employed between power supply and footer node N. When all inputs are high (CHIH state), dynamic node is remains high. Sleep transistor M7 provides high voltage at footer node N and its avoids both subthreshold and gate oxide leakage current in the pull down network. Gate oxide leakage current of transistor M1, M2, M3 and M4 are neglected because all terminals of these transistors have same potential. Leakage currents of the circuit are modeled as

$$I_{sub} = W_{M2} \cdot J_{SHP} + W_{M5} \cdot J_{SHN} + W_{M6} \cdot J_{SLN} \quad (3.3)$$

$$I_{gate} = W_{M5} \cdot J_{GRHN} + W_{M6} \cdot J_{GRLN} + (W_{M7} + W_{M8}) \cdot J_{GRHP} \quad (3.4)$$

Where, J_{SLN}, J_{SHN} , J_{SHP}, $J_{GRLN,}$ J_{GRHN} and J_{GRHP}, are subthreshold leakage current per width unit of low-V_t and high-V_t of PMOS, forward and reverse gate oxide leakage current density per width unit of low-V_t and high-V_t of NMOS and PMOS.

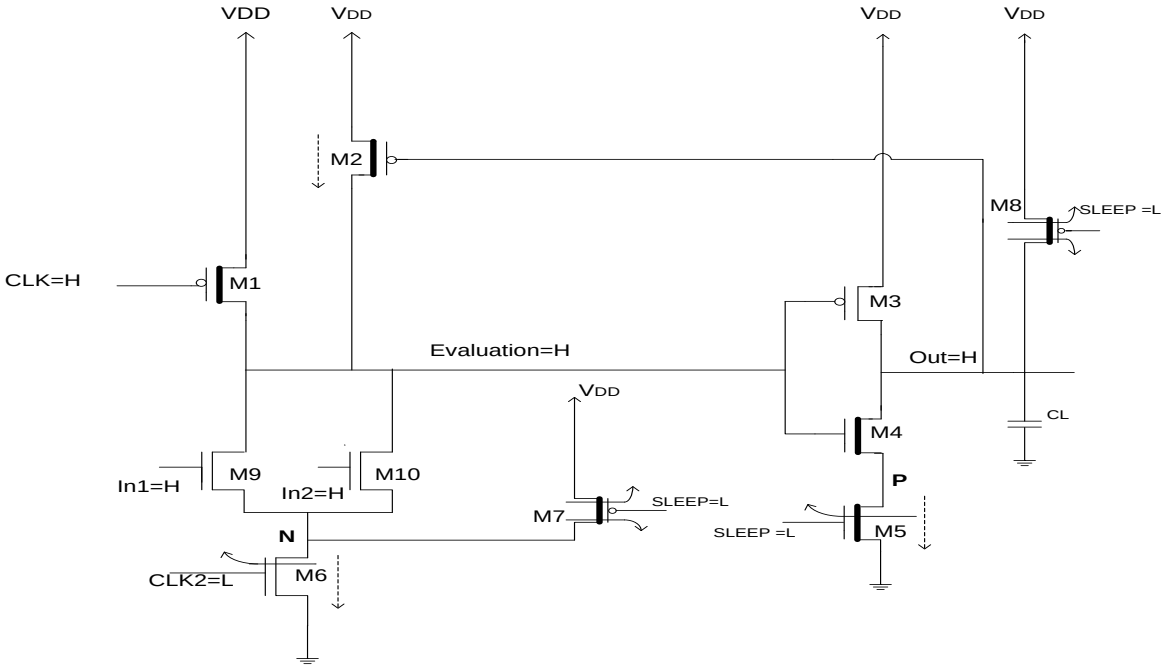

Figure 3 Variation of subthreshold and gate oxide leakage current conduction path in proposed circuit2.

IV. SIMULATION RESULTS

Result Analysis of Footed AND-OR Domino Circuits

Leakage Power Consumption at 25°C

The proposed circuit1 reduces the total leakage power consumption by 61% to 90% as compared to high inputs standard low-V_t circuits, and 54% to 88% as compared to low inputs standard low-V_t circuits. Similarly, it reduces the leakage power by 44% to 85% as compared to high inputs standard dual-V_t circuits, and 10% to 50% as compared to low inputs standard dual-V_t circuits.

The proposed circuit2 reduces the total leakage power consumption by 82% to 91% as compared to high inputs standard low-V_t circuits, and 79% to 90% as compared to low inputs standard low-V_t circuits. Similarly, it reduces the leakage power by 75% to 90% as compared to high inputs standard dual-V_t circuits, and 54% to 66% as compared to low inputs standard dual-V_t circuits. Proposed circuit2 reduces leakage power by 19% to 55% as compared to proposed circuit.

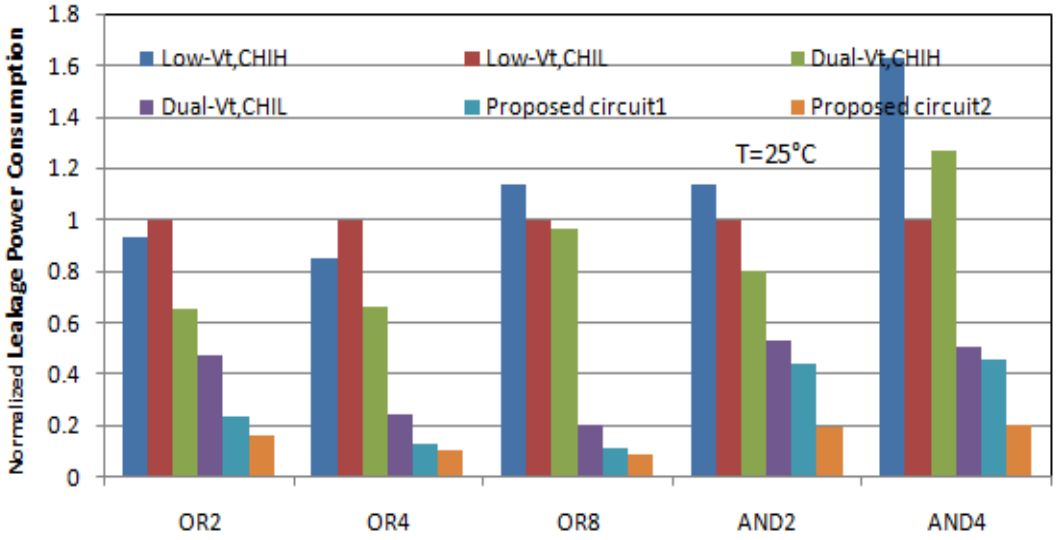

Figure 3.14 Comparison of the leakage power consumption of the proposed circuits and the existing techniques at 25°C. The leakage power consumption is normalized to the leakage power of the standard low-V_t technique with high inputs for each circuit.

Table 3.3 Total leakage power reduction (%) provided by the proposed circuit1 as compared to the existing circuit technique at 25°C.

Circuits	OR2	OR4	OR8	AND2	AND4
Low-Vt, CHIH	74.95	84.10	90.01	61.30	72.07
Low-Vt , CHIL	82.19	86.47	88.58	55.57	54.43
Dual-Vt, CHIH	64.32	79.72	85.27	44.85	64.28
Dual-Vt, CHIL	50.63	44.79	43.36	15.91	10.41

Table 3.4 Total leakage power reduction (%) provided by the proposed circuit2 as compared to the existing circuit technique and proposed circuit1 at 25°C.

Circuits	OR2	OR4	OR8	AND2	AND4
Low-Vt, CHIH	82.82	87.54	91.95	82.84	87.21
Low-Vt , CHIL	83.98	89.40	90.81	80.29	79.15
Dual-Vt, CHIH	75.54	84.11	90.49	75.54	83.65
Dual-Vt, CHIL	66.15	56.76	54.40	62.70	59.08
Proposed circuit1	31.44	21.67	19.48	55.65	54.23

Leakage Power Consumption at 110°C

The proposed circuit1 reduces the total leakage power consumption by 88% to 95% as compared to high inputs standard low-V_t circuits, 83% to 96% as compared to low inputs standard low-V_t circuits. Similarly, it reduces the leakage power by 42% to 84% as compared to high inputs standard dual-V_t circuits, and 22% to 55% as compared to low inputs standard dual-V_t circuits.

The proposed circuit2 reduces the total leakage power consumption by 94% to 95% as compared to high inputs standard low-V_t circuits, and 91% to 96% as compared to low inputs standard low-V_t circuits. Similarly, it reduces the leakage power by 72% to 86% as compared to high inputs standard dual-V_t circuits, and 57% to 65% as compared to low inputs standard dual-V_t circuits. Proposed circuit2 reduces leakage power by 14% to 53% as compared to proposed circuit1.

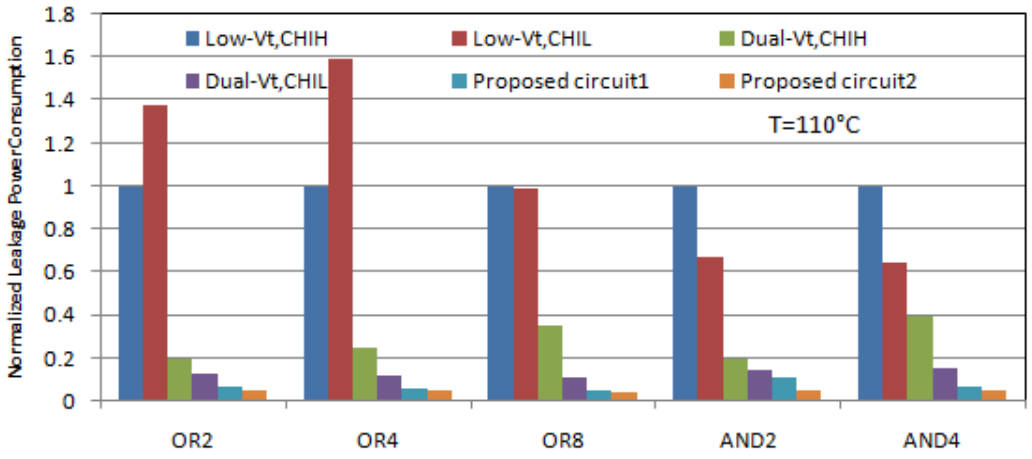

Figure 3.15 Comparison of the leakage power consumption of the proposed circuits and the existing techniques. The leakage power consumption is normalized to the leakage power of the standard low-V_t technique with high inputs for each circuit.

Table 3.5 Total leakage power reduction (%) provided by the proposed circuit1 as compared to the existing circuit technique at 110°C.

Circuits	OR2	OR4	OR8	AND2	AND4
Low-Vt, CHIH	93.47	93.95	95.55	88.81	93.23
Low-Vt , CHIL	95.28	96.21	94.49	83.29	89.58
Dual-Vt, CHIH	66.87	76.14	84.70	42.32	83.06
Dual-Vt, CHIL	50.57	49.94	49.75	22.97	55.59

Table 3.6 Total leakage power reduction (%) provided by the proposed circuit2 as compared to the existing circuit technique and proposed circuit1 at 110°C.

Circuits	OR2	OR4	OR8	AND2	AND4
Low-Vt, CHIH	94.72	95.10	95.36	94.76	94.75
Low-Vt , CHIL	96.19	96.93	95.31	92.17	91.91
Dual-Vt, CHIH	73.24	80.68	86.98	72.99	86.85
Dual-Vt, CHIL	60.08	59.46	57.23	63.93	65.53
Proposed circuit1	19.23	19.01	14.88	53.16	22.40

V. Conclusions

In this chapter, we have proposed new leakage power reduction techniques for OR2, OR4, OR8, AND2 and AND4 of domino footless and domino footed circuits. The performance of these circuits has been evaluated by HSPICE using a BSIM4 0.065µm CMOS technology. We have evaluated the leakage power consumption of the proposed techniques and the comparisons have also been made with the reported circuits at 25°C and 110°C, respectively. Based on the simulation results, it has been culminated that the proposed designs for NAD-OR footless and footed gates have lesser leakage power consumption as compared to the previous reported designs. Consequently, the proposed topologies are appropriate for the realization of low-power high-performance VLSI design.

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