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A New CMOS Voltage Divider Based Current Mirror, Compared with the Basic and Cascode Current Mirrors

Ajay Kumar Dadoria* *MANIT BHOAPL ECE DEPARTMENT* India.
Arjun Singh Yadav *MANIT BHOAPL ECE DEPARTMENT* India.
C.M Roy *MANIT BHOAPL* India.

Abstract— Current mode signal processing implemented in CMOS technology has received increasing interest in the past decades. The circuit implemented in current mode technique occupies small area, consumes less power dissipation and achieves high operation speed. Moreover, many sensors in SOC such as temperature sensors, photo sensors provide current signal. In these applications and high speed data converters such as RF, A/D, D/A converters, oscillators where the function of comparison is a limiting component for accuracy, noise and power consumption reasons, the introduction of current mode solutions is highly desirable. To take the advantages of current mode circuits over the voltage mode limitations, this thesis work proposes two new CMOS Current Comparator circuits, suitable for High Speed and low Power dissipation applications. Modified circuit had been simulated in a proprietary 180nm CMOS process, using Cadence Spectre Simulator and UMC models. Current comparator circuit had impressed with current pulses ranging from Milli-Amperes to Nano-Amperes and its Speed and Power consumption had been simulated and measured. When made a comparison with the earlier reported circuits, our circuit achieves Very High Speed of operation and low power consumption. For Micron range input currents, the power consumption of the newly improved current comparator is very much lower than the other earlier reported circuits.

Keywords— Current Comparator, CMOS, Current Mirror, Cascode Current Mirrors, DC Analysis

I INTRODUCTION

Current Mirrors made by using active devices have come to be widely used in analog integrated circuits both as biasing elements and as load devices for amplifier stages. The current mirror uses the principle that if the gate-source potentials of two identical MOS transistors are equal, then the current flown through their Drain terminals should be the same. The use of current mirrors in biasing can result in superior insensitivity of circuit performance to variations in power supply and temperature [1]. NMOS current mirrors are used as current sinks and PMOS current mirrors are used as current sources. Various current mirror circuits [4] [5] [6] were designed, each of the current mirror configurations has their own intended usage and applications in CMOS analog integrated circuits. There is variety of Current Mirror circuits available, each of them having their own advantages [7] [8].

II Analysis of Basic Current Mirror

Figure-1 shows the Basic Current Mirror circuit using NMOS transistors as active elements. The transistor *M11* is diode connected, forcing its Drain to Gate voltage to zero [1]. In this mode transistor *M11* operates in the saturation region, which in turns acts as a constant current source or reference current source. To work as a current mirror, both *M11* and *M12* are chosen to be identical MOS transistors. Neglecting the channel length modulation effect, if the gate-source of *M12* is being biased to a fixed voltage produces a copy of reference current I_{ref} at the Drain terminals of *M12* transistor, denoted as I_{out}. The Gain of I_{out} is directly proportional to the (W/L) ratio of the transistors, detailed in the below given equation.

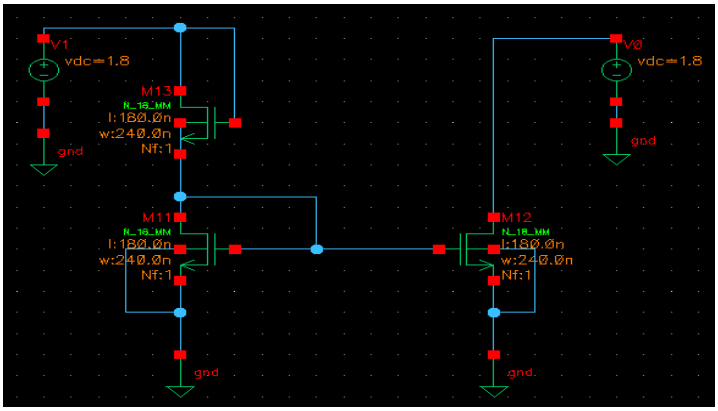

Figure 1 Basic Current Mirror

$$\frac{Io}{Iref} = \frac{\left(\frac{W}{L}\right)2}{\left(\frac{W}{L}\right)1}$$

Where W= Width of the MOS
L = Channel Length of the MOS

If the Channel length modulation has taken in to account, then the above equation should be re-arranged as

$$\frac{Iout}{Iref} = \frac{\left(\frac{W}{L}\right)2}{\left(\frac{W}{L}\right)1}\frac{(1+\lambda\, Vds2)}{(1+\lambda Vds1)}$$

Where λ = Channel Length Modulation
V_{ds2} = Drain to Source Voltage of *M12*
V_{ds1} = Drain to Source Voltage of *M11*

Above equation shows that, copied current I_{out} has direct dependency with Drain to Source voltage of output transistor *M11* and *M12*.

Simulation Results of Basic Current Mirror

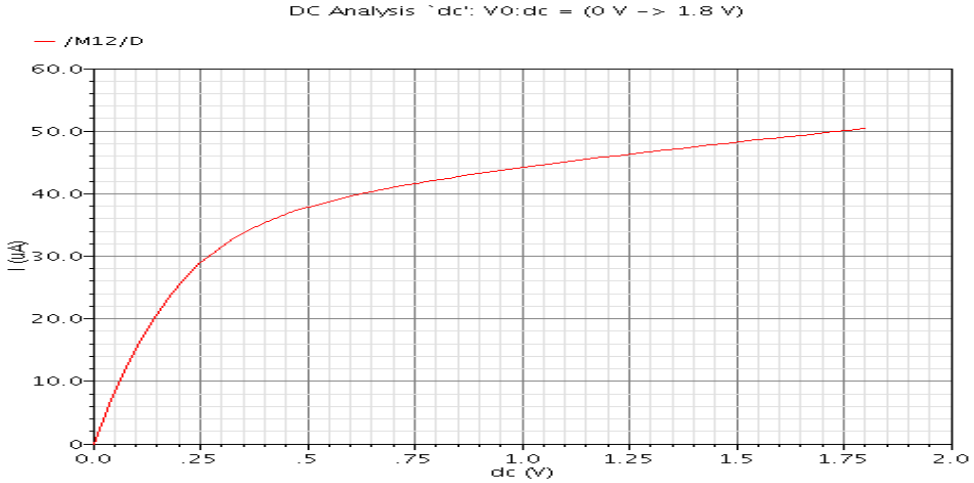

Figure 2 DC Output characteristics of Basic Current Mirror

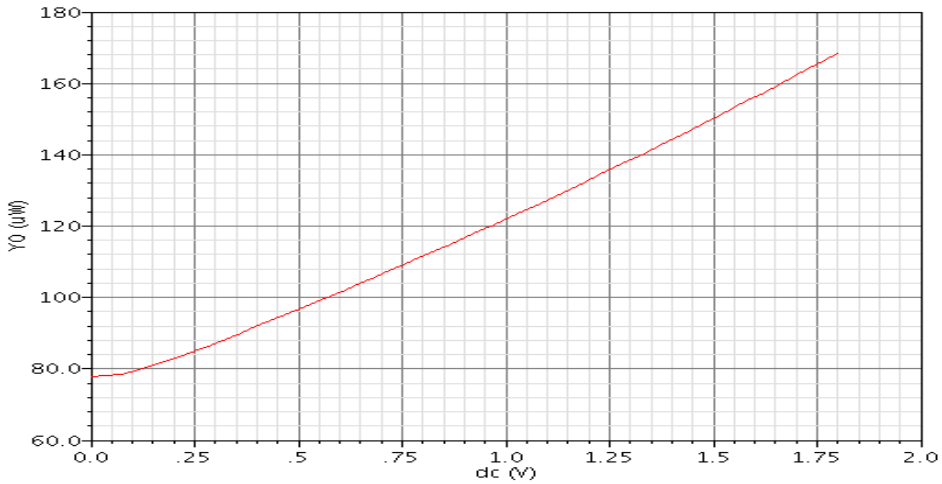

Figure 3 Total Power Dissipation of Basic Current Mirror

When V_{ds} reaches the Supply voltage V_{dd} = 1.8V, Current Mirror consumes maximum power of *170µw*.

III. Analysis of Cascode Current Mirror

To achieve high output resistance, cascode current mirrors are used. Figure-4 shows the Cascode Current Mirror which uses NMOS transistors as active elements. The transistor *M11* and *M15* are configured as diode connected, forcing to operates them in saturation region, which in turns acts as a constant current source or reference current source. One of the advantages of Cascode Current Mirror is its ability to suppress the channel length modulation effects. This is been

achieved by making Drain to Source Voltage of *M11* and *M12* are made equal, so I_{out} always tracks I_{ref}. To work as a current mirror, both *M11* and *M12* are chosen to be identical MOS transistors.

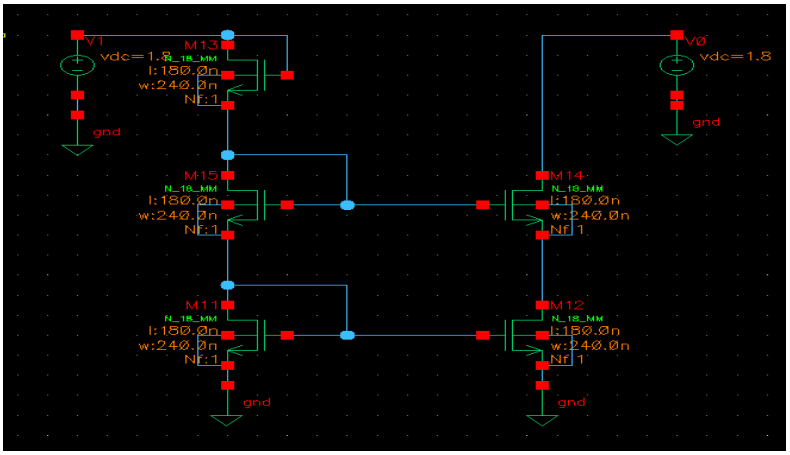

Figure 4 Cascode Current Mirror

Simulation Results of Cascode Current Mirror

DC analysis has been performed. Below graph Figure-5 shows the variation of output current I_{out} against the sweep values of Drain Voltage of *M14*. Figure-6 shows the total power consumption of the Cascode current Mirror. Cascode current mirror reduces the channel length modulation effect.

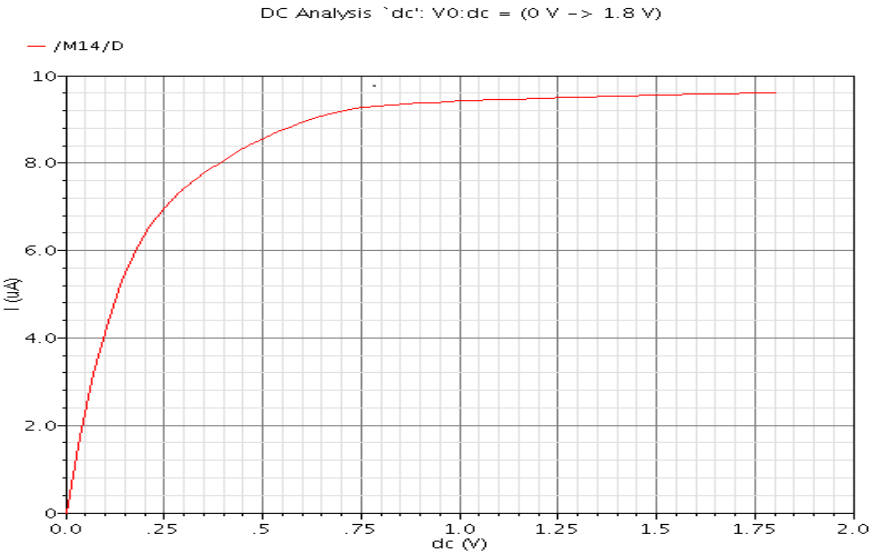

Figure 5 DC Output characteristics of Cascode Current Mirror

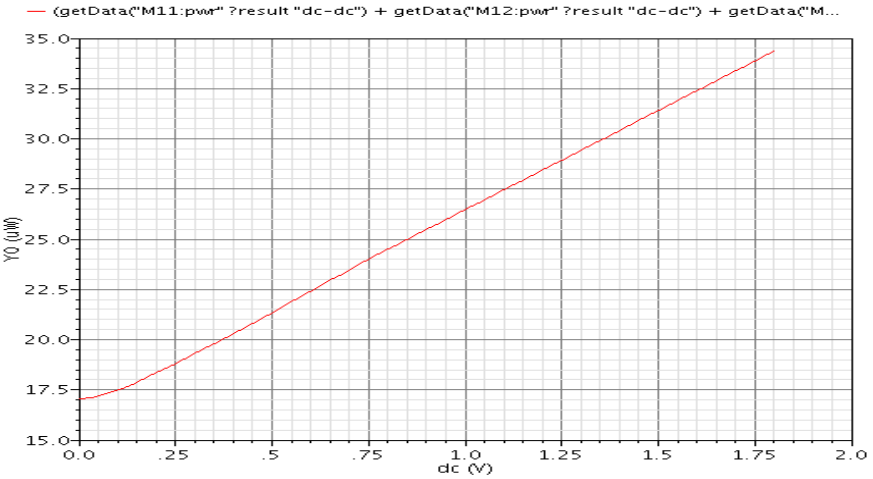

Figure 6 Total Power Dissipation of Cascode Current Mirror

When V_{ds} reaches the Supply voltage V_{dd} = 1.8V, Current Mirror consumes maximum power of *33.8µw*.

IV. Improved Voltage Divider Based Current Mirror

Figure-7 shows the circuit of CMOS Voltage Divider based Current Mirror. Improved circuit uses NMOS and PMOS transistors to form a Voltage Divider, so called as CMOS Voltage Divider based current mirror.

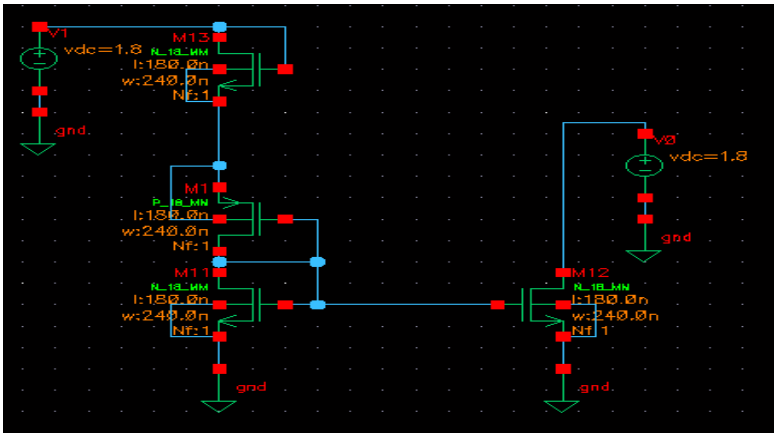

Figure 7 CMOS Voltage Divider based Current Mirror

NMOS and PMOS transistors are diode connected produces the reference voltage V_{gs} to bias the NMOS transistor *M12*, which in turns controls the Output Current I_{out}. The reference current I_{ref} generated by the above circuit is given by

$$Iref = \frac{(Vdd + Vgs1 - Vgs11)}{R}$$

Where I_{ref} = Reference Input Current
V_{dd} = Supply Voltage
V_{gs1} = Gate to Source Voltage of *M1*
V_{gs11} = Gate to Source Voltage of *M11*
R = Resistance offered by the MOS *M13*

Consider the MOS *M12* operates in saturation region, and then the output current becomes

$$Iout = Kn'\left(\frac{W}{L}\right)(Vgs11 - Vds2)\text{^}2(1 + \lambda Vds2))$$

All the MOS transistors having the same W/L ration. Like Wilson current mirror, CMOS Voltage Divider based current mirror used for low current biasing applications. This new current mirror offers low power consumption, when compared to standard current mirrors.

Simulation Results

Below graph Figure-8 shows the Variation of output current I_{out} against the sweep values of Drain to Source Voltage of *M12*, V_{ds2}. From the graph, it's been identified that this improved new current mirror is well suited for lower current biasing applications such as the tail stages of differential amplifier.

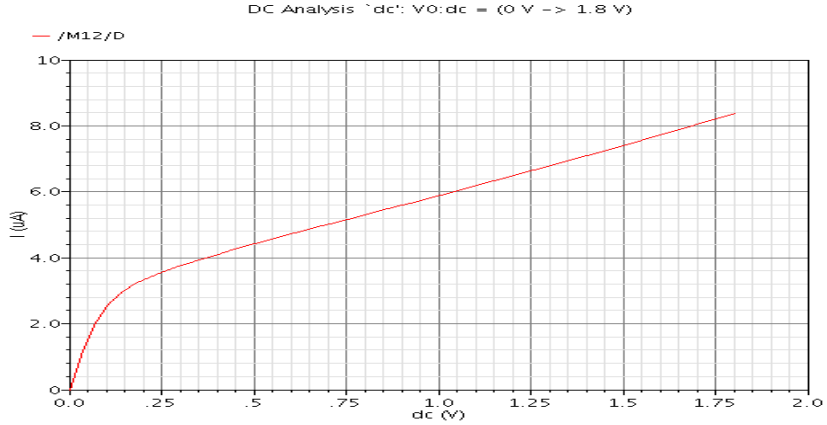

Figure 8 DC Output characteristics of improved Current Mirror

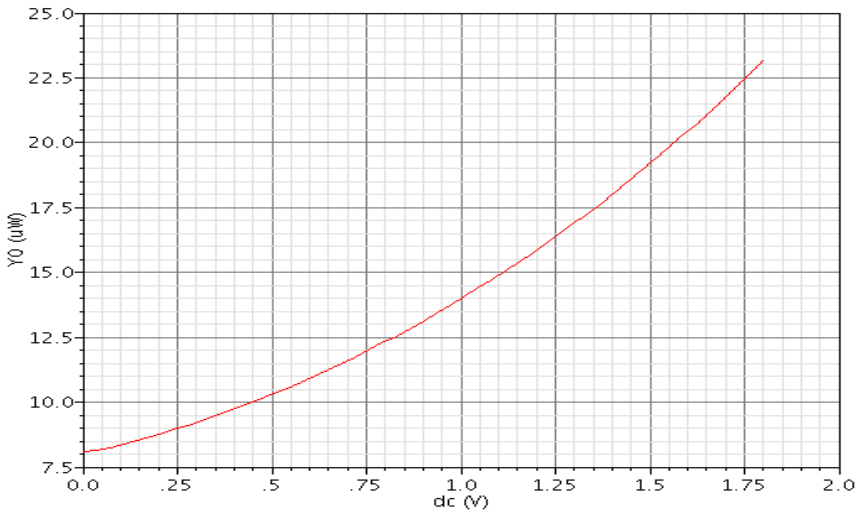

Figure 9 Total Power Dissipation of improved Current Mirror

Figure-9 shows the total power consumed by the newly improved current mirror. Below Table-1, describes some of the important parameters of the improved CMOS Voltage Divider based current mirror. In the Next section, improved Current mirror circuit is being compared with the Basic and Cascode Current mirror circuit, which are already explained in previous sections of this chapter

V. Comparison of Current Mirrors

Characteristics and parameters of the Basic, Cascode and improved CMOS Voltage Divider based current mirror are compared and the observations are explained in detail.

Issue	Number of Transistors	Total Width of all the Transistors (nm)	Power Dissipation(at 7µA) (µW)	Output Resistance (Ω)
Improved Current Mirror	4	960	17.7	$1/(\lambda.I_o)$
Basic Current Mirror	3	720	78.3	$1/(\lambda.I_o)$
Cascode Current Mirror	4	960	18.75	$gm_{14}(rd_{12}.rd_{14})$

Table 1 Comparison of Current Mirror parameters

From Table-1, it is observed that the improved new Current Mirror consumes only $1/4_{th}$ of the power consumed by the Basic Current Mirror, there by achieves 75% of reduction in power consumption. When compared to Cascode current mirror, newly improved current mirror provides marginal reduction in power consumption.

VI Conclusion

Main intention of this paper is to present the simple idea of designing a new CMOS Voltage Divider based Current Mirror, than its comparison with the Basic and Cascode Current Mirrors. This new Mirror is well suited for low current biasing applications. Like the Wilson and Widler current Mirror Circuits, this new Current Mirror can be used as a Low Current Biasing circuit. Also, when compared with Basic Current Mirror, improved one consumes only $1/4_{th}$ of the Power consumed by the Basic Current Mirror. This enormous amount of Power saving leads the viability of the circuit usage in CMOS Analog circuit applications such as biasing of Differential Amplifiers and Operational Amplifiers .

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