Volume 3, Issue 4, April 2013 ISSN: 2277 128X
International Journal of Advanced Research in Computer Science and Software Engineering
Research Paper
Available online at: www.ijarcsse.com

Comparative Analysis Of Variable N-T Sram Cells

Ajay Kumar Dadoria* *MANIT BHOAPL ECE DEPARTMENT India.*
Arjun Singh Yadav *MANIT BHOAPL ECE DEPARTMENT India.*
C.M Roy *MANIT BHOAPL India.*

Abstract— SRAM is designed to provide an interface with CPU and to replace DRAMs in systems that require very low power consumption. Low power SRAM design is crucial since it takes a large fraction of total power and die area in high performance processors. A SRAM cell must meet the requirements for the operation in submicron/nano ranges. The scaling of CMOS technology has significant impacts on SRAM cell – random fluctuation of electrical characteristics and substantial leakage current. The random fluctuation of electrical property causes the SRAM cell to have huge mismatch in transistor threshold voltage. Consequently, the static noise margin (Read Margin) and the write margin are degraded dramatically. The SRAM cell tends to be unstable and the low power supply operation becomes hard to achieve. In this paper we compared different type of SRAM topology, at a 180nm CMOS technology to accomplish improvements in stability, power dissipation and performance compared with previous designs for low-power memory operation. Cadence Virtuoso simulation in standard 180nm CMOS technology confirms all results obtained from this paper.

Keywords— Conventional SRAM, nT SRAM, Low Power, Leakage Current, Output waveform.

I. INTRODUCTION

SRAMs are widely used for mobile applications as both on chip and off-chip memories, because of their ease of use and low standby leakage. In recent years the demand for low power devices has been increases tremendously. This demand may be due to fast growth of battery operated portable applications such as PDAs, cell phones, laptops & other handheld devices. But also at the same time problems arising from continuous technology scaling have recently made power reduction an important design issue for the digital circuits and applications. CMOS scaling beyond the 180nm technology node requires not only very low threshold voltages (Vt) to retain the device switching speeds to maintain the current drive and keep threshold voltage variations under control when dealing with short-channel effects [I]. The increased importance of power is even more noticeable for a new class of energy constrained systems. As sub-threshold circuits can allow ultra-low power designs to be fabricated on modern process technology. Sub threshold operation is applicable to wide range of applications ranging from wireless devices, biomedical applications, spacecraft applications etc. The leakage power dissipation is roughly proportional to the area of a circuit. Since in many processors caches occupy about 50% of the chip area [2]. Lowering supply voltage to reduce power consumption is one of the choice of the designers for designing low leakage SRAM circuits.

However ultra-low power design of high density SRAMs in which the operating voltage is below the transistor sub threshold is extremely challenging. Also by the system integration point of view, SRAM must be compatible with subthreshold combinational logic, operating at ultra-low voltages. Furthermore, many of them try to reduce the subthreshold leakage current only, whereas for sub-nm technology node, the tunnelling gate leakage is comparable to the subthreshold leakage. In this paper we present a method for reducing both subthreshold and tunneling gate leakage current of an SRAM by using different threshold voltages and oxide thicknesses for transistors in an SRAM cell. The idea is to deploy different configurations of six-transistor SRAM cells corresponding to different threshold voltage and oxide thickness assignments for the transistors.

6T SRAM cell

In this 6T memory cell as shown in Figure 1, the load is replaced by a PMOS transistor. This SRAM cell is composed of six transistors, one NMOS transistor and one PMOS transistor for each inverter, plus two NMOS transistors for access. This configuration is called a 6T Cell [4]. This cell offers better electrical performances (speed, noise immunity, standby current) than a resistive load 4T structure. The main disadvantage of this cell is its large size. Each bit in an SRAM is stored on four transistors that form two cross coupled inverters. This storage cell has two stable states which are used to denote **0** and **1**. Two additional access transistors serve to control the access to a storage cell during read and write operations. Access to the cell is enabled by the word line (WL in figure) which controls the two access transistors M5 and M6 which, in turn, control whether the cell should be connected to the bit lines: BL and ~BL. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, but both the signal and its inverse are typically provided in order to improve noise margins.

© 2013, IJARCSSE All Rights Reserved

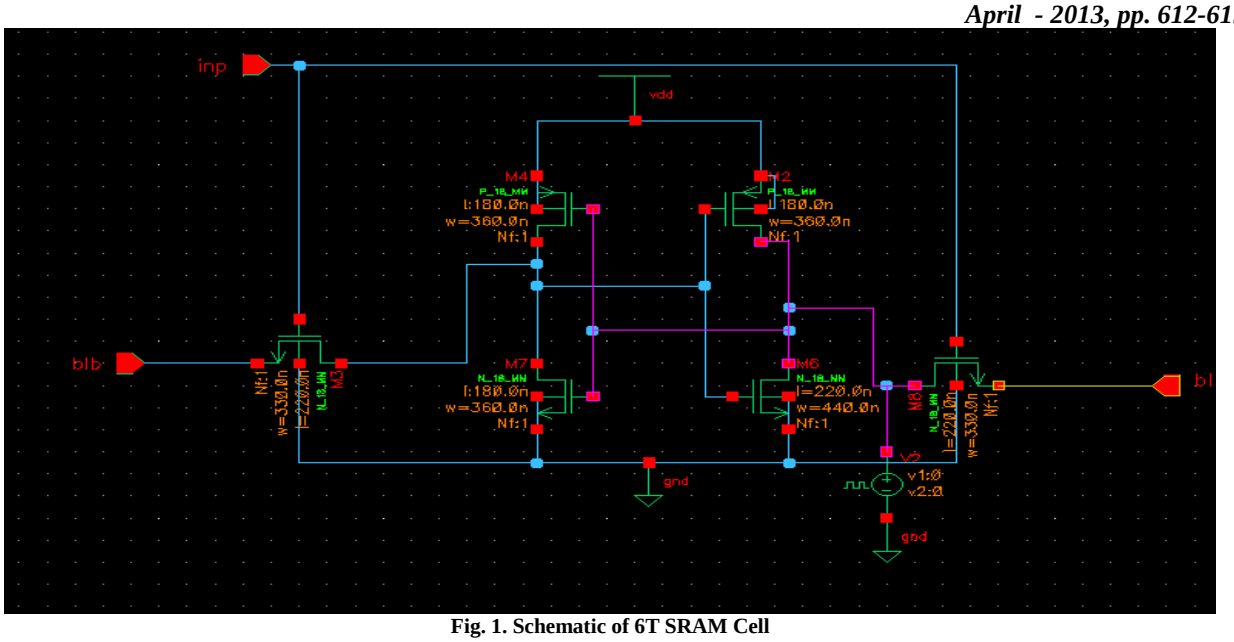

Fig. 1. Schematic of 6T SRAM Cell

Reading

Assume that the content of the memory is a 1, stored at Q. The read cycle is started by precharging both the bit lines to a logical 1, then asserting the word line WL, enabling both the access transistors. The second step occurs when the values stored in Q and ~Q are transferred to the bit lines by leaving BL at its precharged value and discharging BLB through M1 and M5 to a logical 0 (i.e eventually discharging through the transistor M1 as it is turned on because the Q is

Logically set to 1). On the BL side, the transistors M4 and M6 pull the bit line towards V_{dd}, a logical 1 (i.e eventually being charged by the transistor M4 as it is turned on because Q is logically set to 0). If the content of the memory was a 0, the opposite would happen and BL would be pulled towards 1 and BL towards 0. Then these BL and ~BL will have a small difference of delta between them and then these lines reach a sense amplifier, which will sense which line has higher voltage and thus will tell whether 1 was stored or 0. The higher the sensitivity of sense amplifier, the faster the speed of read operation.

Writing

The start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL to 0 and ~BL to 1. A 1 is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. Note that the reason this works is that the bit line input drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily over ride the previous state of the cross-coupled inverters. Careful sizing of the transistors in an SRAM cell is needed to ensure proper operation.

4 T SRAM

In Fig.2 4T SRAM Cell the cross-coupled inverters formed by the transistors store a single bit of information. The write bit line WL used for transferring new data into the cell [6]. When '0' stored in cell, load and driver transistor are ON and there is feedback between ST node and STB node, therefore ST node pulled to GND by drive transistor and STB node pulled to V_{DD} by load transistor. And when '1' stored in cell, load and driver transistor are OFF and for data retention without refresh cycle following condition must be satisfied.

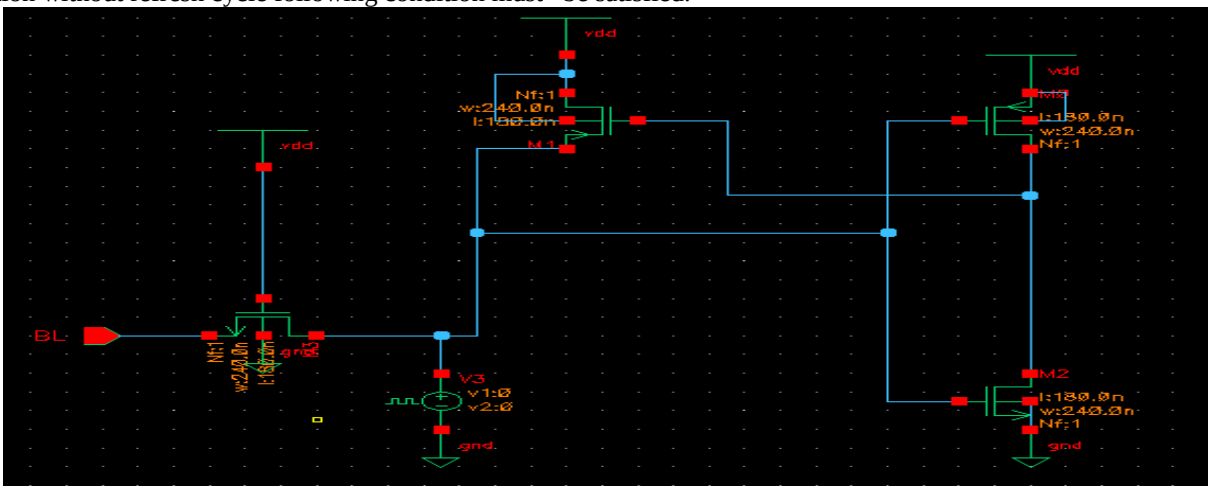

Fig. 2 Schematic of 4T SRAM Cell

© 2013, IJARCSSE All Rights Reserved

7T SRAM cell

In Fig.3 7T SRAM Cell When '1' stored in cell, M3 and M2 are ON and there is positive feedback between ST node and STB node, therefore ST node pulled to V_{DD} by M2 and STB node pulled to GND by M3. When '0' stored in cell M4 is ON and since N node maintained at V_{DD} by M5 the STB pulled to V_{DD}, also M2 and M3 are OFF and for data retention without refresh cycle following condition must be satisfied. For satisfying above condition when '0' stored in cell, we use leakage current of access transistors (Ml), especially sub-threshold current of access transistors (MI). For this purpose during idle mode of cell, bit-line maintained at GND and word-line maintained at V Idle.

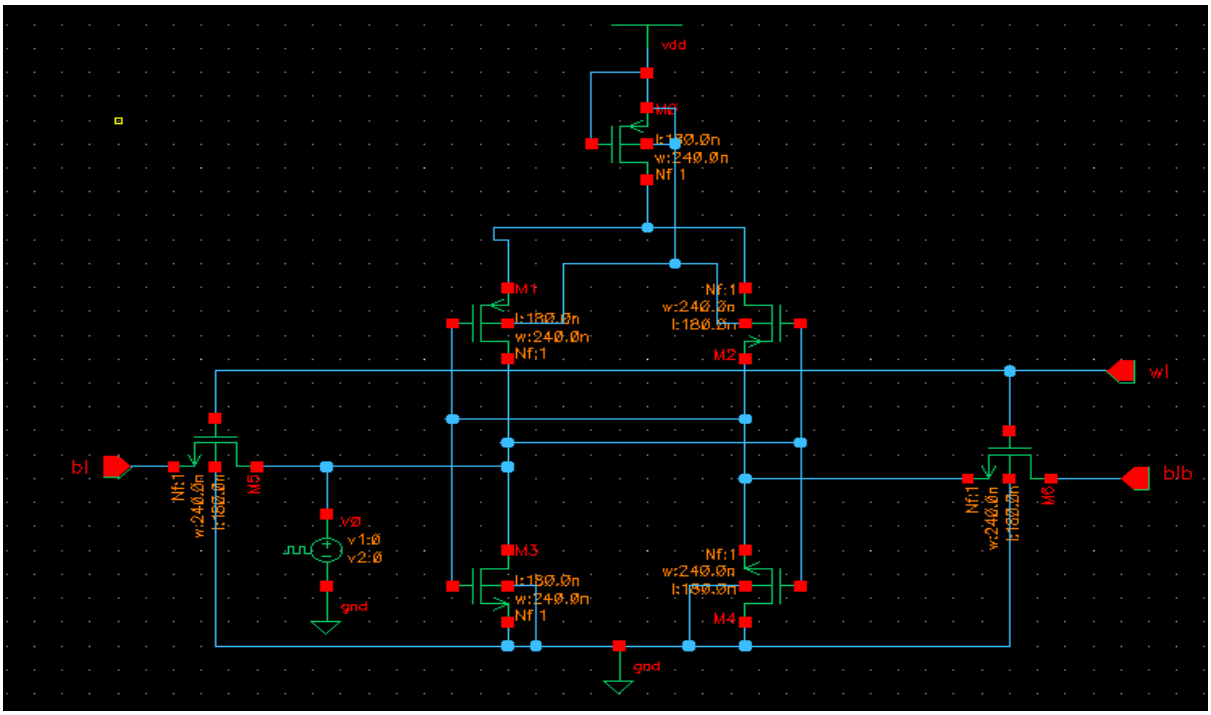

Fig. 3 Schematic of 7T SRAM Cell

4T SRAM CELL

In Fig.4 8T SRAM cell is shown, Four transistors N1, N2, P1, P2 form a cross-couple structure to store data. Four transistors P3 and N3- N5 are access to the internal nodes D and /D of the cell. N3 and N4 connect the cell internal nodes D and /D of the cell. N3 and N4 connect the cell internal nodes to the BLs while P3 and N5 form an inverter to control the voltage of node C1. The source terminal of P3 is connected to a column select (CS) line while gates of P3 and N5 are connected to WL. Unlike conventional design, the sources of P1 and P2 are connected to dynamic cell supply (*cell supply*) line which is raised to the higher voltage during read operation to obtain a higher noise margin.

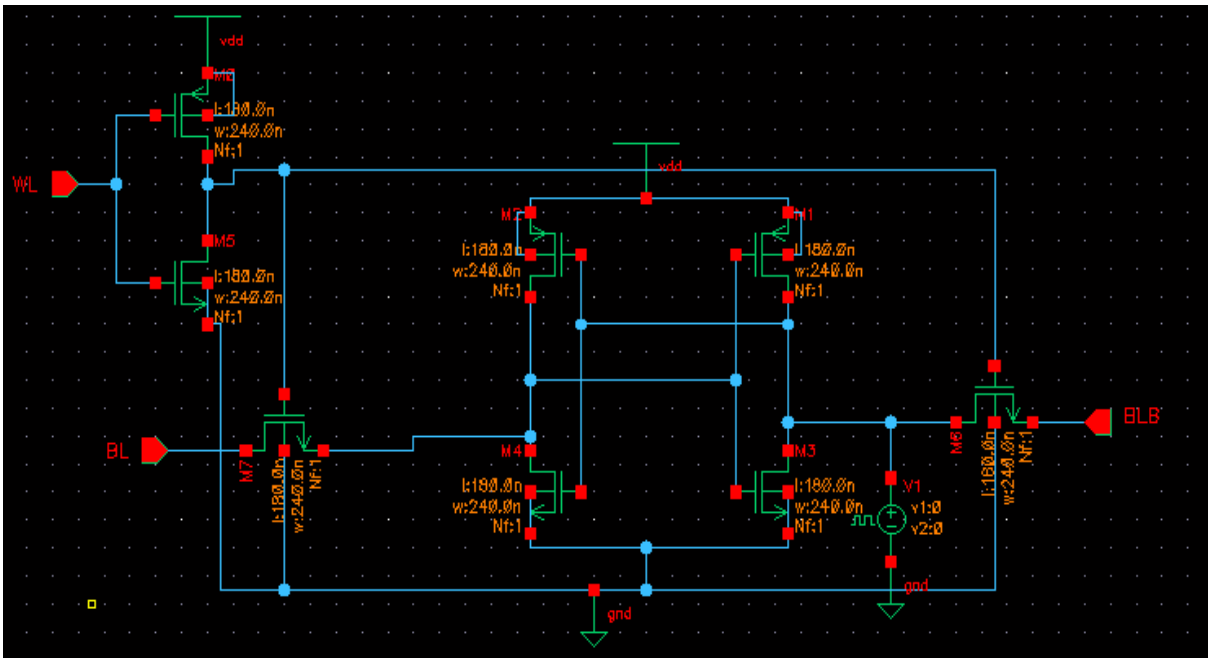

Fig. 4 Schematic of 8T SRAM Cell

© 2013, IJARCSSE All Rights Reserved

8T SRAM CELL

In Fig.4 8T SRAM cell is shown, Four transistors N1, N2, P1, P2 form a cross-couple structure to store data. Four transistors P3 and N3- N5 are access to the internal nodes D and /D of the cell. N3 and N4 connect the cell internal nodes D and /D of the cell. N3 and N4 connect the cell internal nodes to the BLs while P3 and N5 form an inverter to control the voltage of node C1. The source terminal of P3 is connected to a column select (CS) line while gates of P3 and N5 are connected to WL. Unlike conventional design, the sources of P1 and P2 are connected to dynamic cell supply (*cell supply*) line which is raised to the higher voltage during read operation to obtain a higher noise margin.

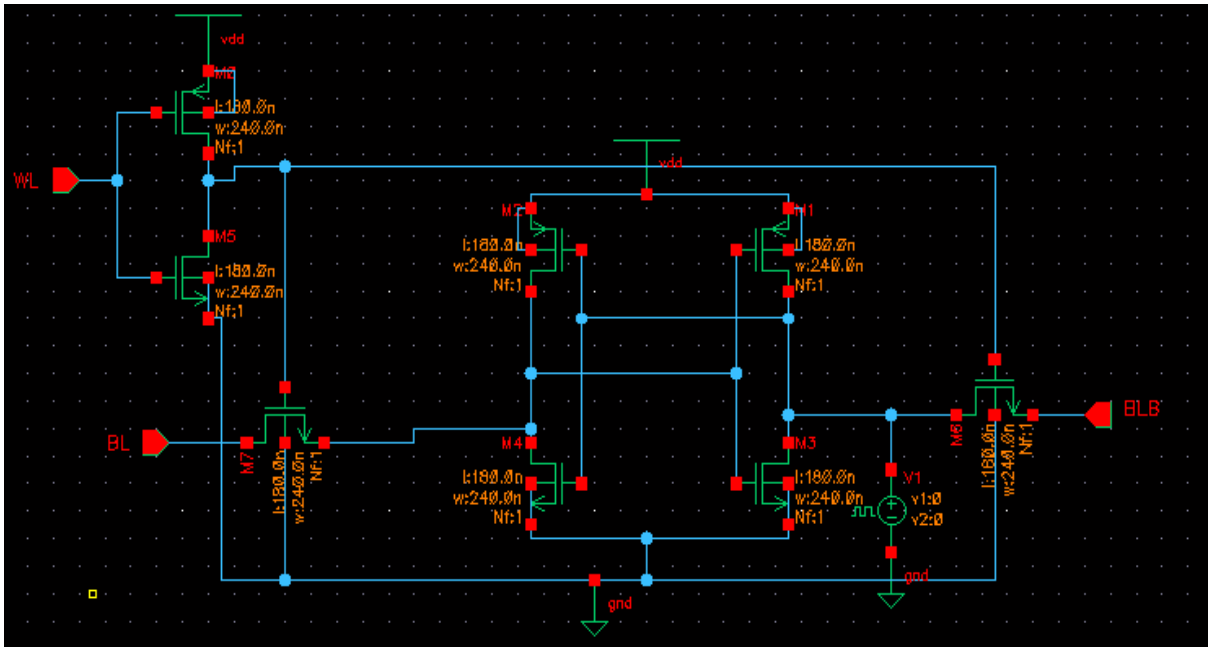

Fig. 4 Schematic of 8T SRAM Cell

9TSRAM CELL

In Fig. 5 schematic of 9T SRAM cell [8] is shown in the Fig. 5. This circuit shows reduced leakage power and enhanced data stability. The 9T SRAM cell completely isolates the data from the bit lines during a read operation. The idle 9T SRAM cells are placed into a super cut off sleep mode, thereby reducing the leakage power consumption as compared to the standard 6T SRAM cells.

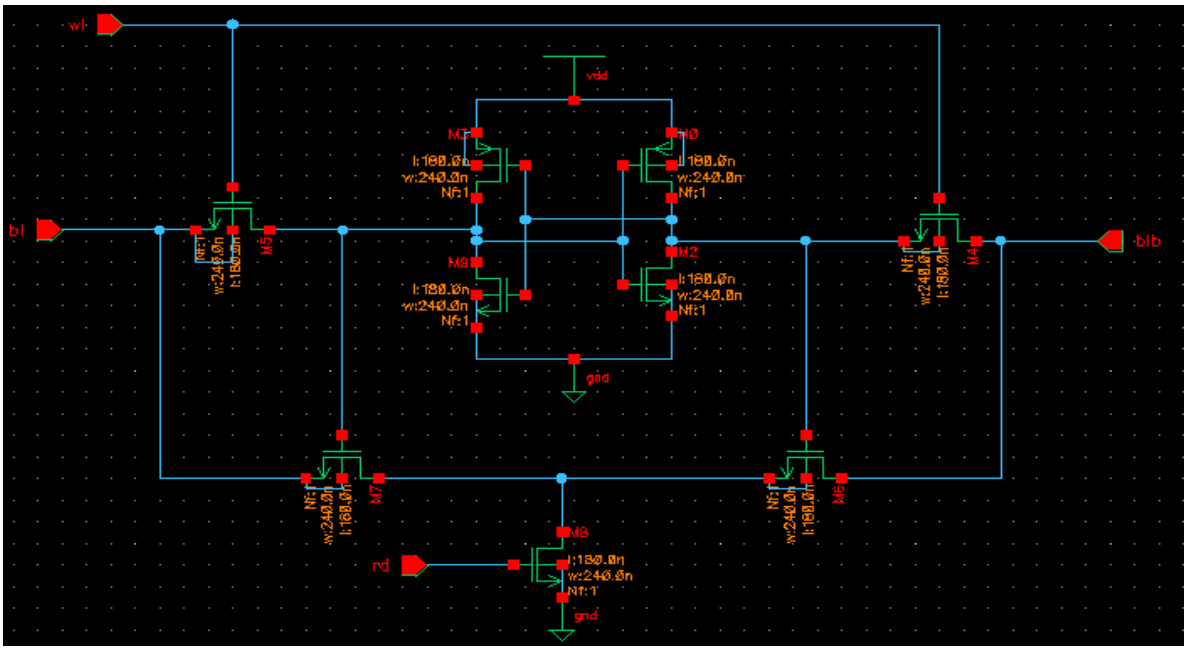

Fig. 5 Schematic of 9T SRAM Cell

10T SRAM Cell

10T SRAM cell [14] is as shown in Fig.6 This circuit shows 10T SRAM Cell with differential read bit lines (BL and BLB). Two NMOS transistors (NMOS_4 and NMOS_8) for the RBL and the other additional NMOS transistors (NMOS_6 and NMOS_7) for BLB are appended to the 6T SRAM. As well as the 8T SRAM, pre -charge circuits must be implemented on the BL and BLB.

© 2013, IJARCSSE All Rights Reserved

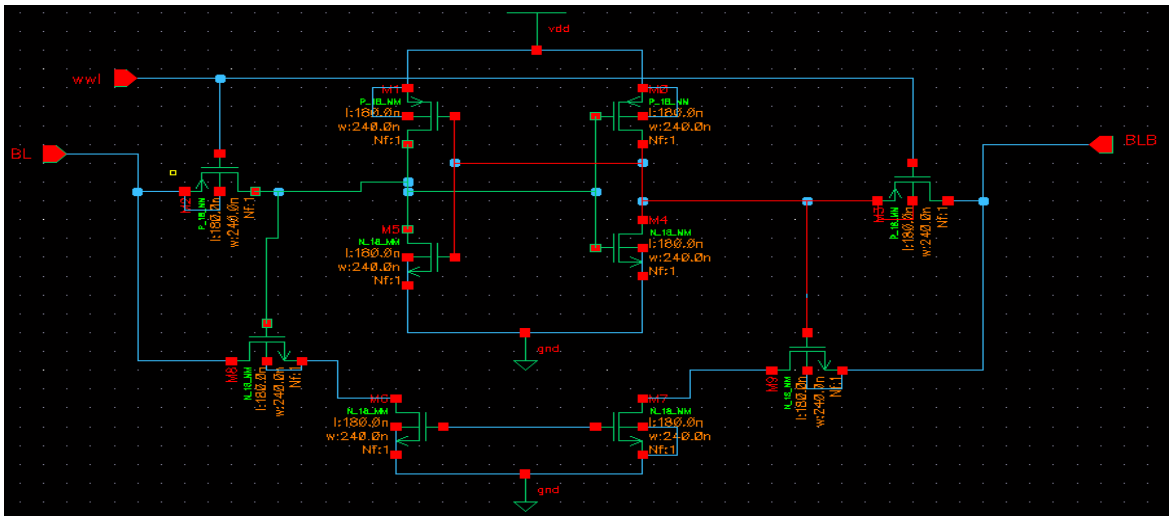

Fig. 6 Schematic of 10T SRAM Cell

11 T SRAM CELL

Fig.7 shows the circuit of the proposed cell. Our circuit contains 11 transistors instead of 6 transistors. Due to overall lower power consumption and faster access time, this hardware burden can be tolerated. The proposed cell includes two tail transistors N7 and N9 which are controlled by bit line and bit bar line respectively. Two other n MOS transistors N8 and N6 are used for read operation. Access transistors N3 and N4, for write operation, are controlled by write word line (WWL) whereas read operation is performed through access transistor N5 which is driven by read word line RWL. Single bit-line RBL is used for read operation. During write operation, RWL is set to be zero while asserting WWL. Write 1 and write 0 operations are performed by selecting proper values on bit line as well as bit-bar line. The critical paths for these two write operations are shown in Fig.3.10. When BL=0, N9 turned OFF, Node B shifts to high means node A =0. This is write 0 operation. When BL=1, N7 turned OFF, node A pushes to high which results low at node B. This operation is equal to write 1 operation. In these operations, BL or BL bar is neither charging nor discharging as in 6T cell; therefore, lot of power is saved during write 1 and write 0 operations.

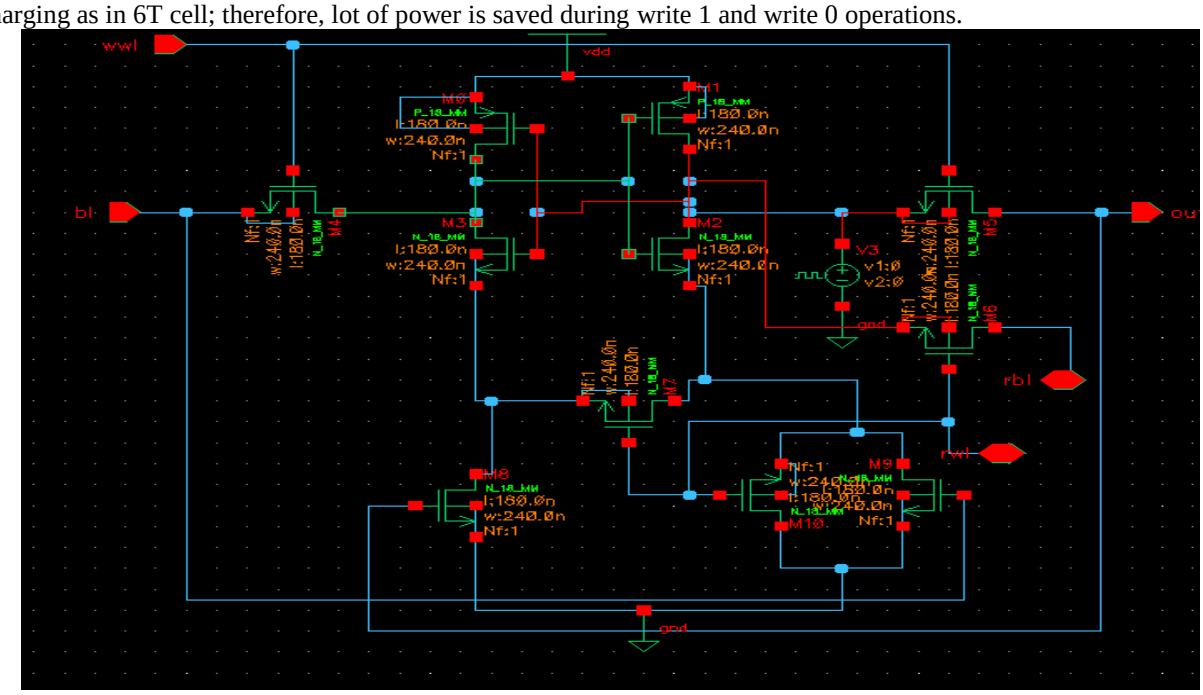

Fig.7 Schematic of 11T SRAM Cell

2. Simulation And Results

The static noise margin for the input series voltage noise source has received a significant attention among different noise sources. That is because this noise source models the static circuit non-idealises such as threshold voltage variation of the MOS devices and mismatches. This type of noise margin is widely known as static noise margin (SNM). Clearly, the two wings of the butterfly curve are identical if the feedback and feed forward VTCs are the same. However, if there is a mismatch between the feedback and feed forward VTC, then there is an asymmetry in the butterfly curves, making the sizes of Maximum Square different.

A butterfly curve for SNM of SRAM cell

© 2013, IJARCSSE All Rights Reserved

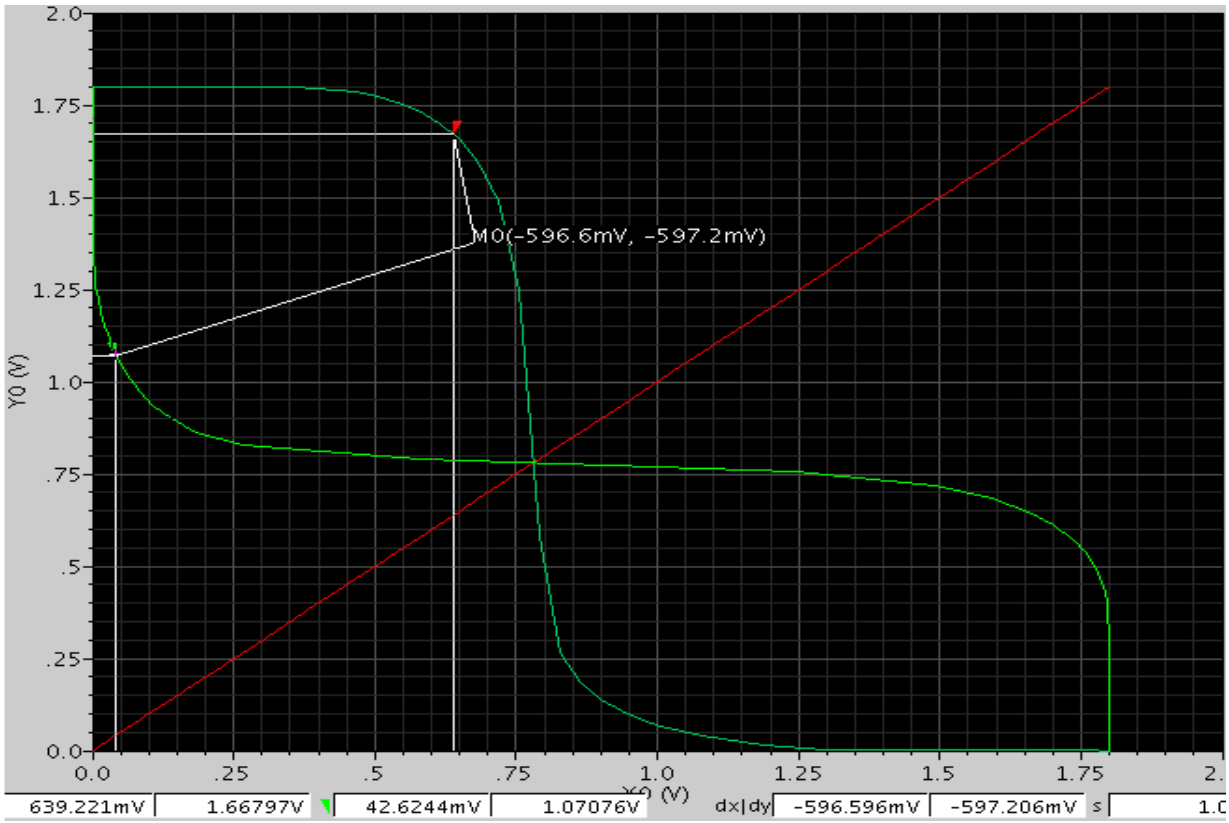

Fig. 8 Abutterfly curve for SNM of SRAM cell

Simulated result for power consumption of SRAM cell

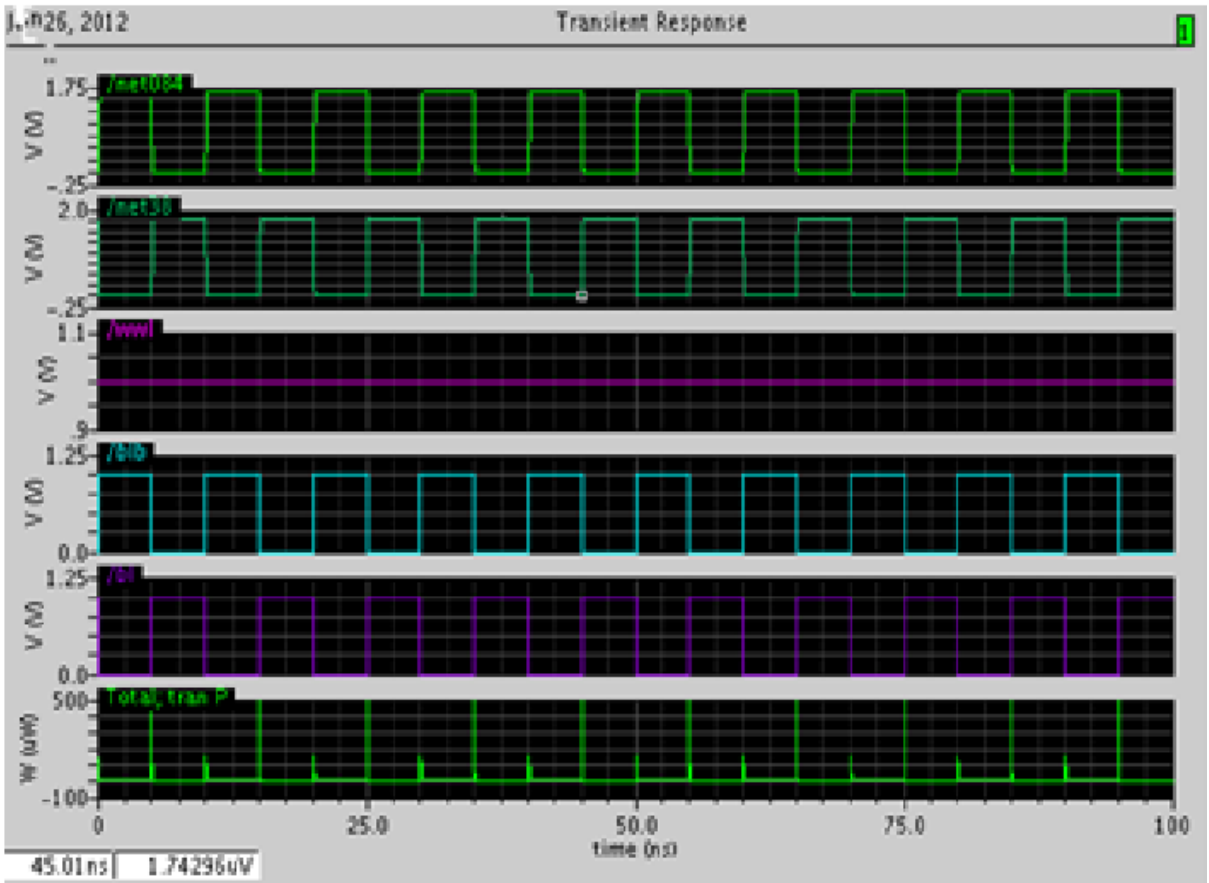

Fig. 9 Simulation Wave Form

© 2013, IJARCSSE All Rights Reserved

RESULTS

Table -1

Parameter	4T	6T	7T	8T	9T	10T	11T
Power consumption	$610.2e^{-9}$	$2.0e^{-6}$	$313.3e^{-6}$	$2.12e^{-6}$	$501e^{-3}$	$25.28e^{-6}$	$8.022e^{-6}$
Delay	$10.04e^{-9}$	$10.83e^{-12}$	$29.66e^{-12}$	$10.08e^{-9}$	$1.16e^{-12}$	$23.1e^{-12}$	$137.8e^{-12}$
SNM (in hold mode)	449.82	596.88	562.23	550.04	541.8	543.3	596.6
PDP	$6346.08e^{-18}$	$21.66e^{-18}$	$9292.48e^{-18}$	$21.97e^{-15}$	$581.16e^{-15}$	$583.97e^{-18}$	$1105.43e^{-18}$

Conclusion

In this thesis we have simulated and analyzed the performance of various topologies of SRAM cells at 180 nm technology for parameters like cell power consumption, delay and SNM. By comparative analysis of various topologies of SRAM cells; we can suggest that which SRAM cell topology is batter based on various analyzed parameters. The comparative results are given in Table 1 which shows that the power consumption, delay and SNM are minimum for 4T, 9T and 4T SRAM Cells and Maximum for 9T, 8T, and 6T SRAM Cells respectively. The results can be used to select SRAM cell topology to design and fabricate memory chips which is best suitable for different type of application. For power constrained projects like space exploration and satellites the SRAM cell which consumes minimum power should be used while for very fast processing devices the SRAM cell which has minimum time delay should be used. The SRAM cell which has maximum SNM can be used in the device which works in noisy environment. The design of SRAM cell can be optimized by trade off between various performance parameters.

References

[I] Y. 1. Chang, F. Lai, and C. L. Yang, "Zero-Aware Asymmetric SRAM Cell for Reducing Cache Power in Writing Zero," IEEE Transactions on Very Large Scale integration Systems, vol. 12, no. 8, pp. 827-836,2004.

[2] A. Kotabe, K. Osada, N. Kitai, M. Fujioka, S. Kamohara, M. Moniwa, S. Morita, and Y. Saitoh, "A Low- Power Four-Transistor SRAM Cell With a Stacked Vertical Poly- Silicon PMOS and a Dual-Word-Voltage Scheme," IEEE Journal of Solid-State Circuits, vol. 40, no. 4, pp. 870- 876,2005.

[3] L. Villa, M. Zhang, and K. Asanovic, "Dynamic zero compression for cache energy reduction," in Proceeding 33rd Annual IEEE/ACM nternational Symposium Micro architecture, pp. 214-220, 2000.

[4] K. Takeda et aI., "A read-static-noise-margin-free SRAM cell for low VDD and high-speed applications," IEEE Journal of Solid-State Circuits, vol. 41, no. I, pp. 113-121, 2006.

[5] J. Rabaey, A. Chandrakasan, and B. Nicolic, *Digital Integrated Circuits A Design Perspective*, 2nd ed. Prentice Hall, 2003.

[6] C. F. Hill, \Noise margin and noise immunity in logic circuits," *Microelectronic Journal*, pp. 16{21, Apr 1968.

[7] J. Lohstroh, \Static and dynamic noise margins of logic circuits," *IEEE J. Solid-State Circuits*, vol. SC-14, pp. 591{598, 1979.

[8] J. Lohstroh, E. Seevinck, and J. D. Groot, \Worst-case static noise margin criteria for logic circuits and their mathematical equivalence," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 803{807, 1983.

[9] C. Mead and L. Conway, *Introduction to VLSI systems*. Addison Wesley, 1980.

[10] E. Seevinck, F. List, and J. Lohstroh, \Static-noise margin analysis of MOS SRAM cells," *IEEE J. Solid- State Circuits*, vol. SC-22, pp. 748{754, 1987.

[11] S. Narenda and A. Chandrakasan, *Leakage in Nanometer CMOS Technology*. Springer-Verlag, 2006.

[12] B. Yang and L. Kim, \A low power SRAM using hierarchical bit-line and local sense ampli¯ers," *IEEE J. Solid-State Circuits*, vol. 40, pp. 1366{1376, June 2005}.

[13] K. Kanda, S. Hattori, and T. Sakurai, \90 % write power-saving SRAM using sense- amplifying memory cell," *IEEE J. Solid-State Circuits*, vol. 93, pp. 929{933, 2004.

[14] E. Seevinck, F. List and J. Lohstroh, "Static-Noise Margin Analysis of MOS SRAM Cells," IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 5, pp. 748-754, Oct. 1987.

[15] J. Lohstroh, E. Seevinck and A. Groot, "Worst-Case Static Noise Margin Criteria for Logic Circuits and Their Mathematical Equivalence," IEEE Journal of Solid-State Circuits, Vol. SC-18, No. 6, pp. 803-807, Dec. 1983.

© 2013, IJARCSSE All Rights Reserved

[16] Koichi Takeda et al, "A Read Static Noise Margin Free SRAM cell for Low Vdd and High Speed Applications",*Solid-State Circuits, IEEE Journa*l vol. 41, Jan.2006, Issue 1 , pp.113-121.

[17] Aly, R.E. Bayoumi, M.A., "Low-Power Cache Design Using 7T SRAM Cell" *Circuits and Systems II: Express Briefs, IEEE Transactions*, vol. 54 April 2007, Issu.e: 4, pp. 318-322

[18] Chang, L. Montoye, R.K. Nakamura, Y.Batson, K.A.Eickemeyer, R.J.Dennard, R.H. Haensch, W.Jamsek, D, "An 8T-SRAM for Variability Tolerance and Low-Voltage Operation in High-Performance Caches", *Solid-State Circuits, IEEE Journal*vol. 43, April 2008, Issue 4, pp-956-963.

[19] Sinangil M., Naveen Verma, A.P.Chandrakasan , "A Reconfigurable 8T Ultra –Dynamic Voltage Scalable(U-DVS) SRAM in 65nm CMOS" , *Solid-State Circuits, IEEE Journal* ,vol. 44 , no. 11, Nov.2009, pp.3163-3173.

[20] Naveen Verma,Anantha P. Chandrakasan, "A 256kb 65nm 8T Subthreshold SRAM Employing Sense-Amplifier Redundancy", *Solid-State Circuits, IEEE Journal*, vol. 43 , no. 1, Jan 2008, pp.141-150.

[21] Neil H E Weste, David Harris and Ayan Banerjee, "CMOS VLSI design –a circuit and system perspective".

[22] Hiroki Noguchi et al., "Which is the best dual port SRAM in 45nm process technology?8T,10T single end and 10T differential" *Renesas Technology corporation,2008.*

[23] RajshekharKeerthi Stability and Static Noise margin analysis of low power SRAM"*IEEE International Instrumentation & Measurement Technology Conference*, Victoria,Henry Chen, "

[24] Zhiyu Liu, Volkan Kursun, " Characterization of a novel Nine Transistor SRAM cell,IEEE Transactions on Very Large Scale Integration Systems,voI. 46, Issue 4,April 2008.pp-488-492.

[25] A. 1. Bhavnagarwala, X. Tang, and 1. Meindl, "The impact of intrinsic device fluctuations on CMOS RAM cell stability," IEEE Journal of Solid-State Circuits, vol. 36, no. 4, Apr. 2001, pp. 658-665.

[26] N. Azizi, F. Najm, and A. Moshovos, "Low-leakage asymmetric-cell SRAM," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 11, no. 4, Aug. 2003, pp. 701-715.

[27] F. Hamzaoglu, Y. Te, A. Keshavarzi, et aI. , "Dual Vt-SRAM cells with full-swing single-ended bit line sensing for highperformance on-chip cache in O.13□m technology generation," in Proc. of International Symposium on Low Power Electronics and Design, 2000, pp. 15-19.

[28] R. Heald and P. Wang, "Variability in sub-100nm SRAM designs," in Proc. of International Conference on ComputerAided Design, 2004, pp. 347-352.

[29] E. Grossar, M. Stucchi, K. Maex, et aI. , "Read stability and write-ability analysis of SRAM cells for nanometer technologies," IEEE Journal of Solid-State Circuits, vol. 41, no.II, Nov. 2006, pp. 2577-2588.

© 2013, IJARCSSE All Rights Reserved