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Scope of Multilevel Phase Change Memory in Future Memory Systems

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Abstract— The main memory currently being used is facing challenges due to its scalability, cost and power issues. Over the last few years, the number of multi-core processors in the market being demanded are increasing due to their ability to handle multiple processes concurrently, thus making them the mainstream of modern computing. Multi-core systems have multiple cores integrated in a single chip and a circuit installed on such system may consist of several of such chips. With systems shrinking, the size of the electrons per cell is also reducing which is creating problems in voltage induction and charge storage. Thus, the main memory is already reaching to its cost as well as power limits. Also, scaling DRAM on and above 40 nm is getting increasingly harder, making it inept for future systems and Cloud Computing services. PCM combines the best characteristics of various memory types, which makes it compelling for system architects for future high end applications and products to take its benefits. This paper enlightens the scope of the multilevel Phase Change Memory (PCM or Pram) in future memory systems as it has much to offer in terms of scalability, speed, storage density, non-volatility and less energy consumption that makes it fit for technologies like cloud and computing systems of the future.

Keywords —Multilevel PCM, DRAM, Scalability, Storage density, Phase Change Memory.

I. Introduction

There are broadly two types of memory, one is the charge memory in which data is stored in form of charge while in the other, data is stored in forms of varying resistance i.e. the resistive memory .Phase Change Memory (PCM) belongs to a class of non-volatile resistive memory in which the data is stored in form of resistance. This memory uses the property of chalcogenide substances to switch between two phases i.e. amorphous and crystalline phase on application of thermal energy via electrical pulses. Depending on the voltage applied, the material will change from the high resistive amorphous state to the low resistive crystalline state by which not only a single bit but multiple bits (MLC) can be stored per cell over extended periods of time. Recently, a two bit logical cell paradigm for the Phase Change Memory has Been demonstrated which means four states of various degrees of crystallization are possible enabling twice as many bits to be stored in a cell with same physical area. The four resistance levels can be used to store the bit combinations of 00, 01, 10 and 11 respectively depending on the phase and the strength of the electric or voltage pulse applied. The Multilevel Phase Change Memory is much more apt and reliable than the main memory for its distinguishing properties. Due to the multilevel or the multi-bit storage in advanced PCM, the storage density of the later is almost 4x the former. Multilevel PCM advances over the DRAM not only because of the static energy consumption but also due to several issues like that of scalability for future technology generations which remains a big problem for the DRAM based main memory systems as far as the future computing is taken into consideration. According to Dr. M K. Qureshi of the IBM research, "The need for memory capacity continues to increase while the main memory system consisting of DRAM has started hitting the cost and power wall. An emerging memory technology, Phase Change Memory (PCM), promises much higher density than DRAM and can increase the main memory capacity substantially"[4] .

II. Drawbacks Of Dram Based Main Memory

Memory is the workspace for the computer processor. It is an area where data and programs that are being executed currently reside. The main memory system is temporary because the data remains there till the electrical power is not switched off. Before the system is to be shut down the data is to be saved in more of a permanent storage device so that it can be further used or reloaded for future uses. The computer memory hierarchy consists of the primary, secondary, and the tertiary storage respectively, the main memory which consists of the RAM is volatile in nature which is a prominent disadvantage of it and the question remains why use volatile memory as primary memory. On the instant the start-up operation of the computer is performed, the Central processing unit derives data from the RAM and performs POST (power on self test), loads the BIOS from the RAM and the operating system from the hard disk drive into the RAM. Opening an application will load it into RAM from the respective storage device and closing it will delete the file from RAM. The computer consists of hierarchy of memory systems which means loading every program to RAM from the secondary and tertiary memory systems which is a time consuming operation and increases architectural complexity. The main memory has permanent and temporary storage areas in which data is stored and loaded. The temporary storage areas consists of the cache memory, RAM and the virtual memory. Cache is a type of memory which stores the data which is to

be used very often and the processing of it occurs very often. The permanent storage areas include the ROM, hard disk drive, removable drives and network storage. When an application is run, the file is first loaded into the RAM and remains there till the execution is not completed.

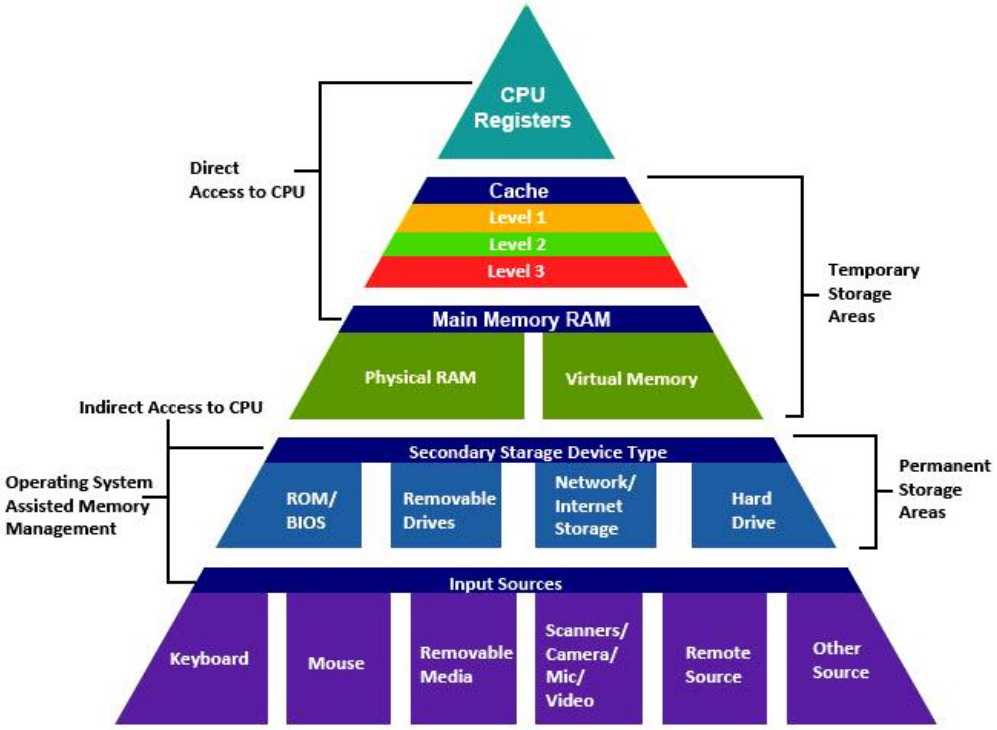

FIGURE 2: The computer memory hierarchy. [3][4]

Once the application is closed, the file is deleted from the RAM and this completes the execution cycle of the respective application. Accessing the temporary storage areas to find the data or file required and moving them to RAM every time the application needs to run is a tedious job even for the computer. The cache memory cannot store enough data as it has size restriction. Thus, the memory system has so many memories in hierarchy which increases the complexity of the design.

III. BACKGROUND

In 1950-1960, Dr. Stanford Ovshinsky of Energy Conversion Devices began researching on the properties of a class of special class of materials called Amorphous materials.[3] Amorphous materials are those materials which doesn't possess or exhibit any ordered crystalline structure. In 1969,Charles H. Sie published a dissertation at Iowa State University on chalcogenide phase change memory devices. These classes of substances have a characteristic of changing from one state to another on application of a current pulse, the states being amorphous state with high resistance and crystalline state with low resistance and definite crystalline lattice. In the September 1970 issue of Electronics, Gordon Moore co-founder of Intel published an article on the technology and unveiled the world's first 256 bits semiconductor device which was the world's first Phase Change Memory workable device. However, due to the material's quality and power consumption issues the commercialization of the technology was not done.

More recently, interest and research have resumed as flash and DRAM memory technologies are expected to encounter scaling difficulties as system or the chip shrinks.

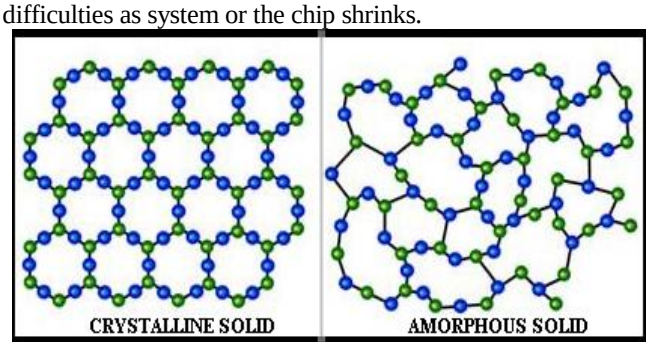

FIGURE 1 shows the chalcogenide materials (GST) phases i.e. amorphous and crystalline respectively.[3]

In 2000, Intel and ovonyx announced their collaboration over the technological development and research of the Phase Change Memory after which Intel agreed to co-develop a 90 nm PCM technology. In 2008 ST microelectronics and Intel formed Numonyx for further accelerating progress in the development of PCM which resulted in first

commercial PCM product in 2008. Since 1970, when the first significant development was made much of the development has been made in the semiconductor technology which has opened ways for the advancements in PCM for both optical as well as electronic storage devices. Phase change materials for many years have been used in re-writable CD's and DVD's.

The electrical resistivity of the materials in amorphous and crystalline phase are different which is the main reason to why data can be stored using these materials. A high resistance state i.e. amorphous state is used to represent a binary 0 and the low resistance state of crystalline materials represents a binary 1. Chalcogenide materials are being used in re-writable media of optical class such CD-RW and DVD-RW and the principle of storage being manipulation of the optical characteristics of these devices rather than electrical resistivity .PCM is not being commercially used in the electrical devices but are employed in nearly all prototype devices. These make use of the alloy of the chalcogenide materials i.e. germanium, antimony and tellurium which is commonly known as GST materials.

The Phase Change materials work on basic that when a solid is cooled down than it solidifies and this state is known as crystalline state .When the same material is cooled very rapidly then it changes into a meta stable state where the lattice of the resulting structure is not defined this state is called amorphous state and the glass formed is amorphous solid .The structures of the crystalline and amorphous solid are different, hence they have different properties which is why they can be used in the concerned technology.

IV. Si Ngle Vs Multilevel Cell Prototype (Slc And Mlc)

The PCM material offers a wide range of resistance between the amorphous and crystalline phases, thus making it possible to store multiple bits in a single cell which is called the multi level PCM. Multi level PCM is denser than the ones which can store only one bit per cell. In MLC devices the data is to be read precisely on the basis of the resistance value which is the reading parameter. The number of levels increases exponentially as the number of bits per cell increase i.e. the range dedicated to a single bit in terms of resistance decreases which in turn increases the storage capacity of the device accordingly.

The read latency of the MLC phase change devices can increase linearly or exponentially with number of bits a cell stores. Furthermore, the endurance capacity of MLC is much more than that of SLC which makes it ideal for memory technologies. Also, PCM in terms of MLC has much more to offer in terms of power, energy which not only increases the lifetime of the device but also makes it more powerful than the devices with SLC's.

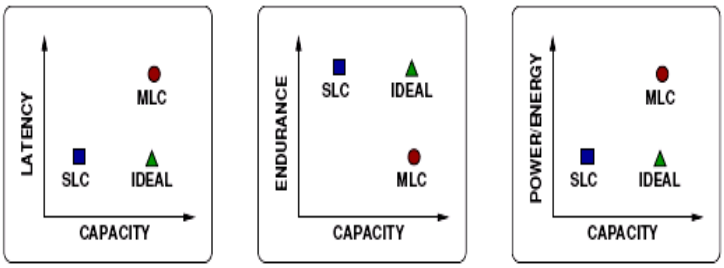

FIGURE 3.1 shows the comparison between SLC and MLC Phase change memory devices respectively[13]

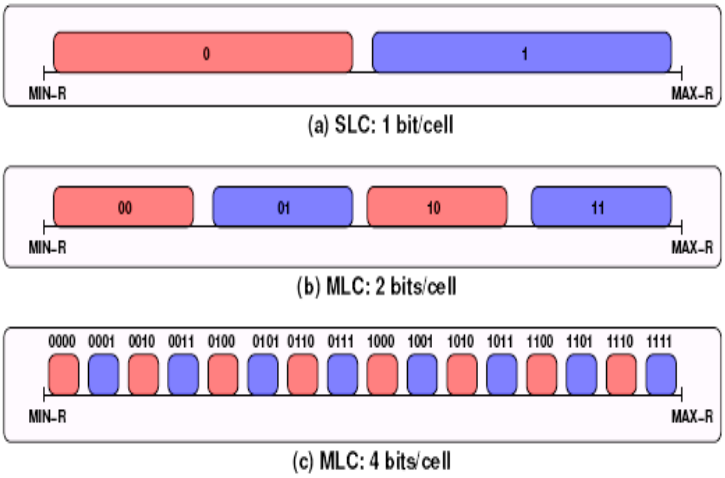

FIGURE 3.2 shows the concept of MLC phase change memory [11].

V. Operating Principle – Multilevel Pcm

The PCM cell works by the application of a current or electrical energy at a voltage above the switching threshold. Devices which have build-in PCM are programmed by electrically transforming one phase into other (amorphous or

crystalline) of a small volume of chalcogenide alloy. Depending on the current supplied, the cell is programmed into a high or low resistance state (phase transition process). Phase transition process can be completed as early as 5 nanoseconds. Information stored in the cell is read out by measurement of the cell's resistance.

VI. Multilevel Pcm Prototype

This part of the paper describes the PCM cell and working of the Multilevel PCM cell in a given environment. DRAM is the basic building block of main memory [5] which is made up of capacitors which stores the information in form of bits. In Multilevel phase change memory we use special material called the chalcogenide substances to store data bits in form of resistance. On using different alloys of GST materials [6], we can obtain two stable structural states namely; the Amorphous and the Crystalline state. We have a standard melting point (600 degrees) for these substances, which when heated quickly above the melting point changes into the GST into its amorphous state and when heated about 300 degrees slowly and uniformly the same changes into changes into the crystalline state. The change of GST into amorphous phase corresponds to logic 0 i.e. RESET state and that into crystalline phase corresponds to logic 1 i.e. SET state in PCM while in Multilevel PCM we represent bits 00,01,10,11 through four distinct states.

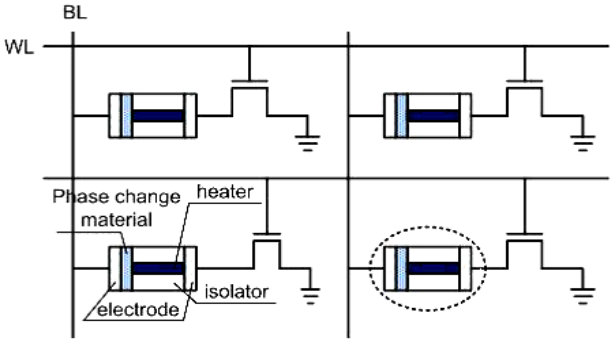

FIGURE 4.1 shows a 2x2 cell structure of the PCM which consists of phase change material sandwiched between two electrodes. [11]

PCM cells are same as the DRAM ones except one difference in the material of the cell in case of PCM being the Phase change material. Also in DRAM based main memory, DRAM not only places charge in storage capacitor but also moderates the charge leakage in the cell. The cell also consists of a heater, a thermal insulator and a transistor. It can also use the same logic as the DRAM array like the decoders, buffers etc. Now for performing read/write operations we require different current densities for different periods of time. In the RESET operation the cell requires high voltage for small amount of time whereas for SET a uniform less voltage pulse is need for the operation.

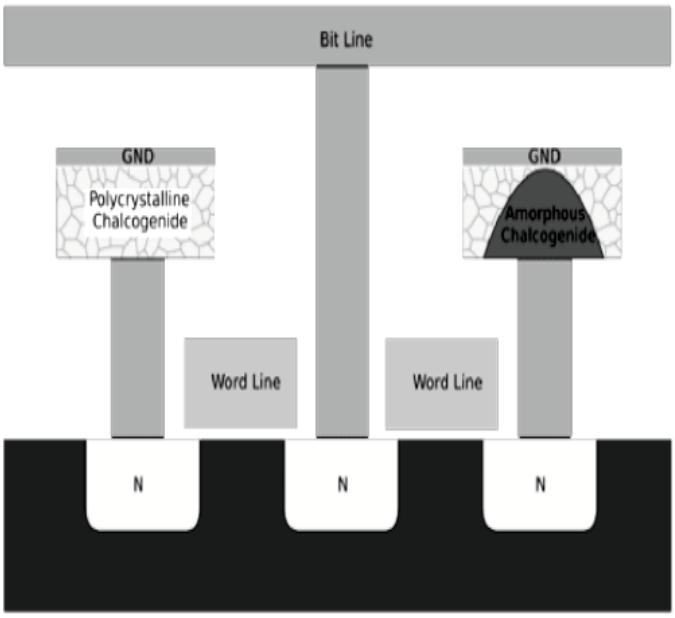

FIGURE 4.2 Two PCM Cells in Crystalline (SET) and Amorphous (RESET) States. [12]

When the thermal energy is applied to the phase change material with the help of electrical pulses, the phase change material changes its state depending on the intensity and time duration of the thermal energy. The multi bit storage can be done by controlling the amount of amorphous material formed, this storing data bits in the range of electrical resistance.

VII. Comparison Between Dram And Multi Level Pcm Attributes

Multilevel PCM is a dense as well as powerful technology in comparison to the DRAM based main memory. Presently, the main memory is giving problems in areas like the scalability, storage density and the most important of all cost and power issues. The Phase Change Memory has excellent scalability, low Read/write latency, and high endurance (cycling) and has far much more superior performance than Flash memory which is the most Pervasive non-volatile memory that is widely being used today.

PARAMETER	DRAM	FLASH	PCM	Multilevel PCM
TIMEFRAME	1966	1980	Available in limited quantities	2016
SCALING	Average	Adequate	Best in class	Best in class
RETENTION	Bad	Best in class	Best in class	Best in class
SPEED	Average	Bad	Optimal	Average
DENSITY	Average	Best	Average	Best in class

Table 1 shows the data over various parameters obtained from [2][3][5][7][9] .

The memory technologies that have the potential either to replace or to contribute in a hybrid memory system are the flash memory and the advanced version of the phase change memory i.e. Multi-Level Phase Change Memory which has comparatively much more storage density than the PCM. When a comparison between the Flash and the Multi level Phase Change Memory is made it is found that the later is much more capable of the flash much more capable of the flash in terms of speed, scalability and retention. The phase change materials are already being used in secondary storage devices. Flash memory is already being replaced by the PCM since it doesn't require a time consuming erase before rewriting which makes it much faster than the flash memory.

Scalability

With the need of the customers, the technology is getting handy that is the cost and size ratio is decreasing. With systems getting smaller, the cell size in the DRAM based main memory is also getting smaller. According to Moore's law as the technology gets smaller the memory should get denser. But in DRAM when the cell size gets reduced, so is the number of electrons present per cell which creates problems in current induction. Also with the size of the gates almost constant it is impossible to decrease the size of the main memory. This is one of the biggest problems in current memory system. Thus, scaling the systems is a necessary and also a complex objective in current computers. In volatile main memory systems , for DRAM the main job is not only place charge from the thermally induced charge in a storage capacitor but must also let through or lessen the threshold charge leakage through the access device. Capacitors must be large enough to store charge for reliable scaling and also transistors must be sufficiently large for exerting effective control over the device channel for current flow. Given these challenges, manufacturable solutions for scaling DRAM beyond 40nm are unknown [13].

In multilevel Phase Change Memory, the current is analog current is induced thermally[1] and does not require control of discrete electrons also as the size of the memory cell decreases so does the size of the phase change material which eliminates this issue. Thus, scalability is one of the biggest motivations in the development of multi level PCM.

Non Volatility

Like Flash memory (NAND and NOR), the multi level phase change memory is non-volatile which is one the biggest advantages of the technology. DRAM requires a constant power backup and as soon as the electrical supply is turned off, the data stored in it is deleted. Thus, DRAM based systems have to have an additional power backup which results in higher power consumption. No such problem is there in PCM or multi level PCM.

Data Retention

The data retention capability of the DRAM based main memory system is also less than multilevel PCM[9]. Since the DRAM based main memory is a charge memory ,the leakage that occurs from the memory cells at a lapse of time leads to the data retention in main memory at cycles of time which is not appreciable. In Multilevel Phase Change memory, data can be retained over period of 10 years without any leakage from the cell.[11]

Speed Speed is an important factor for any of the memory system as it determines the overall performance of the same. The Read latency of the Multilevel Phase change memory is about 5 times than that of DRAM based main memory which enables the PCM to be implemented without a cache memory. The write latency of the multilevel PCM is comparable.

Storage Density

Currently a main memory system of a magnitude of five order is being used. The physical area of the cell hampers the storage density of the memory as far as scaling of the memory technology is concerned. Multilevel Phase Change memory is capable of storing 4 bits instead of one in the same physical area which makes is 4x denser than the main memory.[1][9]

Power and Cost Issues

Being a charge memory when the electron density per cell decreases more voltage is needed for current induction which triggers more power supply and hence more cost indulged. If we see the current computing system, a significant amount of power is diverted to the memory unit for its operation. In a system consisting of multilevel phase change memory, power consumption is 40% less due to the fact that PCM is a resistive memory.[6][7]

VIII. Future Scope of The Multi Level Pcm

The need for memory capacity continues to increase while the main memory system consisting of DRAM has started hitting the cost and power heights. A more of a economically feasible and scalable memory is needed to meet the requirements of the future computing systems, servers and cloud computing system. In the midst of all, the multilevel phase change memory can be proposed as a replacement of the current memory system.

A memory which will lead to much economic, a lot speeder and powerful systems than those present today. This new storage class memory. Multilevel PCM scalability implies lower main memory energy and greater write endurance. Furthermore, non-volatile main memories will fundamentally change the landscape of computing. Software cognizant of this newly provided persistence can provide qualitatively new capabilities. For example, system boot/hibernate will be perceived as instantaneous; application check pointing will be inexpensive; file systems will provide stronger safety guarantees.[5] 90nm PCM device has already replaced NOR[9] while the material and thermal properties of the device pave way for advancement of the technology and to be used in the variety of applications.

Thus, Multilevel PCM as main memory when completely developed will enable a paradigm shift in the modern computing towards powerful computing.

Acknowledgments

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