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A Review of Various Trends of Digital-To-Analog Converter with Performance Characteristics and Behavioral Parameters

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Abstract— The CMOS technology which is really shrinking day by day which favors digital circuitry but it is challenge to the analog designer as there are some limitations such as process gradients and random device variations. Digital-to-analog converters (DAC's) are one of the essential class of analog blocks facing high performance demand and DACs are so closely tied to digital circuitry that they are likely to be included in an ASSP or a SoC. Digital-to-analog converters (DACs) Comprises voltage or charge or current based elements which includes resistor string i.e. voltage, charge redistribution i.e.(charge) and current source type i.e.(current). The Digital-to-analog converter (DAC) will convert all combinations of number of bits from digital form into correspondent levels which is depend upon the design of type of converter (DAC). In this paper we reviewed design basics and also various functional specifications for various digital-to-analog converters (DACs) are covered. Outlines of digital-to-analog conversion principles, together with various DAC architectures, are briefly explained. The effectiveness of various technologies and its application to high-accuracy DACs are covered.

Keywords— CMOS, DAC, R-2R, and resistor string, current steering, weighted capacitor, etc.

I. INTRODUCTION

Highly integrated wireless communication systems require a modular which is universal design of all the components included in the radio frequency (RF) subsystem. Basically, design of RF system consists of connecting modules to each other which form a receiver/transmitter chain including components such as a power supply, antenna, baseband layer, and other interfaces, constitute a radio system. Particularly, radio transmitter front-end architectures are consist of a digital signal-processing (DSP) stage, a digital-to-analog converter (DAC), analog circuitry (modulators, filters, etc.), an RF power amplifier, and a transmitter antenna. Digital-to-analog conversion is generally transform the digital input signal into a corresponding analog output signal. Basically, a discrete-amplitude; discrete-time digital input signal is converted into a continuous-amplitude, continuous-time analog counterpart. A block diagram of a DAC, together with the digital input and output (continuous analog signal) signals, are shown in Figure 1. According to Figure 1 an N-bit digital signal that can only have 2N values is converted into an analog signal (voltage or current). Here the input digital signal is a binary-coded representation of an analog signal using N bits. The leftmost bit of the input digital word is usually called the most-significant bit (MSB), and the rightmost bit is called the least-significant bit (LSB).

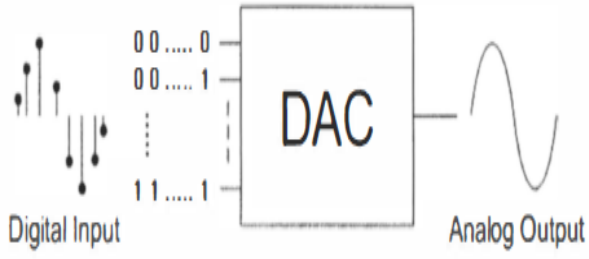

Figure 1.Digital to Analog Converter

Generally CMOS current mode DACs are the very much for many applications because of their high speed, low power, and cost effectiveness. Moreover, the DAC can equally be used in an ASSP, as a standalone chip, or as a precision analog intellectual property (IP) block for SoCs. High performance current-steering DACs find applications in the area of wireless transceivers such as Wireless Local Area Networks (WLAN) and Wireless Metropolitan Area Networks. (WMAN), image signal processor such as High Definition Television (HDTV), digital signal synthesizers, and etc.There are several digital to analog architectures for DAC designs which includes resistor string, R-2R ladder networks, charge scaling, current steering, and segmented current steering. Most of them could not able to avoid glitches

because of the change of more than one digital input bit at a sampling time or can be suffered by noise problems since resistors are noise sources. Because of which DAC output dose not result in expected value. Also as per as area is concern DAC chip is big because passive components have large area and their static characteristics are not good because of more differential nonlinearity (DNL) errors occur at higher resolution. The strengths and drawbacks of each architecture are evaluated by parameters such as integral nonlinearity (INL), differential nonlinearity (DNL), monotonicity.

II. ARCHITECTURE TRENDS OF DAC

Among the many existing DAC architectures, the high-speed market segment is widely dominated by current-steering flash topologies.

• Current source DACs are unrivaled for very high-speed conversions up to the gigahertz range. With high ac performances they are a natural choice for communication applications (GSM, *x*DSL, HDTV).

• Inverted R2R ladders offer high precision in the Megahertz range. With high trimmed dc performances, they are favored for high absolute accuracy applications (sensors, instrumentation, and digital waveform generation). These DACs generate radioed reference currents which are added to the output according to the digital input word. Speed is enhanced by steering any unused current source to a complementary output thus avoiding any shut-down and power-up delays in current sources. Flash DACs resolution is mainly limited by the level of matching reached between all reference current sources and many different solutions have been explored to cancel mismatch errors caused by gradient and random variations: careful layout, and other special techniques such as improved switching schemes and dynamic element matching (DEM) can reduce the mismatch effects to a certain extent. However, over 10–12 bits of resolution the matching requirement is such that some sort of calibration must be used to obtain the desired full accuracy. There are several different topologies for DAC which are design with the help of CMOS technology, for example resistor ladder architecture, resistor string architecture, current steering architecture, etc

A. Resistor ladder architecture

Another DAC is called R-2R ladder network which consists of resistors R and 2R. For example, analyzing a 3-bit resistor ladder DAC is as follows:

Mathematically analyzing this ladder network is a bit more complex, a where each input resistor provided an easily calculated gain for that bit. Thevenin's theorem and simulation program like SPICE can be used for each binary input to determine circuit response.

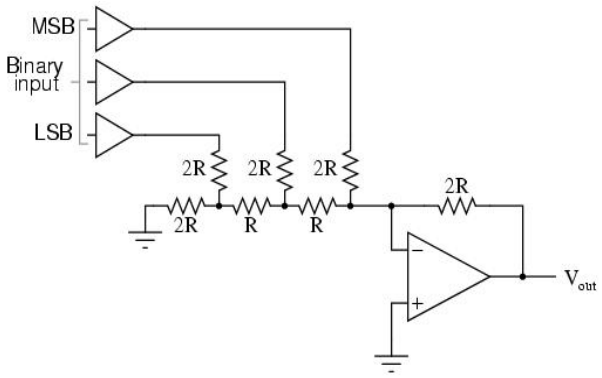

Fig 2. R-2R ladder network D/A converter system

B. Resistor string architecture

The simplest DAC topology is resistor string architecture. It consists of 2N identical resistors and switches, the analog output is the voltage division of the resistors. This structure results in good accuracy and is inherently monotonic. The disadvantage of this topology is that the output is always connected to 2N -1 switch in "off" state and one switch in "on" state. When resolution becomes a big value, a large parasitic capacitance appears at the output and conversion speed becomes much slower. Also this architecture occupies large area.

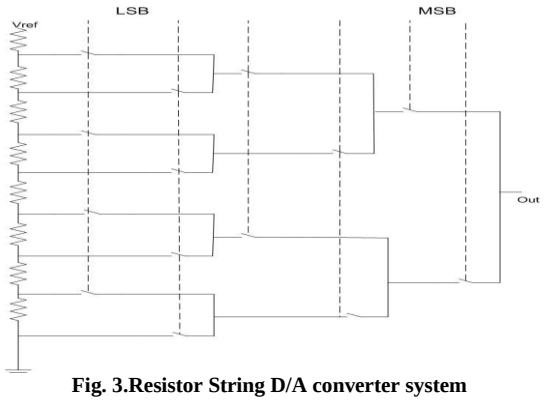

Fig. 3.Resistor String D/A converter system

C. Current steering architecture

Current steering architecture replicates a reference current source rather than divides it in each branch of the DAC. Each branch current is switched on or off based on the input codes. The architecture can achieve high speed at the cost of complex structure and relatively large power and chip area. The key part is a precise current source.

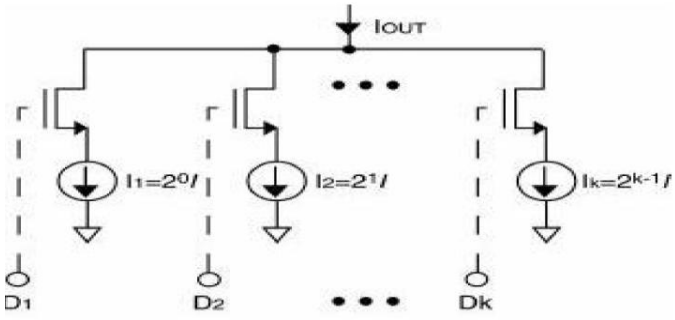

Fig 4.Binary current steering D/A Converter system

D. Weighted capacitor converter architecture

In a MOS technique capacitor with MOS switches performs an identical operation as resisters and transistors in a bipolar technique. Fig shows that system consist of n binary weighted capacitor , an additional capacitor with unit capacitance C and set of switches that can connect the weighted capacitor to the reference voltage Vref. Reset discharges all the capacitor with the digital input at 0.At the start of conversion all the capacitor are discharged & the reset switch is opened. The capacitors are connected to reference voltage or remain connected to ground depending on the digital input code. A charge distribution occurs and finally at the output reconstructed analog value is obtained. Furthermore the layout of capacitor must be in such a way that the wire connecting every capacitor to the output terminal has the same binary weighted value. This is requiring maintaining an accurate binary weighting of this network.

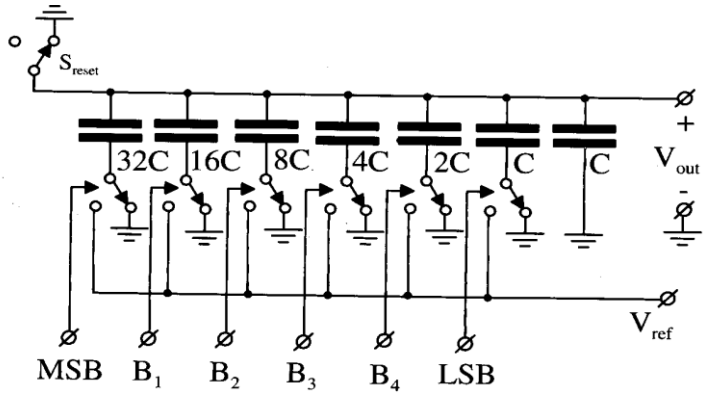

Fig 5.Weighted capacitor converter system

III.PERFORMANCE CHARACTERISTICS AND PARAMETERS OF DAC

There are different parameters of DAC. Some are explain below:

A. Resolution

The number of bits used to generate the analog output is called resolution. Resolution is normally expressed in bits which determine the number of analog output levels that can be produced by the DAC. This is the smallest possible change in output voltage as a fraction or percentage of the full-sale output range. For example, for an 8 bit converter, there are 28 or 256 possible values of analog output voltage. Hence the smallest change in the output voltage is1/255th of the full scale output range. Its resolution is one part in 255, or 0.4 percent.

B. D/A speed

The speed of D/A converter is defined as the amount of time required to settle to a particular accuracy. This speed is Conversion rate at which a DAC can produce repetitious data conversions at the output. Usually, it is specified in samples per second.

C. Linearity

In a D/A converter, equal increments in the numerical significance of the digital input should result in equal increments in the analog output voltage. In an actual circuit, the input-output relationship is not linear. This is due to the errors in resistor values and voltage across the switches. Differential nonlinearity (DNL) and integral nonlinearity (INL) are use to characterize Static performance of DAC. Differential nonlinearity expresses the difference between the actual step size and the ideal least-significant-bit step size, i.e., Differential nonlinearity is a measure of the deviation between

the analog output levels corresponding to two successive (in binary value) input codes from the ideal one-least-significant bit step. A measure of the deviation of the DAC output from the output provided by an ideal straight-line transfer characteristic is called Integral nonlinearity. The ideal straight line can be drawn as an endpoint line, passing through the zero and full-scale points .For an N-bit DAC, endpoints are usually given as the analog outputs matching with code 0 and 2N - 1 or as a best-fit line to the DAC's actual transfer characteristic. The unit of measure of differential nonlinearity and integral nonlinearity is one least-significant-bit step size. Figure 6 shows Non-ideal output of a three-bit DAC, differential nonlinearity and integral nonlinearity.

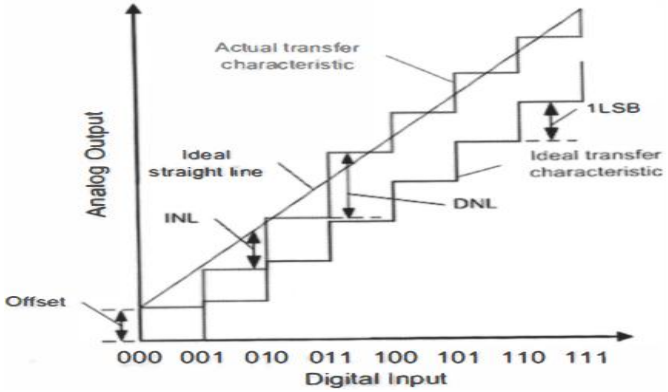

Fig 6.Transfer characteristic of a three-bit DAC, differential nonlinearity and integral nonlinearity

Differential nonlinearity can be given in terms of least-significant-bit step sizes with the normalize form in Equation (1)

$$DNL_k^{norm} = \frac{A_{k+1}^{actual} - A_k^{actual} - \Delta_{LSB}}{\Delta_{LSB}} \quad ...(1)$$

where A_{k+1}^{actual} and A_k^{actual} are the analog outputs corresponding to adjacent codes of the converter. DNL_k^{norm} is the differential nonlinearity normalized to the least-significant-bit step, Δ_{LSB}.Integral nonlinearity can also be described as the accumulation of previous differential nonlinearity errors, and given in terms of least-significant-bit step sizes with the normalized form in Equation (2)

$$INL_k^{norm} = \frac{A_k^{actual} - A_k^{ideal}}{\Delta_{LSB}} = \sum_{j=1}^{k} DNL_j^{norm} \quad ... (2)$$

Where A_k^{actual} and A_k^{ideal} are the actual and ideal analog outputs of the converter. INL_k^{norm} is the integral nonlinearity normalized to the least-significant-bit step, Δ_{LSB} .

D. Monotonocity

A D/A converter is said to be monotonic if its output voltage increases regularly as its binary digital input signal is increased from one value to the next value. A monotonic DAC has an analog output that never decreases with an increasing decimal value corresponding to the digital input code, and conversely.

E. Accuracy

The accuracy of a D/A converter is a measure of the difference between the actual output voltage and the expected output voltage. It is specified as a percentage of full-scale or maximum output voltage.

F. Setting time

It is the time required for the analog output to settle within (1/2) LSB of the final value after a change in the digital input. Settling time should be kept as small as possible to keep the distortion on the analog output signal low. Figure 7 shows a full-scale transition for a DAC's output, the settling time.

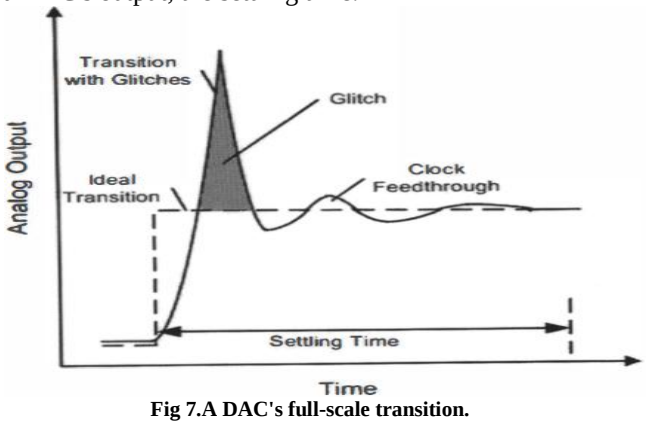

Fig 7.A DAC's full-scale transition.

G. Temperature sensitivity

The analog output voltage for any fixed digital input varies with temperature. This is due to the temperature sensitivities of the reference voltage source, resistors, OP-AMP etc.

IV. Conclusion

Performance Characteristics including various parameters and the design basics of DACs, widely used in communication applications, have been discussed. The main conclusions drawn from this paper are, the proper design of a DAC starts with the analysis and interpretation of the given specifications, which depend on the application. It is important to know possible limitations of the DAC and how they affect the performance of the entire system. Various architectures can be used for the implementation of the DAC. Through a standard design methodology and considering the tradeoffs among performance parameters, the designer thus has to ensure the required performance of the DAC. Prior to transistor-level design analysis of the DAC is required in order to gain full insight into the DAC's non-ideal behavior.

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