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A Review on Effectuation of Serial Communication Inter-IC Protocol

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Abstract— Embedded system mainly uses serial communication to communicate with peripherals. Therefore serial communication plays vital role in embedded system design. Many serial communication protocols are used like Universal Asynchronous Receiver Transmitter (UART), Control Access Network (CAN), Universal Serial Bus (USB), Serial Peripheral Interface (SPI) and Inter IC Protocol (I^2C).Serial communication protocol have characteristic of high speed and low data loss and it simplifies system level design and ensure data transfer. Inter IC protocol satisfy the requirement of embedded system of less number of wires for interconnection. Implementation of inter IC protocol on FPGA gives flexibility to use it according to application. This paper provides reviews use of I^2C protocol with prelude of FPGA implementation.

Keywords— Inter-IC (I^2C), SCL, SDA, FPGA

I. INTRODUCTION

This document is a template. An electronic copy can be downloaded from the conference website. For questions on paper guidelines, please contact the conference publications committee as indicated on the conference website. Information about final paper submission is available from the conference website. Embedded system technology is growing very rapidly for various applications. Use of microcontroller in embedded system increases according to that different peripherals are also used such as Analog to Digital Converter (ADC), Liquid Crystal Display(LCD), sensors, memory and Application Specific IC (ASIC). To communicate with these peripherals serial communication is used. Serial communication is advantageous because it communicates without shared memory, low pin count and collision rate is very low. There are different types of serial communication protocols are present like Universal Asynchronous Receiver Transmitter (UART), Control Access Network (CAN), Universal Serial Bus (USB), Serial Peripheral Interface (SPI), Inter-Integrated Circuit (I^2C).Each protocol has certain advantage and disadvantage depends on application. SPI and UARTs can communicate from one point to another point only.USB use multiplexing technique to communicate multiple devices while CAN and I^2C useful for software addressing of receiver. CAN and SPI protocol are beneficial protocol in communication but CAN is complex to design and have limited portfolio so it is not used in general communication. If we consider SPI protocol which has advantages of low cost small and easy to design but if peripheral increases the number of interconnects also increases. Hence not useful for communication purpose where peripherals are more. I^2C is protocol is two wire protocol which is easy to design. I^2C is useful in network where adjustment of node is to be done and low speed has to be maintained.

II. INTER-IC PROTOCOL

An easy way to comply with the conference paper formatting requirements is to use this document as a template and simply type your text into it. In an embedded system physical size of device get reduce due to reduction in size of transistor but as number of components or ICs increases on devices, interconnects also increases which creates problem. To overcome this problem Philips Electronics design protocol for communication between different integrated IC called as Inter IC protocol. Many electronics appliances such as Liquid crystal display (LCD), memory, keyboards, cell phones, PCs, TVs use I^2C protocol for communication. I^2C bus physically consists of two active wires namely serial clock line (SCL) and serial data line (SDA). SCL and SDA both are active high bidirectional and half duplex in nature. Each device which is connected to these wires has unique address. Each device can act as transmitter or receiver depending on its nature. The I^2C bus is a multi-master bus. This means that more than one IC capable of initiating a data transfer on the bus is considered to it. I^2C provides low cost and efficient link between ICs. It is synchronous protocol in which master initiate data communication and data get exchanged between master and slave. All communication is control by master using SCL line. All slave connected with SCL line. Slaves are controlled by same SCL line. SCL and SDA line avoids collision of data by using clock stretching

There are two bidirectional wires SDA and SCL connected to a positive supply voltage via a pull-up resistor as shown in Figure 1. When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector in order to perform the wired-AND function. They are pulled-up to the logic 'high' level by

resistors connected to a single positive supply, usually +3.3 V or +5 V. All the connected devices have open collector driver stages that can transmit data by pulling the bus low and high impedance. [6]

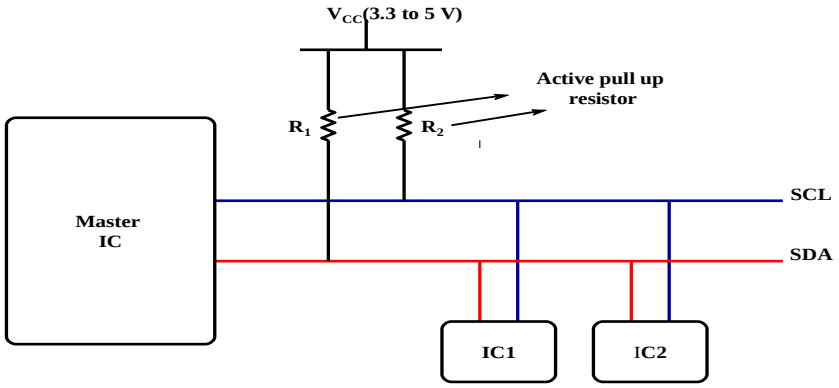

Fig. 1 Schematic representation of devices with I^2C bus

The I^2C is governed by certain frame structure which is byte oriented. Slaves gives start signal to the master which then follows slave address and data direction. Data direction means write or read. The slave addressing can be 7 or 10 bit and data direction means receiving (read) or transmission (write) data. Write operation is also term as transmission of bytes to particular receiver. This operation depends on frame structures third bit whether it is read or write bit. The '0' bit means write and '1' bit means read.START condition is when SCL is at logic high and SDA has transition from high to low while STOP means SCL is at high position and SDA transition from low to high.

Initially both SCL and SDA are active high due to active pull up resistor. For start condition SCL should be active high while SDA is low. At each clock cycle frame structure contains address, read or write bit and ACK is received. Reception of ACK means proceed otherwise it restart again. The process of data reading and writing will continue till stop signal arrives. After STOP signal SCL and SDA will be again high.

III. IMPLEMENTATION OF I^2C

To increase in speed of operation of embedded system, effective protocol has to design. Many researchers proposed different model to implement inter IC protocol which helps to control various applications. Some of the models are summerised below.

Sahu *et al.* developed inter IC protocol for data surveillance purpose. Data surveillance is very important application to monitor people or sensors.I^2C is used for data surveillance because it could make system efficient, accurate, flexibility, and low development cost. They designed a protocol in VHDL and interface with OV7620 single chip CMOS VGA color digital camera. Data surveillance includes monitoring people or collection of sensors information from various nodes. They developed system which will replace traditional cameras with LAN cameras with complex image processing and IP routing. Data compression takes place with H.263 algorithm due to its high compression efficiency and high data rate. For surveillance constant bit rate limit the real time communication of cameras so variable bit rate is used. Variable bit rate efficiently uses available bandwidth.H.263 encoding is very complex normal DSP processor cannot handle it so FPGA as programmable solution is used. All results were verified using Modelsim and FPGA can be used as interface in between camera and local monitor system.[1]

shah *et. al* designed inter IC protocol using system verilog and FPGA. Design mainly includes master design and slave design. Master design was implemented in medium size FPGA and its computation was performed on 32 bit Microblaze processor which performs all encryption and decryption. Design contained different register as prescale register, command register, status register, transmit and receive register. Status register contains information about status of pins. Command register contains command as start, stop, write, read. Transmit and receive register contains data of transmission and received. Byte command controller was main unit of design which controls data in terms of byte. Design of interface includes design of master byte controller, master bit controller which then connected to SCL and SDA line.[2]

Some researchers developed Inter-IC protocol with volume controller application. WM 8731 sound driver was used in MP3 audio or speech players. The designed interface was used to control features like volume control, mutes and power management. For designed purpose state machine model approach was used because it keeps track of operation from one state to another. A main tool used to design protocol was VHDL and Verilog. Assignment of pins can be done with assignment editor. Joint test action group (JTAG) programming was used and for simulation results validated using Modelsim- Altera 6.5b (Quartus II 9.1). [3]

Researcher developed an interface model for scale free network using inter-IC bus protocol which includes master and slave design. Master was made up of different blocks as initiator, address block, write block, read block, clock generator. Initiator tested whether data bus was free to use or not. Address bit was transmitted by address block bit by bit to SDA line and after completion of address it reset SDA line to high position. Transmission and reception functions were performed by write and read block. All functions of master are governed by clock generator block. Slave was made up of design of monitor, address block, receiver and transmitter. Monitor function was same as initiator in

master which sense the SCL and SDA line whether it is in use or not. Other blocks were functioned same as master block. Quartus II 6.0 was used to create VHDL model while it is simulated in Stratix II. [4]

Jesus lazaro *et al*. A chip to chip communication protocol was proposed using AES-GCM cryptographic and authentication algorithm. Advanced Encryption Standard (AES) was specification for encryption of electronic data. Galois/Counter Mode (GCM) was mode of operation use to encrypts data because of its efficiency and performance. AES along with GCM algorithm used for secure data flow between devices. Embedded system along with sensor had played vital role in industrial application but problem with system security and privacy of data. Implementation of protocol along with AES-GCM algorithm gives strong computation and flexibility capability along with security of data. [5]

IV. SYSTEM DEVELOPMENT

The prelude of the systems explained above is to implement inter IC protocol. For Inter IC system development master and slave has to design. Design can be developed using Active HDL 9.1 software.

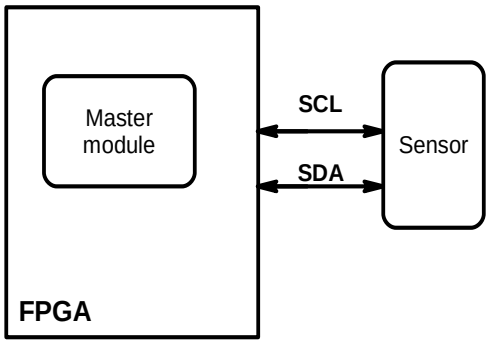

Fig. 2 Proposed block diagram of inter-IC

Design may contain two units as master unit and slave unit. Master and slave design can be embedded into FPGA. It can have two outputs as SCL and SDA. The outputs communication can be validated using EEPROM AT 2408 series or using sensors like RTC DS1307.thus FPGA can work as dedicated interface between different devices foe communication

V. CONCLUSION

This paper reviews about implementation of I^2C protocol. This protocol uses serial communication protocol which reduces the requirement of wires in embedded system. It is useful in terms of number of pin count and with easier controlling. Implementation of I^2C on FPGA is beneficial for data processing, minimal coding and faster operation. Implementation of protocol on FPGA aids in development of dedicated hardware for various applications

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