



An Overview: RF Design of Fast Locking Digital Phase Locked Loop

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Abstract— Phase locked loop (PLL) is a control system that generates a signal having a fixed relation with the phase of a reference signal. This system responds to both frequency and phase of the input signals, automatically raising or lowering the frequency of a controlled oscillator until it is matched to the reference in both frequency and phase. The performance of PLL is primarily dependent on the lock time, it is the time PLL takes to adapt and settle after a sudden change of the input signal frequency. It is desired to design a novel fast locking digital PLL. The high speed, high throughput applications needed for information technology demand that the lock time should be as small as possible. Fast locking is also of great importance for fast frequency hopping among data bursts in high-speed digital communications. Various technologies used for the improvement of the PLL design, to make it work faster are discussed in this paper.

Keywords— Phase Locked Loop (PLL), Injection Locked Frequency Divider (ILFD), Radiation Hardened Design Topology (RHDT), Single Event Transient (SET).

I. INTRODUCTION

A Phase Locked Loop is a device that generates a signal whose phase is having a fixed relation with the phase of the input signal. A conventional PLL consists of a phase frequency detector, charge pump, low pass filter and voltage controlled oscillator. The phase frequency detector compares the frequencies of input and output signal. The difference between the two is given to the charge pump, which converts the same into current. The output from charge pump is given to voltage controlled oscillator, which converts it into voltage with appropriate frequency. This signal is again compared with the input signal. In this way the input and VCO frequencies are brought close to each other. Once the two frequencies are same, the PLL is said to be locked. The process is called as phase tracking. This time which PLL takes to respond to change in the input frequency is called as lock time of PLL. Lock time plays most important role in the working of PLL. Ideally, the lock time should be as small as possible. Digital PLLs are used for wide range of applications including clock recovery, clock distribution and spread spectrum communications. [7]

The digital PLL generates a clock signal in synchronization with the incoming signal. Receiver circuits use this clock signal to provide clock to the shift registers to recover the data. This application of a digital PLL is often termed a clock recovery circuit or bit synchronization circuit. [9]

PLLs are widely used in applications like wireless transceivers, cellular phones, global positioning systems, etc. The locking time of the conventional PLL is quite high. Due to which they are not suitable for current high speed applications. PLLs with low-power constraints demand that they should be turned off during inactivity, but then require that they lock quickly when turned back on. Thus fast locking becomes necessity if PLL is used in the circuits like frequency hopping spread spectrum communications, clock/data recovery circuits, cellular phones etc. [8]

Fast locking circuits find its use mainly in applications like techniques based on a mathematical algorithm to achieve fast convergence, techniques based on nonlinear characteristics of the charge pump to change the convergence rate, techniques based on a feedback mechanism associated with the PD or the charge pump and techniques based on using current mode techniques in lieu of voltage mode techniques. [6]

Another important use of PLL is found in the pitch synchronization purpose. The best way of analysing a periodic signal is analysing its pitch synchronously. One approach to pitch synchronous analysis is sampling the signal at an integer multiple of the pitch frequency so that the samples within each cycle are uniformly spaced and the number of them remains constant. To do this, PLL is often needed as a frequency tracker and multiplier.

The conventional PLL however is not compatible to ever increasing networking speed. So it is required to design a fast working PLL and new technologies are needed to make the PLL work fast. The design for fast locking digital PLL with single charge pump after building and testing in Cadence is seem to be having some drawbacks. The charge pump was not able to react fast enough to the coarse tuning stage as expected. It was then easier to remove the digital to analogue converter and replace the single charge pump with a multiple one activated by a decoder which selects the charge pump suitable for a particular frequency jump (hop) at the input.

Another advancement that can be made in the design is replacing single frequency comparator with an array of comparators. Single comparator takes time to differentiate between the reference signal and the signal from the voltage control oscillator. While use of array makes it easier to trace difference between the two. The changes mentioned ultimately result in the reduced lock time which is the greatest need of the hour.

II. TECHNIQUES USED FOR ADVANCEMENT OF PLL

Cao *et al.* have designed a 50 GHz charge pump PLL with the help of an LC oscillator based Injection Locked Frequency Divider (ILFD). The PLL is constructed using 0.13 μm logic CMOS process. The locking range of PLL is 45.9 to 50.5 GHz and output power level is around -10 dBm. The PLL intended works at voltage from 1.5/0.8 V and consumes of 57 mW of power. Main motto of the work is to design the frequency dividers using CMOS technology operating at the maximum speed possible. The 1/512 static frequency dividers designed using SiGe BiCMOS technology lead to higher power consumptions. The drawback of high power consumption is removed using an ILFD. The operating frequency range is augmented combining an ILFD with an increased input frequency range. The VCO and ILFD self oscillation frequencies are tracked using this combination. Also the use of push-push VCO increased the output frequency to 91.8 through 101 GHz which is highest for silicon integrated technologies. The very first component in the design is charge pump which is very much similar to the conventional one. The dead zone problem in the charge pump is overcome using four inverters in the reset path of the delay cell. The pMOS or nMOS current sources control the output voltage of the charge pump. The leakage current is reduced using longer channel transistors. A 50-GHz Push-Push VCO is designed, in which the anti-phase fundamental signals cancel at the common-mode nodes of the VCO and the second-order harmonic signal are obtained. Ansoft HFSS, a 3-D EM simulator is used for the replication of S parameters of the transmission line. The third important component used in the design is a 50 GHz Injection Locked Frequency Divider. The phenomenon called oscillator injection pulling or locking is used which helps in pulling away oscillator output with the help of a continuous wave close to the oscillator's fundamental, super-harmonic, or sub-harmonic frequencies. For the convenient locking range and voltage swing the size of 0.18 μm /0.12 μm is preferred. When the ILFD is driven by the VCO on the same chip, the locking range extends beyond 1.8GHz. The locking range is further increased by designing such that its tank resonant frequency tracks that of the VCO. Hence the frequency of the VCO is tracked by the self-oscillation frequency of the ILFD which is around half of the VCO frequency. Deviation of the ILFD frequency distracts the working of the circuit. The main advantage of static frequency divider is its achievement of wider frequency range with much smaller area. The power consumed by the design is reduced by ten times as compared to the conventional SiGe PLLs.

The tuning range of the ILFD is increased to half of the VCO tuning range in future designs, in order to increase the margin. The establishment of a 50 GHz PLL is done using 0.13 μm CMOS. Need of advancement in push-push node is expected to reduce the effect of noise. This can be done by designing 192 GHz push-push VCO. A limit on the frequency of PLL is found because of the limited operating frequency of oscillator. [1]

Chow *et al.* have compared and classified different phase frequency detectors from the aspect of theoretical analysis and circuit operation, phase sensitivity, dead zone characteristics and maximum operation frequency. They have anticipated a high speed phase frequency detector for PLL design having superior phase characteristics with no glitch output. The simulations are performed on 0.35 μm CMOS process. The PLL designed is very much similar to the conventional PLLs with the operating frequency of 3.5 GHz. It is having the phase detector block, charge pump and the voltage controlled oscillator. The PFD compares both the phase and frequency difference between the reference input signal and the feedback signal. The LPF filters out the high frequency components of the output signal from the charge pump. While the VCO accepts this DC voltage from the low pass filter and then generates a corresponding output digital signal. Once the whole PLL loop becomes stable the output signal is synchronized with the reference input. There is ideally no phase difference.

The simulation results showed that the phase frequency detector designed were having reasonable circuit performance with elevated operation frequency, lower phase jitter and smaller circuit complexity. [2]

Hao *et al.* have designed a completely digital phase locked loop without any hardware component having modified 9-gate phase detector, a frequency multiplier and a loop filter. One of the important use of the PLL is as a frequency tracker. The conventional PLLs take time to transit from the original state to the steady state which is done in loop by searching the frequency. But this long process can be replaced by simply measuring the period of the first and second cycles of the input. This is the elemental idea used in this design which also helps in reducing the tracking time. The digital PLL is designed by combining ZC digital PLL and LL digital PLL in one loop. The advantage of directly using above digital phase modulator is that it can track the input frequency very fast. A 9-gate phase comparator is used in the design having three outputs indicating phase lag, lead and no phase difference between the two inputs of the phase detector. The comparator changes its state when the two negative adjacent edges of one input are captured by the two negative edges of another input, the process being called state reversing condition. The logic adjusting process takes place from the starting point to the point of state reversing condition. The frequency phase adjustment takes place at the very end of this process. The logic adjusting process takes more time when the frequency of two inputs is too close. With the help of short frame fast fourier transform, the pitch synchronous analysis used for the simulation purpose lead to better results for quasiperiodic signals. The locking and tracking speed however was found not to be so satisfactory which lead to further advancements in the circuit. The simulation showed that even when the pitch period was reduced from 154 Hz to 80 Hz that too in 32 cycles, the performance of the digital PLL was good enough.

The digital PLL designed showed high lock-in speed. There was no steady state frequency tracking error for period ramp input signals. Also the PLL was easy enough to integrate on a single chip. In spite of these good results of the PLL there are some drawbacks in the design. A steady state error was occurred between the input frequency and the VCO frequency due to the inherent quantization effects or the frequency variation of the input signal. No phase locked state was found even if the input frequency and phase remained constant due to which the steady state errors tend to accumulate. The low acquisition of the detector also came as the drawback of the design. [3]

Loveless *et al.* have proposed a radiation hardened by design (RHBD) topology for digital PLLs for single event transient (SET) mitigation. A SET resistant tristate voltage switching charge pump and a low-pass filter were used in the design instead of the vulnerable current based charge pump. It is clear from the simulations showed that a sufficient charge is deposited by a single ion strike in the output stage of the charge pump alters the frequency of the generated clock signal. The digital PLL considered in this work is very much similar to the conventional PLL and designed in 130nm CMOS process. The design is its centre frequency as 400MHz with the locking range from 150 MHz to 1 GHz. The output stage of the charge pump is directly connected to the capacitive node of the low pass filter, due to which a single event strike in this sector either depletes or deposits charge on the low pass filter capacitors, which ultimately affects the rate at which this deposited charge is removed by the charge pump determines the single event response of the digital PLL. The main function of the charge pump used in the design was to reduce the number of vulnerable nodes present in the charge pump, increase the rate of charge sourcing and sinking, improve operational performance of the digital PLL, and provide a mechanism to isolate the vulnerable nodes from the single event sensitive capacitive nodes of the low pass filter. Two transmission gates are used in the design to implement the charge pump. These gates are controlled by the dead zone circuitry and are switched all together. An analytical model has been developed to determine the electrical parameters of the proposed design. The natural frequency representing the response time of the loop is used to derive the lock and pull-in ranges and the lock and pull-in times of the digital PLL. The redundancy technique was used to increase the area and power requirements of the design. The technique uses multiple copies of the charge pump and low-pass filter to reduce the effects of an ion hit on a single node. A draft was developed that determined the maximum amount of phase jitter that was encountered in the charge pump and the voltage charge pump during a specified time window. The area, power design tradeoffs and resistive tolerances between the digital PLLs implementing the voltage charge pump over the charge pump were examined. A MOSIS process with IBM 130 nm is used to simulate the circuit with SE strikes which was represented by the double-exponential current pulse model for charges up to 500 fC.

The voltage charge pump can significantly reduce the voltage perturbation on the input of the voltage controlled oscillator and reduce the amount of phase displacement in the output of the digital PLL by approximately 2 orders of magnitude, reducing the number of incorrect pulses below those resulting from strikes in the voltage controlled oscillator. So with the design made a charge pump sensitivity towards the digital PLL was considerably reduced and its effects on the output were brought down to a proper level. The design results in a decreased area requirement with minimal impacts on phase jitter and power consumption. Furthermore, the design eliminates the charge pump as the most susceptible module and significantly hardens the digital PLL. In spite of the fact that the charge pump proposed results in improvement of single event transient susceptibility, some parameters like phase jitter, resistor design tolerance and area have scope for further advancement. [4]

Boulghassoul *et al.* have worked on the characteristics of Single Event Transient (SET). The circuit is designed to achieve speed applicable to mixed signal RF operations. The circuit is implemented using 0.18 μm and 0.13 μm technologies. The dynamics of SET pulse shaping for each module is different. Each digital PLL module designed has a separate level of sensitivity to irradiation. This module has capability to alleviate to various degrees by the feedback action of the closed loop. The radiations from the phase frequency detector and voltage controlled oscillator do not affect the digital PLL's normal operation. Charge pump becomes sensitive due to the circuit elements used for jitter effect and for the improvement of speed of PLL. The SET phenomenon is experimented in the design for high speed mixed signal circuits. The PLL is designed to operate upto the frequency of 1.3 GHz. The discrepancies in the operation of charge pump do not affect the working of PLL even at the higher frequencies. Its effects are lessen by adjusting the loop parameter. Instead of the normal operations of the circuit at higher frequencies, the design gets affected parasitic photocurrents.

The analysis showed that the sensitivity of a digital PLL system is strongly dependent on which of its modules is subjected to ionizing radiation. Computer simulations of single-event transients on the phase-frequency detector module and the voltage-controlled oscillator module indicated that their radiation responses have a negligible impact on the digital PLL normal operations. The sensitivity of the charge pump module was found to be the dominant contributor to the radiation vulnerability of the digital PLL system. The charge pump incorporated a design element favourable to achieving high-speed operations. But it also introduced a circuit configuration that can be easily disconcerted by the impact of a heavy-ion. [5]

Wagdy *et al.* have proposed a novel fast locking digital PLL based on successive approximation register. Three technologies are used in the design, namely, SPICE modelling, VHDL Analog and Mixed Signal extensions (AMS) and 0.18 μm CMOS process. The digital PLL design has two distinct stages of operation viz. a coarse tuning stage and a fine tuning stage. The fine tuning stage is similar to the conventional PLL having a phase frequency detector, a charge pump with low pass filter and a voltage controlled oscillator. A coarse tuning stage is used as a circuitry to boost the digital PLL. It consisted of a frequency comparator array, a successive approximation register and a digital to analogue converter. The architecture of this digital PLL has been designed and simulated in 250 nm SPICE. The switching

between coarse and fine tuning is handled by control logic. The working of the PLL goes like this. The input frequency and the frequency from the voltage controlled oscillator are compared in the phase frequency detector. The phase difference between the two is given as input to the charge pump. According to the input to the charge pump *i. e.* negative or positive, the charge pump is charged up or down. The low pass filter removes the high frequency components like the noise signal and the other disturbances. The output voltage from the charge pump is given as input to the voltage controlled oscillator which converts this voltage into the oscillations which is again compared with the input waveform and the process is repeated. According to the working of the fast locking digital PLL, the VCO frequency and the input frequencies are compared in the frequency comparator array, the output of which is given to the successive approximation register which is 4 bit bidirectional counter. The counting of the counter depends upon the input. The output from the successive approximation register is given to digital to analogue converter. This analogue output is the input to the charge pump. The charge pump output is given to the voltage controlled oscillator. The output frequency of oscillator is compared with the input frequency. Initially the two frequencies are compared in the coarse tuning stage. If the difference between the two frequencies is very small then the mechanism is shifted to the fine tuning stage. And the process is carried out in the fine tuning stage. This design is implemented in the three technologies.

The fast locking digital PLL was found to be 1.5 to 3 times faster than the conventional digital PLL. The flash word in the design was brought from the mechanism used in the flash analog to digital converter. The fast locking circuitry boosted the speed of the circuit and the range of the frequencies captured by the PLL was also increased. ([6]-[8])

III. CONCLUSIONS

Various technologies used for the implementation of PLL are discussed in the paper. The tuning range of the Injection Locked Frequency Divider is increased to half of the VCO tuning range, in order to increase the margin. The PLL formed using 0.35 μ m CMOS process showed phase frequency detector with higher operation frequency, lower phase jitter and smaller circuit complexity. In the PLL formed using nine gate phase detector there was no steady state frequency tracking error for period ramp input signals. Also the PLL was easy enough to integrate on a single chip. In spite of these good results, no phase locked state was found in the design even if the input frequency and phase remained constant due to which the steady state errors tend to accumulate. The low acquisition of the detector also came as the drawback of the design. The voltage charge pump designed in the experiment significantly reduced the voltage perturbation on the input of the voltage controlled oscillator and reduced the amount of phase displacement in the output of the digital PLL by approximately second orders of magnitude, reducing the number of erroneous pulses below those resulting from strikes in the voltage controlled oscillator. The Radiation Hardened By Design technology used indicated that their radiation responses have a negligible impact on the digital PLL normal operations. But it also introduced a circuit configuration that can be easily perturbed by the impact of a heavy ion. The fast locking digital PLL designed using SAR technique was found to be 1.5 to 3 times faster than the conventional digital PLL.

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