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Optimized Methodology for Realization of Logic Circuits using QCA Gates

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Abstract*— Quantum dot cellular automata (QCA) is one of the possible technologies to exert the reversible logic. While quantum computation and low power design represent the most prominent application scenes of reversible circuits, promising results have been achieved in other domains as well. In this paper, We was discussed one specific model of designing. This model proves that designing capabilities of sequential circuits are compatible with QCA gates under nanotechnology. We was made an important step toward a circuit implementation with sample function, by introducing a model of computation based on QCA technology. We propose a new paradigm for how computation could be performed with the truth tables to achieve several schemes with one output based on QCA technology. The advantage of computing with the truth table is that it ensures the computing process to generate same output. The proposed technique improves the performance at variety states configuration profoundly.

***Keywords*— Optimized methodology, QCA gates, full subtractor**

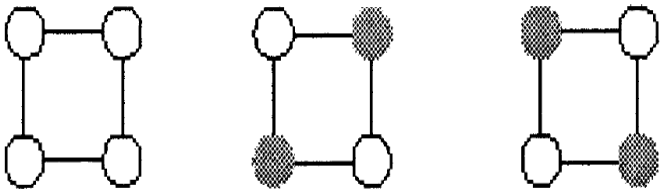
I. INTRODUCTION

Reversible logic is emerging as a promising computing paradigm with applications in low power quantum computing and QCA in the field of very large scale integration (VLSI) design[1]. For irreversible logic, each bit of information lost produces kTln2 Joules of heat energy, where k is Boltzmann's constant and T is absolute temperature at which the computation is performed. At room temperature T, the amount of heat dissipated for one bit is small i.e. 2.9×10^{-21}J. This heat dissipation reduces the performance and lifetime of the circuits. The solution is to use revolutionary technology which enables extremely low power consumption and heat waste in computing[2]. It is hard to design these circuits with complex QCA gates only by truth table. so comes scientic instinct and experiences. Basically there is one kind of strategy to demonstrate these structures. by measuring the actual system state and comparing it with the ideal value, it can call "concurrent evaluation" the truth table that we have achieved variety states of configurations, but with the same output. we demonstrate two proposed gates of different categories.

QCA structures are constructed as an array of quantum cells with in which every cell has an electrostatic interaction with its neighboring cells. QCA applies a new form of computation, where polarization rather than the traditional current, contains the digital information. In this trend, instead of interconnecting wires, the cells transfer the information throughout the circuit. The basic operators used in the QCA are the three input majority gate and inverter. Any QCA circuit can be built using only majority gates and inverters[3]. Quantum-dot Cellular Automata (QCA) is one of the most attractive technologies for computing at nano-scale[4]. In this paper, the synthesis experiment is conducted for a subtractor, and the result show that the proposed approach is feasible and effective.

II. QUANTUM DOT DELLULAR AUTOMATA

Quantum-dot cellular automata (QCA) is a scheme for molecular electronics in which information is transmitted and processed through electrostatic interactions between charges in an array of quantum dots. A schematic diagram of an idealized four-dot QCA cell is shown in Figure 1a. The cell consists of four quantum dots positioned at the corners of a square. The cell contains two extra mobile electrons, which can tunnel between neighboring sites of the cell[5]. There exist two equivalent energetically minimal arrangements of the two electrons in the QCA cell, as shown in Fig.1(b and c).



a) **b) P=+1** **c) P= -1**

Fig.1. Schematic four-dot QCA cell

Any QCA circuit can be efficiently built using only majority gates and inverters. As shown in Fig. 2 (a), an ordinary QCA gate implementing the majority function is as follows:

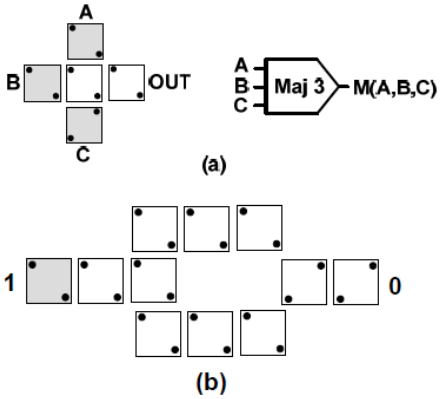


Fig2. (a) A QCA majority gate (b) A QCA inverter[6]

As illustrated in Fig. 2 (a and b), each QCA majority gate in normal form requires only five QCA cells. The QCA Majority Voter (MV) realizes MV(A, B, C) = Maj(A, B, C) = AB+BC+CA, as in Fig. 2, outputs '1' if there are two or more 1s in an input pattern[7]. The truth table of MV gate has been shown in Table 1.
Nand-Nor-Inverter (NNI) where NNI(A, B, C) = MV(A', B, C') = A'B+BC'+C'A'. It is shown in Fig. 3. The NNI gate is a universal gate and can be employed for realizing versatile Boolean logic functions[7]. The truth table of NNI gate has been shown in Table 2.

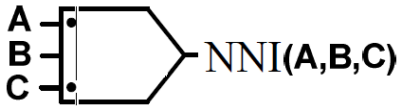


Fig. 3. QCA Nand-Nor-Inverter (NNI) Gate

Table1.Truth table of MV gate

A	B	C	MV(A,B,C)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Table2.Truth table of NNI gate

A	B	C	NNI(A,B,C)
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

III. OPTIMIZED METHODOLOGY USING QCA GATES

This method assumes that the three inputs are presented. In order to make improvements in the capability and effectiveness of QCA's synthesis, we adopt the evolutionary design technique, and then propose an automatic synthesis approach of QCA based on the specialized expansion recent method. However, this method can lead to the single output from inputs , but we cuold achieved some other various states configurations of logic circuits in quantum information and quantum computation. Hence, proposed assumption logic circuit should be the same output for all configurations which has been verified by the truth table. It is mentioned that the selected example is not necessarily the best architecture or only way to describe that.
The basic framework of methodology is described as follows:

Step 1: Firstly, the truth table of mentioned circuit with inputs and output should be shown.
Step 2: Consider the assumption function of MV and NOT gates or only MV gates.
Step 3: Investigating rows that need to have clear answers according to information and fill in them.
Step 4: According to the inputs, consider another assumption function.
Step 5: Guess that remain functional.
Step 6: Finally, we investigate the accuracy of the results by the truth table.

Firstly, we evaluated some characterization of MV and NNI gates. In the other words, any Boolean function is deduced either by combination of MV and NNI gates or by NNI gates alone. For example, we have following equations:
A'=NNI(A,0,0) (1)
A=MV(A,0,1)

MV(A,B',C')=NNI(B,A,C)

We can utilize to design NAND gate by using MV gates. Equation (2) demonstrates the NAND gate equation[9].

NAND =MV(A', B',1) =(AB)' (2)

For the NOR gate Equation (3) shows the gate formula[8].

NOR =MV (A', B',0) =(A+ B)' (3)

In the following, we are going to present one example to illustrate the application of recent methodology in full subtractor architecture.

We can implement a full subtractor using these majority gates. Fig.4 shows one design from full subtractor. Majority expression of full subtractor functions operator as Eq.4.

Borrow=MV(MV(A,B',C),B,A') (4)

Difference=MV(MV(A',B',C'),MV(A,B',C),B)

The currently available MV gates can be used to implement arbitrary logic functions. but, how did the Eq(4) obtain? For example, we have borrow in mentioned circuit. It can be easily seen form Fig.4 that the truth table is shown in the following implementation. The corresponding truth table of full subtractor using MV gates is shown in Table 3.

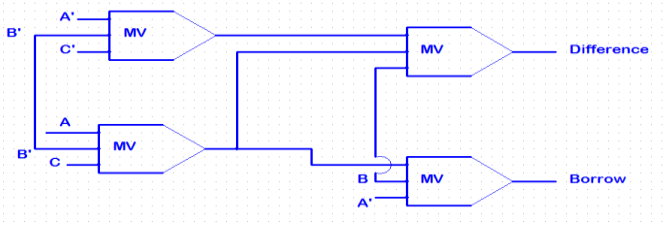


Fig.4. Full Subtractor Circuit Diagram with 4 MV gates

Table3.Truth table of full subtractor using MV gates

A	B	C	F_1	F_2	F_3	F=Borrow
0	0	0	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	1	1	1
0	1	1	0	1	1	1
1	0	0	1	0	0	0
1	0	1	1	0	0	0
1	1	0	0	1	0	0
1	1	1	1	1	0	1

From the truth table, it can be concluded that the input pattern corresponding to a particular output pattern with MV gates can be uniquely determined. For example when designing full subtractor, we use three rail inputs and by Assuming F_1=MV(A,B',C). In this method the first selection function is very noticeable to achieve the desired result. The first unknown column is obtained(that is red).Therefore, The initial value for design has been considered. Now, we compare $F_1$and F for computing remaining columns. Hence, the relationship between the F_1,F_2,F_3 and F described here. Clearly, the method determine the unresolved state of the truth table based on its configuration in the previous generation. Therefore,we fill in safe places(that is green). With a little care we found that one of columns could be B. Therefore, F_2=B(That is brown). Finally, we complete the remaining blanks(That is blue). Ultimately, we will specify the last column by the following equation: F_3=A' . According to the results as we can be seen in Table1, several benchmark functions could be implemented using the above approach. Optimized methodology is a kind of concurrent evaluation for achieve the best design that is illustrated as an example circuit.

IV. CONCLUSION

Quantum dot cellular automaton (QCA) is an emerging technology in the scope of nanotechnology. In this paper, we have focused on the optimized synthesis based on MV gates and we have proposed a step by step synthesis approach of QCA gates based on truth table.This paper describes full subtractor using majority voter gates. In this method, each step is dependent on the previous step and the next step will produce from the previous pitch. However, the first selection function is very noticeable to achieve the desired result. we have adopted truth table to eliminate optimization problems. By using these concurrent evaluation, the function of implemented subtractor can be observed the results quickly. In other words, it is especially suitable for reversible computing as the primary goal in QCA design.

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