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Design of Digital Modulators: BASK, BPSK and BFSK using VHDL

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Abstract- ***Digital modulation is less complex, more secure and more efficient in long distance transmission. The noise detection and correction in digital is more efficient than analog counterpart. So it has more importance in modern communication. Digital modulation represents the transfer of the digital bit stream from the transmitter to the receiver via the analog channels. During the modulation process the information signal modifies one or more carrier parameters, leading to shift keying techniques. A very widespread solution is the Software Defined Radio (SDR), whose modulation/demodulation methodology consists in programming either software in a dedicated processor (DSP), or logic in a programmable logic device (FPGA). These digital modulation techniques can be realized using FPGA (Field-programmable gate-array). In literature survey found that design employs the minimum number of blocks necessary for achieving BASK, BPSK and BFSK modulation. The modulating and carrier signals can be user controlled and the modulators are developed and compiled to a Verilog Hardware Description Language (VHDL) netlist. The functionality of these digital modulators will be demonstrated through simulations using the Quartus II software and experimental measurements of the real-time modulated signal via an oscilloscope.***

Keywords – BASK, BFSK, BPSK, digital modulator, FPGA, Verilog

I. INTRODUCTION

The choice of digital modulation scheme will significantly affect the characteristics, performance and resulting physical realization of a communication system. There is no universal 'best' choice of scheme, but depending on the physical characteristics of the channel. Consideration must be given to the required data rate, acceptable level of latency, available bandwidth, anticipated link budget and target hardware cost, size and current consumption. The objective of a digital communication system is to transport digital data between two or more nodes. In radio communications this is usually achieved by adjusting a physical characteristic of a sinusoidal carrier, either the frequency, phase, amplitude or a combination thereof. This is performed in real systems with a modulator at the transmitting end to impose the physical change to the carrier and a demodulator at the receiving end to detect the resultant modulation on reception.

Field-programmable gate arrays (FPGAs) are semiconductor devices containing programmable logic elements (LEs) and a hierarchy of reconfigurable interconnects to realize any complex combinational or sequential logic functions. Today's FPGAs consist of configurable embedded static random-access memories (SRAMs), high-speed transceivers, high-speed input/output (I/O) elements, network interfaces, and even hard-embedded processors [1]. A literature survey shows that FPGAs are widely used in different applications, such as motor controllers [2], neural network implementations [3-5], finite-impulse-response (FIR) filter realization [6,7], fuzzy-logic controllers [8], etc.

In this paper, implementation of digital modulation and demodulation using FPGAs has received considerable attention due to their high flexibility, low cost, and high speed.

II. DESIGN OF DIGITAL MODULATORS

A. BASK Modulator –

In a BASK (binary amplitude-shift keying) modulation process, the amplitude of the sinusoidal carrier signal is changed according to the message level ("0" or "1"), while keeping the frequency and phase constant. If transmitting data is 1, BASK modulated signal is carrier signal. But when transmitting data is 0, BASK modulated signal is 0. In modulation, data bits are multiplied with a carrier signal and then modulated signal is created.

$$S(t) = A_c \sin(2\pi f c t) \quad ; \text{if symbol} = 1$$
$$S(t) = 0 \quad ; \text{if symbol} = 0 \qquad (1)$$

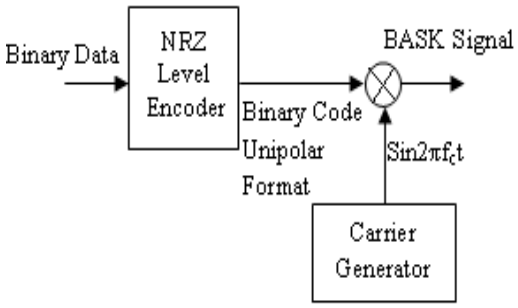

Fig. 1 A block diagram of BASK modulation

In Fig.1, it is shown a block diagram of BASK modulator. Output of multiplier is modulated by binary code. This NRZ level encoder converts the input binary sequence to the signal suitable for product modulator [8]. In Fig. 2, it is shown that BASK modulation [9].

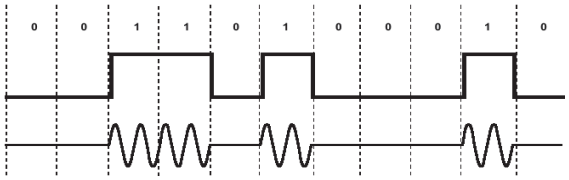

Fig. 2 The modulating-signal (message) and the BASK signal waveforms

B. BPSK Modulator –

In a BPSK (binary phase-shift keying) modulation process, the phase of the sinusoidal carrier signal is changed according to the message level ("0" or "1") while keeping the amplitude and frequency constant. Beginning of BPSK modulated signal's period is positive values, if transmitting symbol is 1. But if transmitting signal is 0, beginning of BPSK modulated signal's period is negative values. A block diagram of the BPSK modulation and its signal waveforms are shown in Figures 3 and 4, respectively.

$S(t) = A_c \sin(2\pi fct)$; if symbol = 1
$S(t) = -A_c \sin(2\pi fct)$; if symbol = 0 (2)

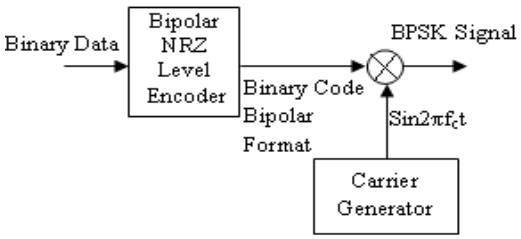

Fig. 3 A block diagram of BPSK modulation

In figure 3, it is shown the block diagram of BPSK modulator. Binary data is converted to binary code bipolar format, then binary code bipolar format signal is multiplied carrier signal. Thereby, BPSK modulated signal is created.

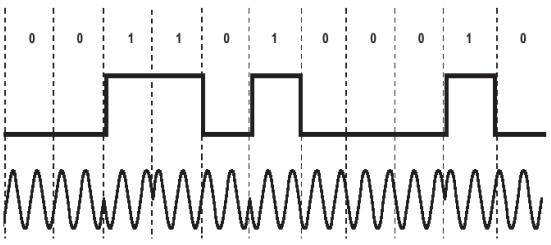

Fig. 4 The modulating-signal (message) and BPSK signal waveforms

C. BFSK Modulator –

In a BFSK (binary frequency-shift keying) modulation process, the frequency of the sinusoidal carrier signal is changed according to the message level ("0" or "1") while keeping the amplitude and phase constant. A block diagram of the BFSK modulation and its signal waveforms are shown in Figures 5 and 6, respectively.

$S(t) = A_c \sin(2\pi f1ct)$; if symbol = 1
$S(t) = A_c \sin(2\pi f2ct)$; if symbol = 0 (3)

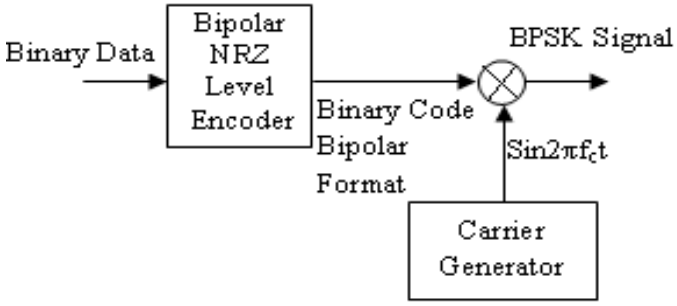

Fig. 5 A block diagram of BPSK modulation

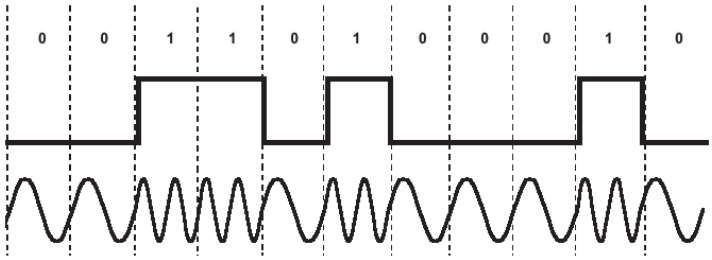

Fig. 6 The modulating-signal (message) and BFSK signal waveforms

III. FPGA BASED DESIGN OF DIGITAL MODULATORS

A. FPGA Based Design of BASK Modulation-

BASK based on FPGA application will be implemented on Quartos II compiler. Also, both modulation and demodulation can be implemented on FPGA. So, modem based on FPGA is created [10]. The principle of the BASK system implemented on the FPGA is illustrate in fig.7.

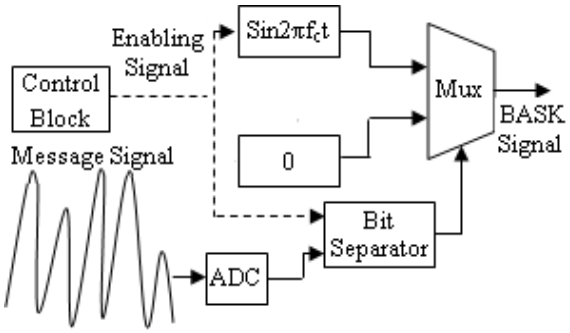

Fig. 7 BASK system implemented on FPGA

B. FPGA Based Design of BPSK Modulation-

Using Quartos II complier, BPSK modulated signal can be created. Proposed block diagram in FPGA is shown in Fig.8. Using ADC, message signal is converted digital signal. Thereby, in FPGA, this signal can be processed and FPGA based BPSK modem can be created. Used bit separator separates one by one in 14 bits output of ADC. Bit Separator will be created using Very high speed integrated circuit Hardware Description Language.

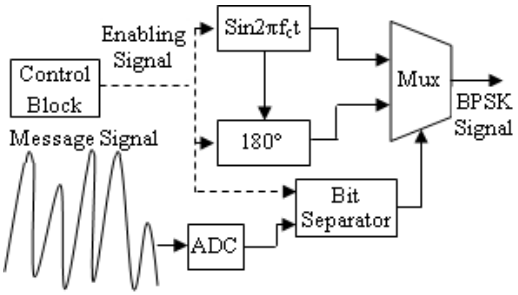

Fig. 8 BPSK system implemented on FPGA

IV. **DESIGN OF DEMODULATORS**

BASK, BPSK and BFSK Demodulator-

BASK, BPSK and BFSK demodulators can be achieved from the Fig.9. The most important point for receiver, received signal is obtained quite correctly. As realizing in modulator input signal is firstly multiplied with a carrier of signal in demodulator. Next, multiplied signal is passed through integrator, then integrated signal is passed through a decision making device.

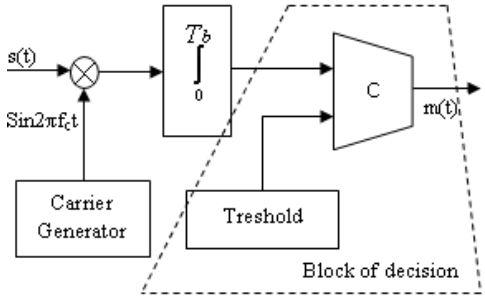

Fig. 9 Block diagram of BASK, BPSK and BFSK demodulator

V. BIT ERROR RATE (BER)

In an AWGN channel, the BER (Bit Error Rate) decreases approximately exponentially as the SNR (Signal to Noise Ratio) increases [11]. Straight BPSK produces good BER value at the receiver. Although the symbol error rate for BPSK is low that of BASK, BPSK transmits symbols at same the rate of BASK Bit error rate of BPSK.

V. CONCLUSION

FPGA implementations of BASK, BFSK, and BPSK digital modulators could be demonstrated. The main advantage of the implementations is the minimum numbers of digital blocks used for performing digital modulations, the ability to integrate with modules in FPGA boards, and the user controllability of the input signal's frequencies. In addition, we can show hardware implementation of BASK, BPSK and BFSK modulation techniques based on FPGA. Also, comparison to different performance parameters of modulation techniques will be analyzed. It is shown that modulation techniques (BASK, BPSK and BFSK) have disadvantage and advantage in simulation and plotting results.

The implemented FPGA designs are suitable for realization of the digital baseband-modulation part of software-defined radio systems. In addition, usage of this kind of implementation for educational purposes in digital communications laboratories or courses clearly emphasizes the correlation between different courses in electronics engineering.

REFERENCES

[1] http://www.altera.com/products/fpga.html.

[2] B. Alecsa, and A. Onea, "Design, Validation and FPGA Implementation of a Brushless DC Motor Speed Controller," Proceedings of the 17th IEEE International Conference on Electronics, Circuits, and Systems (ICECS), December 12-15, 2010, pp. 1112-1115.

[3] S. Himavathi, D. Anitha, and A. Muthuramalingam, "Feedforward Neural Network Implementation in FPGA Using Layer Multiplexing for Effective Resource Utilization," IEEE Transactions on Neural Networks, 18, 3, 2007, pp. 880-888.

[4] N. M. Botros and M. Abdul-Aziz, "Hardware Implementation of an Artifi cial Neural Network Using Field Programmable Gate Arrays (FPGA's)," IEEE Transactions on Industrial Electronics, 41, 6, 1994, pp. 665-667.

[5] T. Orlowska-Kowalska and M. Kaminski, "FPGA Implementation of the Multilayer Neural Network for the Speed Estimation of the Two-Mass Drive System," IEEE Transactions on Industrial Informatics, 7, 3, 2011, pp. 436-445.

[6] P. K. Meher, S. Chandrasekaran, and A. Amira, "FPGA Realization of FIR Filters by Effi cient and Flexible Systolization Using Distributed Arithmetic," IEEE Transactions on Signal Processing, 56, 7, 2008, pp. 3009-3017.

[7] K. N. Macpherson and R. W. Stewart, "Rapid Prototyping – Area Effi cient FIR Filters for High Speed FPGA Implementation," IEE Proceedings ─ Vision, Image and Signal Processing, 153, 6, 2006, pp. 711-720.

[8] D. Kim, "An Implementation of Fuzzy Logic Controller on the Reconfi gurable FPGA System," IEEE Tran sactions on Industrial Electronics, 47, 3, 2000, pp. 703-715.

[9] C.Erdogan, I. Myderrizi, and S. Minaei, "FPGA Implementation of BASK-BFSK-BPSK Digital Modulators", IEEE Antennas and Propagation Magazine, Vol. 54, No. 2, April 2012

[10] Mehmet Sonzem, Ayhan Akbal, "FPGA-Based BASK and BPSK Modulators Using VHDL: Design, Applications and Performance Comparison for Different Modulator Algorithms", International Journal of Computer Applications (0975 – 8887), Volume 42- No. 13, March 2012.

[11] Molisch, A., F., "Wireless Communication", john Wiley & Sons, UK 2011.

