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Design and Implementation of Low Power Pipelined Coefficient Ordered Fft Processors Using Body Bias Technique

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Abstract - In this paper we present a modified coefficient ordering based pipelined 16 point FFT processor. The fixed radix- 4 and single path pipelined architecture is used in this FFT design. The pipelined architecture provides higher throughput rate comparing with the ordinary pipelined architecture. The low power issue is addressed by minimizing the switching activity using minimum Hamming distance transition. The switching activity of twiddle computation is thus reduced from 192 to 78, i.e. 59% reduction. The multiplier less architecture uses reduced number of multipliers to realize complex multiplication. The processor is implemented in VHDL and synthesized using 0.18um Cadence RTL complier. The power evaluation was then carried out on the circuit netlist using a clock frequency of 100MHz.

Keywords – FFT, OFDM, Switching activity, VHDL, Commutator, Compressor

I. Introduction

The FFT processor is the critical block in orthogonal frequency division multiplexing (OFDM) technology. Due to the nature of non stopping processing on the same clock frequency of sampling data, pipelined FFT is preferred especially for a high throughput or low power solution. In the pipelined architecture, the commutator and the complex multiplier at each stage contribute a dominating part of the whole power consumption[2][3]. This paper proposes an optimal design to minimize one of the power consuming factor , the switching activity. The switching activity between successive coefficients fed to the complex multiplier can be drastically reduced by coefficient ordering. The coefficient ordering requires corresponding data sequence as per new coefficient ordering. In this way we can meet the less hardware complexity and the maximum efficiency.

In this paper, FFT algorithm is described in Sec II. The architecture of coefficient ordering pipelined FFT is discussed in Sec III. The proposed minimum switching activity design and multiplierless approach has been discussed in Sec IV. The processor have been implemented with 32 bit complex data and is presented in Sec V.

II. Algorithm

The N point DFT can be expressed as

$$X(K) = \sum_{N=0}^{N-1} x(n) \exp(-j2\Pi nk/N), \quad k=0,1\ldots N-1 \qquad (1)$$

the $\exp(-j2\Pi nk/N)$ is usually represented with W_N^{nk}, where $W=\exp(-j2\Pi/N)$. Let N be a composite number of v integers such that $N= r_1 r_2 \ldots\ldots\ldots r_v$, and define

$$N_t = N / r_1 r_2 \ldots\ldots\ldots r_t, \text{ and } 1 \le t \le v-1 \qquad (2)$$

where t is the stage number of the decomposed DFT and r_t is the radix. Using the recursive property and the relationship $W_{Ni\,Nj}^{Nj\,k} = W_{Ni}^{k}$ for radix r_1 Eqn(1) becomes

$$X(K)= \sum_{q_1=0}^{N_1-1} W_N^{q_1 k} \sum_{p=0}^{r_1-1} x(N1p+q_1)\ W_{r1}^{pk} \qquad (3)$$

This equation defines the computation for the first stage. The final stage is defined as follows.

$X(r1r2\ldots rv-1mv + \ldots\ldots + r1m2 + m1) =$

$$\sum_{qv-1=0}^{rv-1} Wrv\ xv-1\ (qv-1, mv-1) \qquad (4)$$

whereas intermediate stages are given by the following recursive equation.

$$xt(qt,mt) = WNt-1 \sum_{p=0}^{qtmt} Wrt\ xt-1 \quad (Ntp+qt\ mt-1) \qquad (5)$$

Where $2 \le t \le v-1$, $0 \le mt \le ri-1$, $0 \le qi \le N-1$ and $2 \le i \le v$.

For $r_1 = 4$, the flowgraph of a 16 point FFT based on the above formulation is shown in Fig.1. the corresponding equation is as follows.

$$X(4m2 + m1) = \sum_{q1=0}^{3} W4\ x1(q1,m1) \qquad (6)$$

where,

$$X1(q1,m1) = W\ 16^{q_1m_1} \sum_{p=0}^{3} W4^{pm1}\ x(4p + q1) \qquad (7)$$

In the Figure 1 each open circle represents a summation while the dots define the stage boundaries. The integer outside the open circle is the power of FFT twiddle factor W_N used. The integer inside each open circle is the value of *m1* (for stage 1) or *m2* (for stage 2). The number outside the open circle is the FFT coefficient applied.

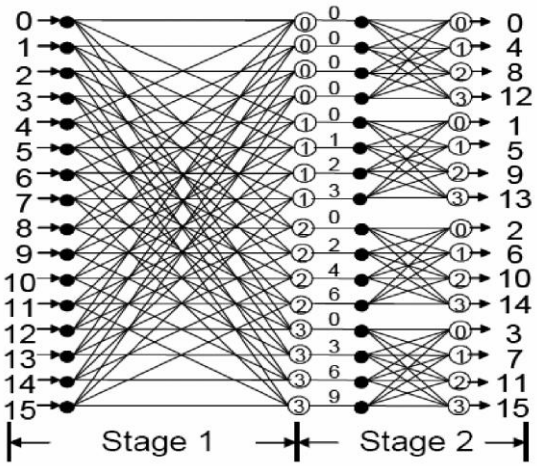


Fig 1. The signal flow graph of radix-4 16-point FFT [1]

III. Ordered pipelined FFT Architecture

A pipelined N point radix- 4 FFT Processor based on the previously described algorithm as shown in Fig.1 wil have $\log_4$ N stages. Each stage produces one output within each word cycle. Each stage contains a commutator, a butterfly and a complex multiplier. The sequential output of each stage must be ordered in accordance with the value of m_t. For a instance, from Fig 1 at stage 1, the output associated with m_1=0 are produced in first four word cycles, then those associated with m_1=1 in the next four cycles and so on. As seen in equation (2), the input data for each summation at stage t are separated in time by Nt words. The commutator comprises of six shift register along with three multiplexer.

IV. Implementation

The coefficients are reordered in order to minimize switching activity between successive coefficients by minimizing the hamming distance for each coefficient transition. The hamming distance is defined as the number of 1's of the XOR operation between two binary coefficients. Both the original and ordered coefficient sequence are encoded with 15 bit fixed points. To get the minimum switching activity, transition matrix of the hamming distance between each coefficient is developed.

Table 1
The transition matrix of switching activity
between each two coefficient with 16 word length

	W0	W1	W2	W3	W4	W6	W9
W0	0	15	17	19	3	21	13
W1	15	0	14	16	12	20	24
W2	17	14	0	14	14	16	14
W3	19	16	14	0	16	12	18
W4	3	12	14	16	0	20	16
W6	21	20	16	12	20	0	16
W9	13	24	14	18	16	16	0

The switching activity decreases from 192 to just 78, a reduction of 61% by following this approach.

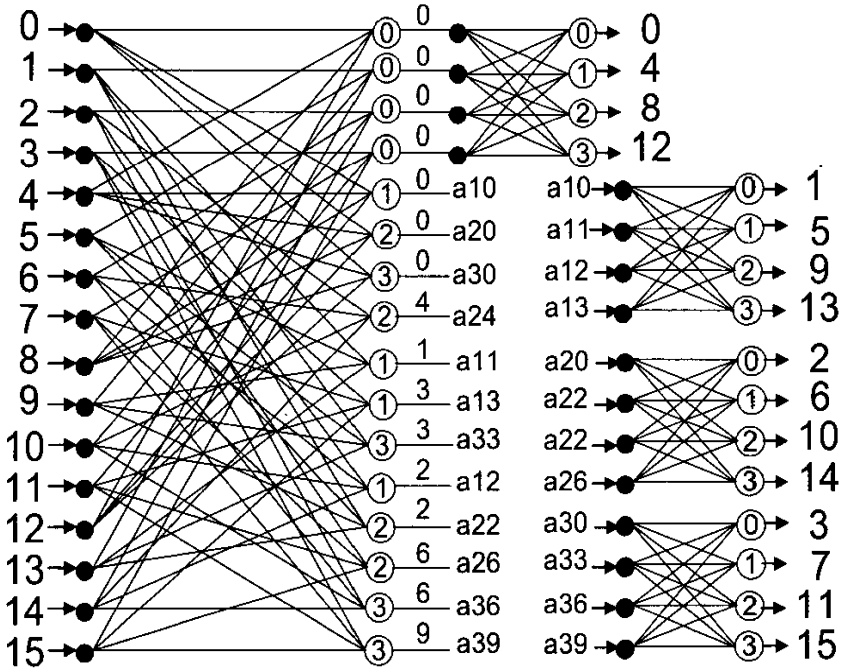


Fig.3 signal flow graph of a radix- 4 ordered 16 point FFT

The change in coefficient ordering requires corresponding data ordering accordingly. The data ordering is performed by s novel design of the commutator for stage 1 of a 16 point radix 4 FFT processor. The ordered data sequence has to be converted back into normal data sequence for its stage 2.

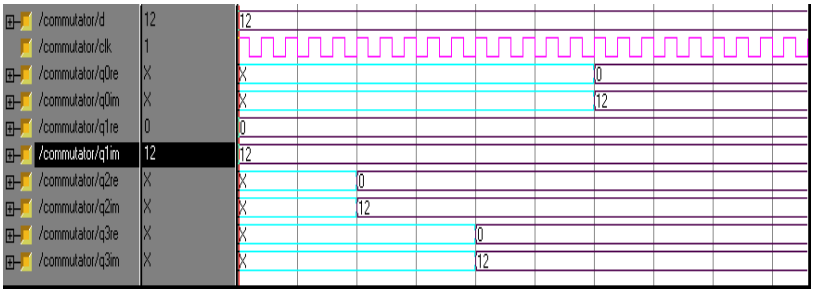
Table II.
Reduced switching activity

Normal coefficient sequence	16 bit quantized coefficient sequence	Ordered coefficient sequence	Ordered quantized coefficient sequence
W0	4000,0000	W0	4000,0000
W0	4000,0000	W0	4000,0000
W0	4000,0000	W0	4000,0000
W0	4000,0000	W0	4000,0000
W1	3b20,e7a2	W0	4000,0000
W2	2d41,d2be	W0	4000,0000
W3	187d,c4df	W0	4000,0000
W0	4000,0000	W4	0000,c000
W2	2d41,d2be	W2	2d41,d2be
W4	0000,c000	W2	2d41,d2be
W6	d2bf,d2bf	W3	187d,c4df
W0	4000,0000	W3	187d,c4df
W3	187d,c4df	W6	d2bf,d2bf
W6	d2bf,d2bf	W6	d2bf,d2bf
W9	C4e0,187e	W9	C4e0,187e
Normal Switching activity = 192		Ordered Switching activity = 78	

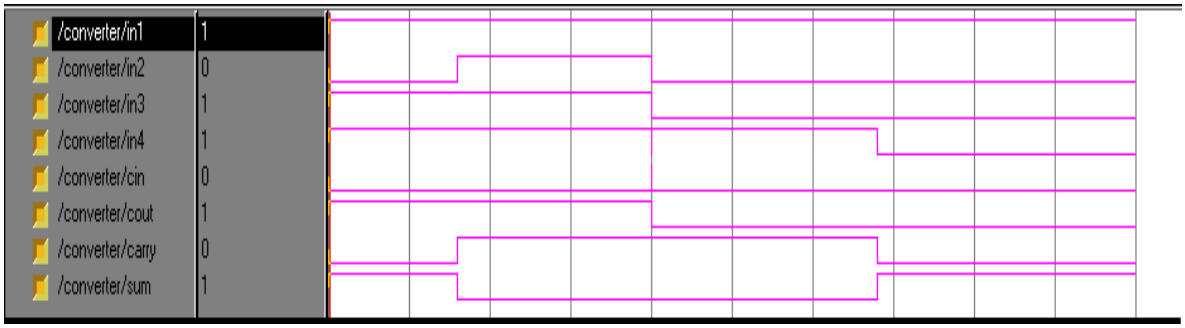
V. Results

The conventional and ordered pipelined FFT processor architectures have been implemented in register transfer level hardware descriptive language and synthesized using 0.18um Cadence RTL compiler. Power evaluation was then carried out on the circuit netlist using a clock frequency of 100 MHz. The switching activity decreases from 192 to 78, a reduction of 61% as per table II. The comparative results in terms of power for 16 point FFT, FIFO implementation styles and three common low power multiplier types are given in Table III. The FIFO was implemented two different ways namely SR and DM. The design of a 16-point FFT processor has been carried out for three different multiplier namely carry save array type, Wallace tree type and Non Booth coded Wallace tree type (nbw). It is clear from table III that our ordered architecture gives power savings for two multiplier types. The percentage power saving of our ordered approach is less for Wallace multiplier type.

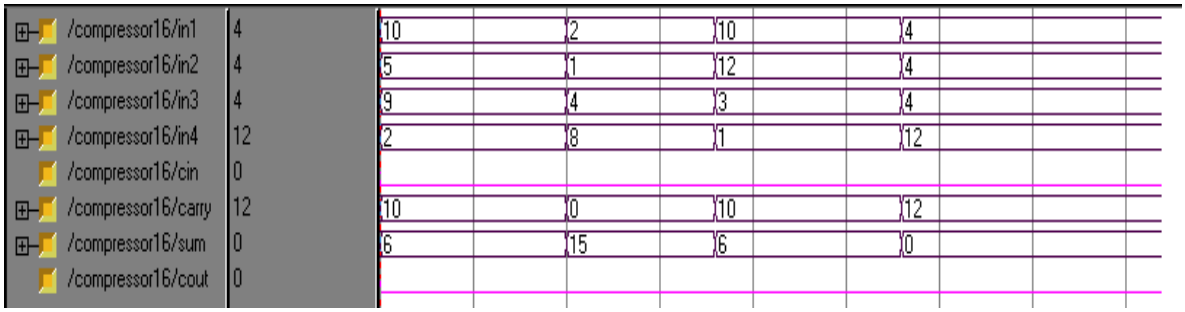
COMMUTATOR:



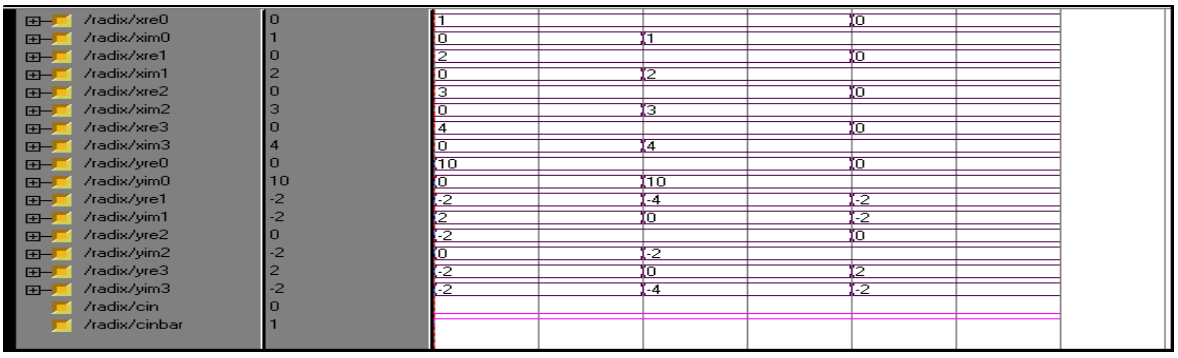
CONVERTER



COMPRESSOR



RADIX



COMPLEX MULTIPLIER:

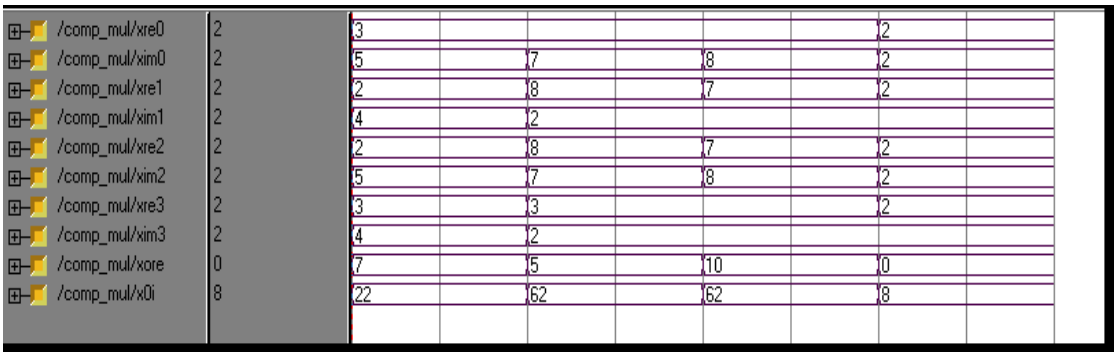


Table III
Comparitive power analysis

FFT size	Multiplier Type	SR based (mW)	DM based (mW)	Ordered (mW)	% saving (SR)	% saving (DM)
16 point	CSA	70.97	124.47	65.49	8	47
	Nbw	68.45	114.47	58.24	14	49
	Wallace	73.13	121.39	70.92	3	41

VI. Conclusion

In this paper, we modify the coefficient ordering technique and apply to 16-point FFT processor. The switching activity decreases from 181 to 78 in a whole 16 point cycle, a reduction of 61%. We have shown that the switching activity is minimized through the transition matrix. The corresponding power saving varies from 14% to 49% for a 16-point FFT for SR and DM respectively using commonly used low power multipliers.

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