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FPGA Implementation of Adaptive Equalizer for Software Defined Radio

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Abstract— When a signal is transmitted through a channel, the bit error rate increases due to channel imperfections. As channel characteristics vary with time, so to compensate these variations, only adaptive equalizers can be of worth. This paper presents the design and simulation of an adaptive equalizer using least mean square algorithm and implement the proposed equalizer on FPGA using EDA tools for resource calculation.

Keywords— Adaptation, Equalizer, Field Programmable Gate Array, Least Mean square algorithm

I. INTRODUCTION

A communication system is used to send information from transmitter to receiver.

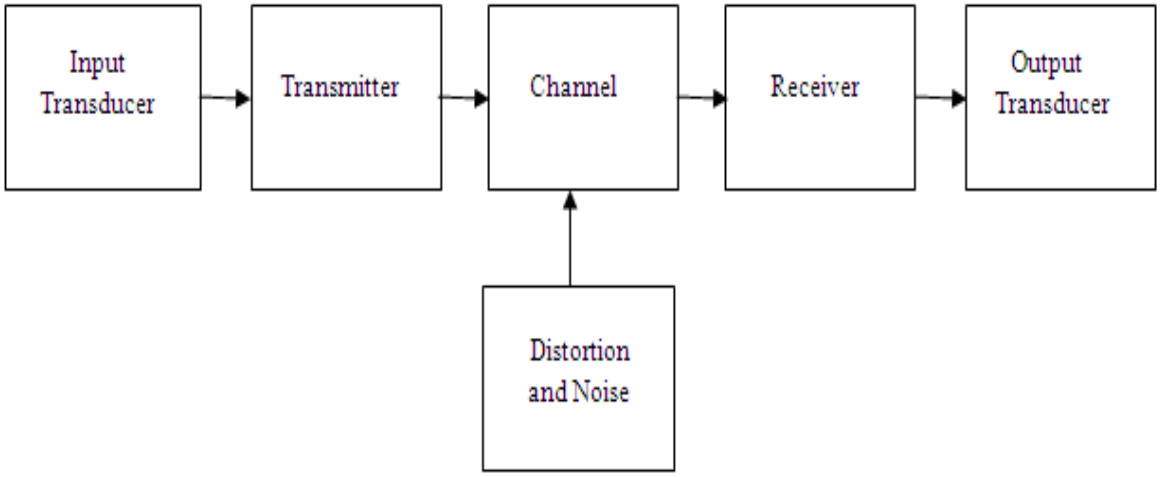

Fig.1 The Basic Communication Model

Generally the transmitter consists of amplifier, modulator, oscillator, filter circuits to perform necessary signal processing operation. The receiver consists of demodulator circuit, rectifier and filter circuits. Thus useful information extracted by receiver is conveyed to the end user. Channel is the medium that carries the signal from the transmitter and receiver. Channel have different characteristics like channel bandwidth, phase distortion, signal attenuation etc. The receiver should be able to recover the original symbols without error, the distortions or inter-symbol interference (ISI) caused by the channel, noise and other sources are tried to be minimized. This can be done by using equalizer. Earlier, the design of equalizer depends on the assumption of the channel transfer function is known. But, for most of the communications applications, the channel transfer function is not static. The channel transfer functions vary with time. In order to solve this problem equalizers are designed with adaptive characteristics. Section II describe the concept of equalization. Section III describe FPGA implementation of adaptive filter and the resources of FPGA required to implement the equalizer with adaptive filter. Section IV concludes the article.

II. CONCEPT OF EQUALIZATION

Equalizer gives the inverse of channel to the Received signal and combination of channel and equalizer gives a flat frequency response and linear phase as shown in Fig.2. Equalizer is meant to work in such a way that BER (Bit Error Rate) should be low and SNR (Signal-to-Noise Ratio) should be high [1].To compensate for the signal distortion, the adaptive filter for channel equalization is commonly used [2]. The structure of the adaptive filter is [3] shown in Fig.3. Least mean squares (LMS) algorithms are a class of adaptive filter used to mimic a desired filter by finding the filter coefficients that relate to producing the least mean squares of the error signal (difference between the desired and the actual signal). It is a stochastic gradient descent method in that the filter is only adapted based on the error at the current time [4]. The Fractionally Spaced Adaptive Equalizer shows fast convergence and better ISI mitigation over the other equalizers.

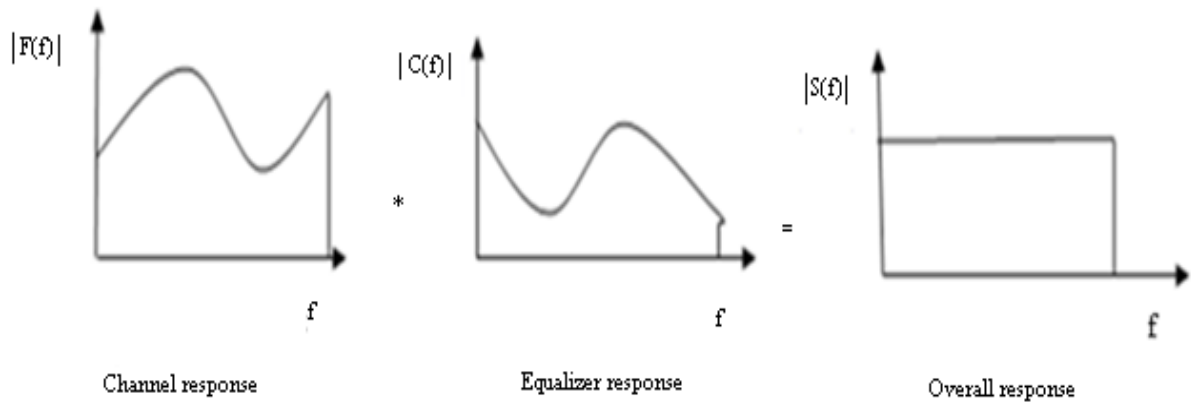

Fig.2 Concept of Equalizer

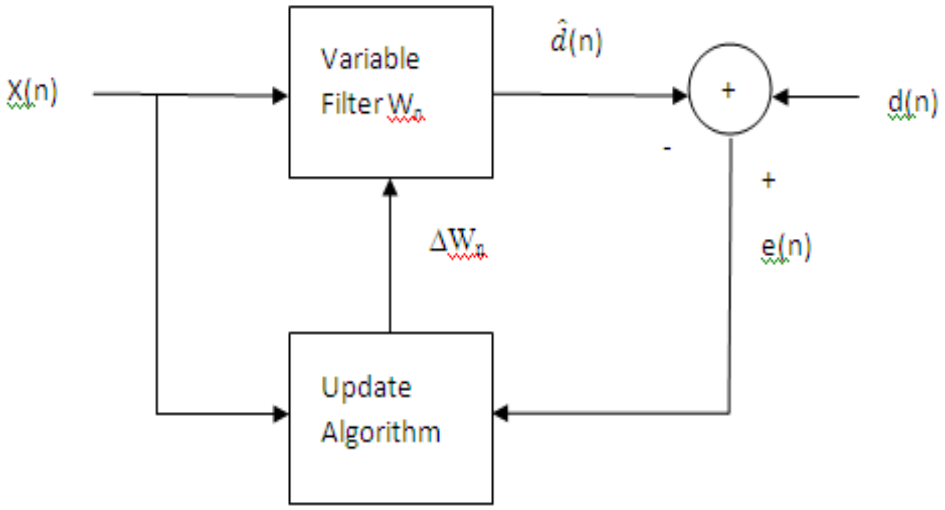

Fig.3 Adaptive Filter

The input signal is the sum of a desired signal *d* (*n*) and interfering noise v (n)

$$x(n) = d(n) + v(n) \quad \text{.... (1)}$$

The variable filter has a Finite Impulse Response (FIR) structure. The coefficients for a FIR filter of order *p* are defined as

$$w_n = [w_n(0), \quad w_n(1), \quad ..., \quad w_n(p)]^T \quad \text{....(2)}$$

cost function is the difference between the desired and the estimated signal

$$e(n) = d(n) - \hat{d}(n) \quad \text{.... (3)}$$

The variable filter estimates the desired signal by convolving the input signal with the impulse response. This can be expressed as

$$\hat{d}(n) = w_n * x(n) \quad \text{.... (4)}$$

Where

$$x(n) = [x(n), \quad x(n-1), \quad ..., \quad x(n-p)]^T \quad \text{.... (5)}$$

is an input signal vector. The variable filter updates the filter coefficients at every sampling instant

$$w_{n+1} = w_n + \Delta w_n \quad \text{.... (6)}$$

Where Δw_n is a correction factor for the filter coefficients.

The Fractionally Spaced Adaptive Equalizer shows fast convergence and better ISI mitigation over the other equalizers. Hence, its frequency response should inverse to that of the channel. This can be easily verified from the Fig.4. Fig.5 shows a MSE Cost Function for Conventional Equalizer and proposed Fractionally Spaced Equalizer. Fig.6 shows MSE Convergence for Conventional Equalizer and proposed Fractionally Spaced Adaptive Equalizer. Fig.7 represents the bit error rate (BER) analysis for the Ideal QAM, Conventional Equalizer and Fractionally Spaced Adaptive Equalizer.

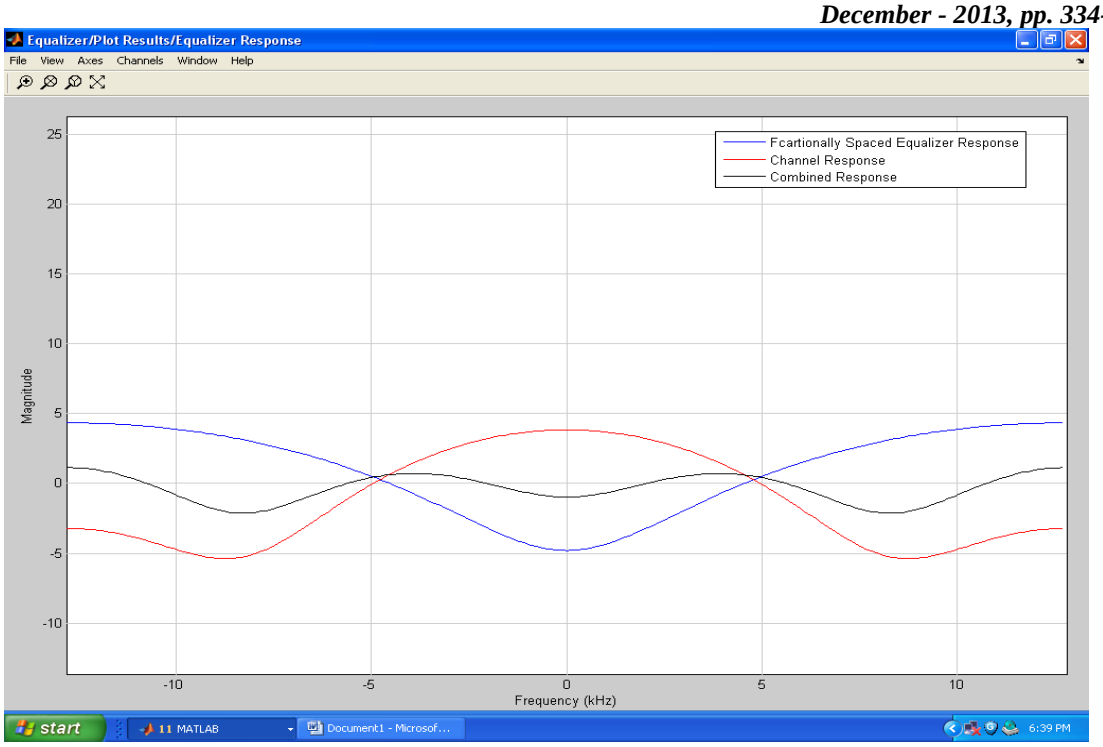

Fig.4 Magnitude Spectrum of FSE, Channel and Combined System

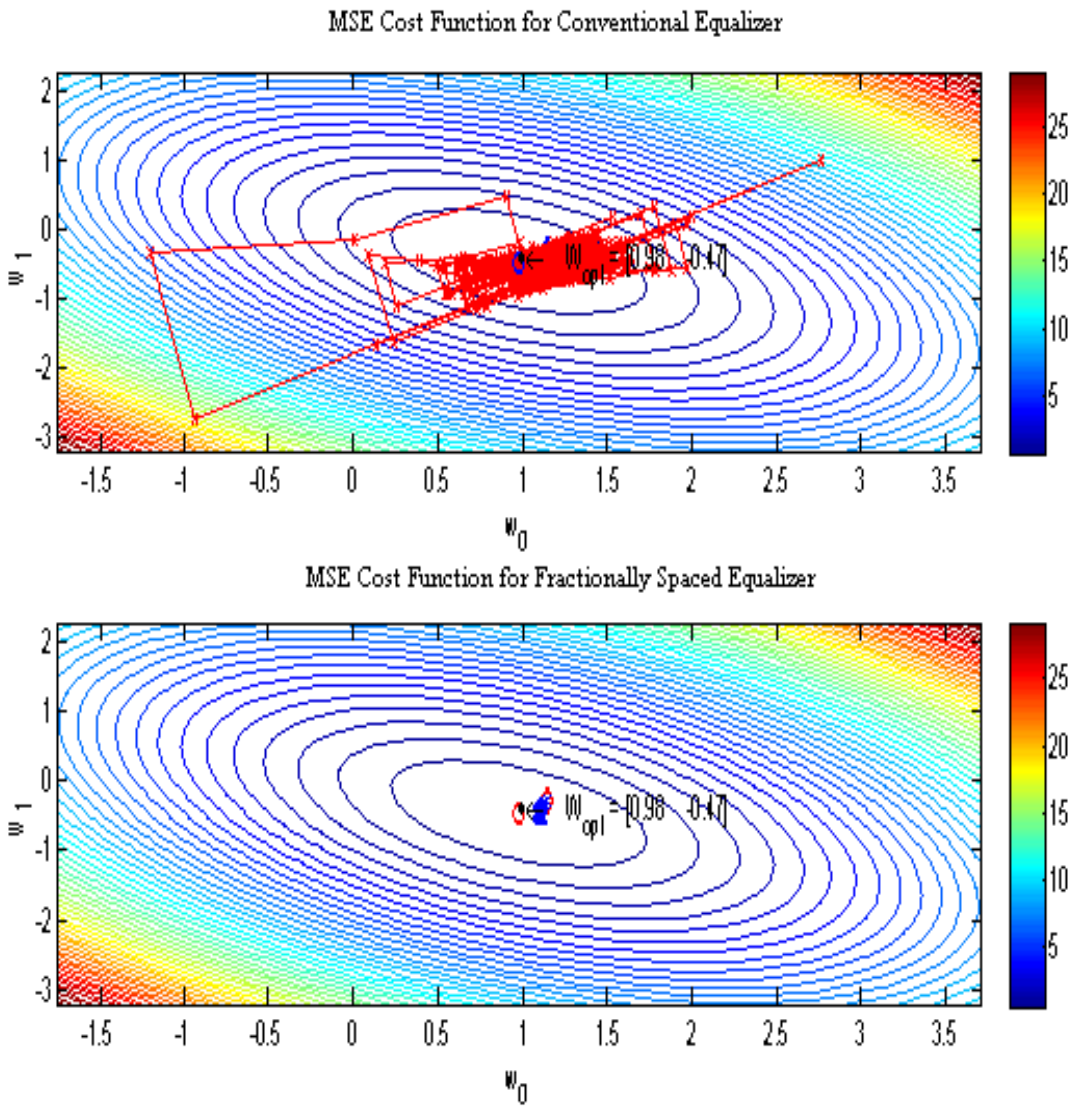

Fig.5 MSE Cost Function for Conventional Equalizer and FSE

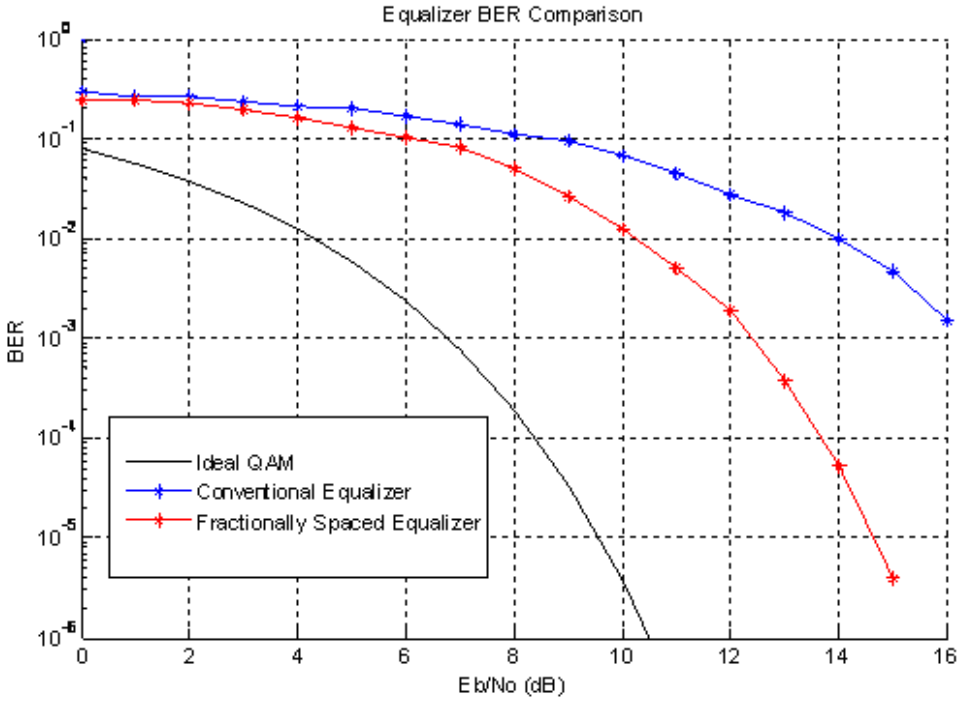

Fig.6 Equalizer Bit Error Comparision

The paper also presents FPGA implementation of Fractionally Spaced Equalizer.

III. FPGA IMPLEMENTATION OF THE EQUALIZER

In the present work, a Virtex-II Field Programmable Gate Array (FPGA) is used for implementations Equalizer. Using an Xilinx 9.2i tool for synthesis, VHDL code of the circuit has been implementation on an FPGA. Various parameters of Fractionally Spaced Adaptive Equalizer will be optimized by implementing the optimization algorithm in MATLAB. System Generator will be used to generate the hardware description code of the proposed fractional spaced equalizer due to its ability to provide rapid development cycle. The hardware description code will be used to implement the proposed fractionally spaced equalizer on an FPGA using Xilinx Integrated System Environment (ISE) tool for resource calculation. Fig.4 shows an internal structure of RTL Schematic diagram.

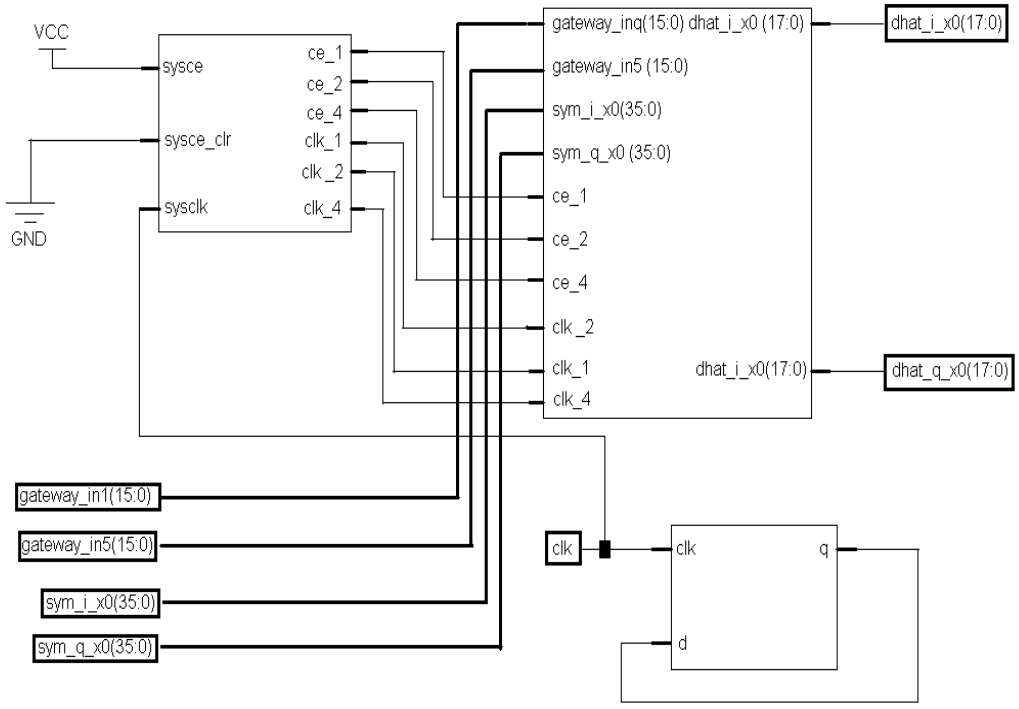

Fig.7 Internal Structure of RTL Schematic diagram

After testing model on simulation, the simulation design is compiled to ISE file before generating the programming file, bit file Table 1 show the resources used in this model which just takes a small part in Xilinx Virtex-II FPGA.

TABLE 1
DEVICE UTILIZATION SUMMARY OF XILINX FPGA

Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	2,232	67,584	3%
Number of 4 input LUTs	1,070	67,584	1%
Logic Distribution			
Number of occupied Slices	1,746	33,792	5%
Total Number of 4 input LUTs	1,981	67,584	2%
Number used as logic	1070		
Number used as route-through	273		
Number used as Shift register	638		
Number of bonded IOBs	133	684	19%
IOB Flip Flops	32		
Number of MULT18X18s	24	144	16%
Number of GCLKs	1	16	6%
Total equivalent gate count for design	168,129		
Additional JTAG gate count for IOBs	6,384		

Table 1 shows that how much resources of FPGA are required to implement the equalizer with adaptive filter. The resources used by the proposed design are well below 40%.

IV. CONCLUSION

Equalizers are commonly used to combat the channel imperfections. Due to time varying property of the channel characteristics, the equalizer must be adaptive. In this work, a fractionally spaced equalizer has been synthesized and implemented on an FPGA device and resources used by the design are well below 40%.

REFERENCES

[1] S. Haykins, "Adaptive Filter Theory," Fourth edition, India: Dorling Kindersley, 2002.

[2] Wang Junfeng and Zhang Bo, "Design of adaptive equalizer based on variable step LMS algorithm," *Proceedings of the 3rd International Symposium on Computer Science and Computational Technology* (ISCSCT '10) JIAOZUO, P. R. China, pp. 256-258, 2010.

[3] Antoinette Beasley and Arlene Cole-Rhodes, "Performance of adaptive equalizer for QAM signals," *IEEE, Military Communications Conference*, vol.4, pp. 2373 – 2377, 2005.

[4] En-Fang Sang, Hen- Geul Yeh, "The use of transform domain LMS algorithm to adaptive equalization," *International Conference on Industrial Electronics, Control, and Instrumentation, Proceedings of the IECON*, vol. 3, pp. 2061-2064, 1993.

