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FPGA Implementation of A/D SINC Compensation Filter

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Abstract— The sigma-delta (Σ-Δ) ADC is the converter of choice for modern voice band, audio, and high-resolution precision industrial measurement applications. The Σ-Δ modulator produces a single bit output resulting in hardware saving and thus making them suitable for implementation in very large scale integration (VLSI) circuits. To reduce quantization noise produced, higher-order modulators such as multi-loop and multistage architectures are commonly used. . In this paper, theory and design of a sinc compensation filter, using FPGA, is explained for single bit sigma-delta A/D converter with medium oversampling ratio for the processing of audio signal. This filter is designed and simulated with MATLAB Filter Design Toolbox and finally mapped into XILINX virtex-2pro XC2VP30 series FPGA.

Keywords— Sigma-Delta ADC, Sinc filter, Digital filter, Signal processing, FPGA.

I. INTRODUCTION

Oversampled ADC architecture is preferred over Nyquist ADC due to their high signal to noise ratio and high resolution [1]-[2]. So for moderate speed application such as voice communication or digital audio technology oversampled ADC architecture are most preferable compared to Nyquist rate converters [3]. In case of Sigma Delta A/D converter the modulator portion behaves like a noise shaper and digital filter remove the out of band quantization noise thus ensure much higher SNR which is impossible to achieved in Nyquist A/D converter [4, 5].The Σ-Δ modulation techniques have been successfully applied in numerous applications such as low-cost and high-resolution A/D and D/A converters, software-defined radio [6, 7], correlators, multipliers, and synchronizers [8]. One main reason for popularity of Σ-Δ modulation lies in its ability to trade bandwidth with quantization noise. Σ- Δ circuit allows reduction in hardware complexity, while at the same time provides higher signal resolution. The fewer number of bits removes the need for expensive multibit circuitry such as multipliers and hence decreases the overall circuit complexity. In some cases, multipliers can be entirely eliminated from the circuit [9]. These features make Σ-Δ based circuits attractive for complete system-on-chip designs [10, 11].In this paper, theory and efficient realization of a sinc compensation filter is described and implemented in hardware using field programmable gate array (FPGA). The simulation and synthesis results of FPGA implementation of the filter are reported.

II. BASICS OF SIGMA DELTA ADC

A Σ-Δ ADC contains very simple analog electronics (a comparator, voltage reference, a switch, and one or more integrators and analog summing circuits), and quite complex digital computational circuitry, a digital filter (generally, a low pass filter).The Σ-Δ ADC operates as follows. Assume a dc input at VIN. The integrator is constantly ramping up or down at node A. The output of the comparator is fed back through a 1-bit DAC to the summing input at node B. The negative feedback loop from the comparator output through the 1-bit DAC back to the summing point will force the average dc voltage at node B to be equal to VIN. This implies that the average DAC output voltage must equal the input voltage VIN. The average DAC output voltage is controlled by the *ones-density* in the 1-bit data stream from the comparator output. As the input signal increases towards +VREF, the number of "ones" in the serial bit stream increases, and the number of "zeros" decreases. Similarly, as the signal goes negative towards –VREF, the number of "ones" in the serial bit stream decreases, and the number of "zeros" increases. From a very simplistic standpoint, this analysis shows that the average value of the input voltage is contained in the serial bit stream out of the comparator. The digital filter and decimator process the serial bit stream and produce the final output data. Block diagram of a 1st order Sigma Delta modulator shown in Fig.1.

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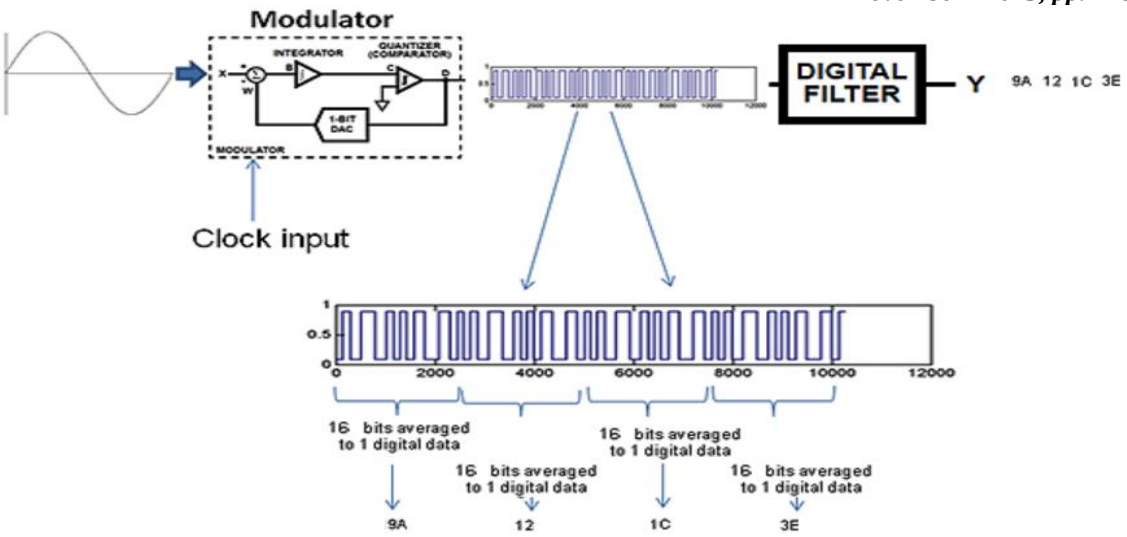

Fig. 1 Signal flow diagram of Sigma Delta ADC

The Σ-Δ ADC can also be viewed as a synchronous voltage-to-frequency converter followed by a counter. If the number of "1"s in the output data stream is counted over a sufficient number of samples, the counter output will represent the digital value of the input. Obviously, this method of averaging will only work for dc or very slowly changing input signals. In addition, 2N clock cycles must be counted in order to achieve N-bit effective resolution, thereby severely limiting the effective sampling rate.

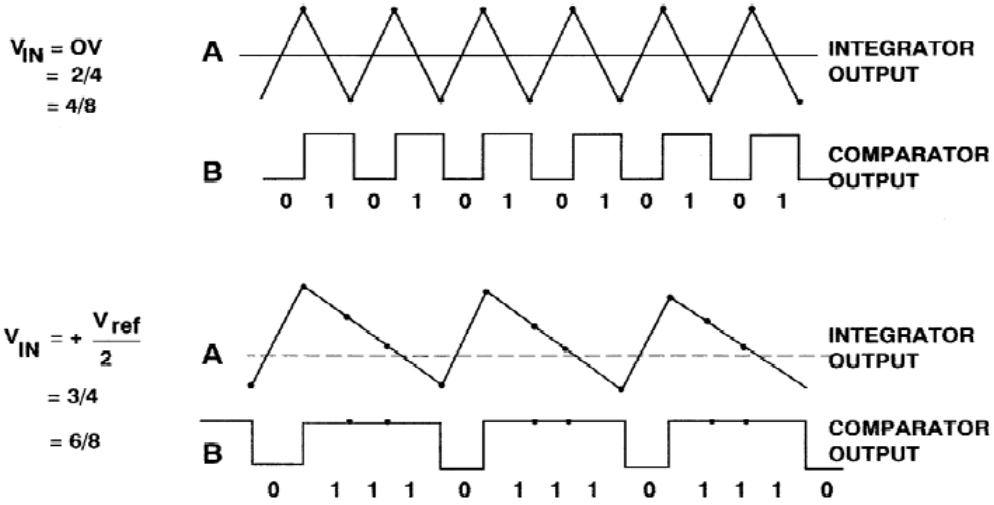

Fig. 2 Sigma-Delta Modulator Waveforms

III. DESIGN OF SINC COMPENSATION FILTER

A. Purpose of Filtering: Basic tasks are to be performed in the digital filter sections are:

1. Remove shaped Quantization Noise: The Σ-Δ modulator is designed to suppress quantization noise in the baseband. Thus, most of the quantization noise is at frequencies above the baseband. The main objective of the digital filter is to remove this out-of-band quantization noise. This leaves a small amount of baseband quantization noise and the band-limited input signal component. Reducing the baseband quantization noise is equivalent to increasing the effective resolution of the digital output.

2. Decimation or sample rate reduction: The output of the Σ-Δ modulator is at a very high sampling rate. This is a fundamental characteristic of Σ-Δ modulators because they use the high frequency portion of the spectrum to place the bulk of the quantization noise. After the high frequency quantization noise is filtered out, it is possible to reduce the sampling rate. It is desirable to bring the sampling rate down to the Nyquist rate which minimizes the amount of information for subsequent transmission, Storage or digital signal processing.

B. Sinc filter: The primary purpose of Sinc filter is to attenuate out of-band noise components from the SD modulators. While doing so, they decimate 1-bit SD data into lower frequency 16-bit data suitable for the FIR filter. An N-tap sinc filter is described by the impulse response.

$$h(k) = \frac{1}{N} \quad (0 \leq k \leq N-1)$$

An N-tap Sinc k filter is a cascade of *K* (*N/K*)-tap filters. The amplitude response of S*inc* filter is given by

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$$|H(f)| = \left| k \frac{\sin\left(\frac{\pi f N}{k}\right)}{N.\sin(\pi f)} \right|^{k}$$

Usually, a Sinc $^{L+1}$ filter is used to filter out the quantization noise of an *L*th-order modulator.
The Sinc filter has two cascaded sections, Sinc1 and Sinc2.

Sinc1 Filter The architecture of the first stage is shown in Fig.3

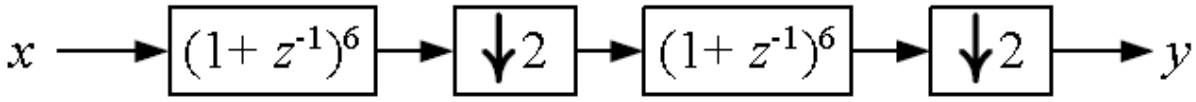

Fig.3 The architecture of the first stage

The decimation factor of 4 has been factorized as 2 × 2 to reduce area and power.
The first section is Sinc1 (6th order, 4 tap) fixed decimate by2 x 2 Sinc filter. This Sinc filter decimates the incoming 1-bit □□ stream from the modulators down to a 40 M Hz rate. 24 the combination of the two filtering blocks then gives

$$(1+Z^{-1})^6.(1+Z^{-2})^6 = (1+Z^{-1}+Z^{-2}+Z^{-3})^6$$

This is easily recognized as a sixth-order, four-tap sinc filter.

Sinc2 Filter The second section is Sinc2, a single stage 6th order, 7 tap fixed decimate by 2 Sinc filter. This Sinc filter decimates the incoming 16-bit stream down to a 20 M Hz rate.
System Function of this filter is given as

$$H(z) = \left(\frac{1-z^{-2}}{1-z^{-1}}\right)^6$$

Filter Coefficients are $h_0 = 1, h_1 = 6, h_2 = 15, h_3 = 20, h_4 = 15, h_5 = 6, h_6 = 1$.
Since the output digital signal is at Nyquist rate, a steep transition band and high stop-band attenuation are required so as to eliminate all the out-of-band noise while not affecting the in-band signal. This second stage has been designed to compensate for the attenuation introduced by the sinc stage in the pass band.

IV. PROPOSED DESIGN

The proposed design method has been applied to the design of a multi-stage digital filter to be used for sinc compensation in a ΣΔ analog-to-digital converter.

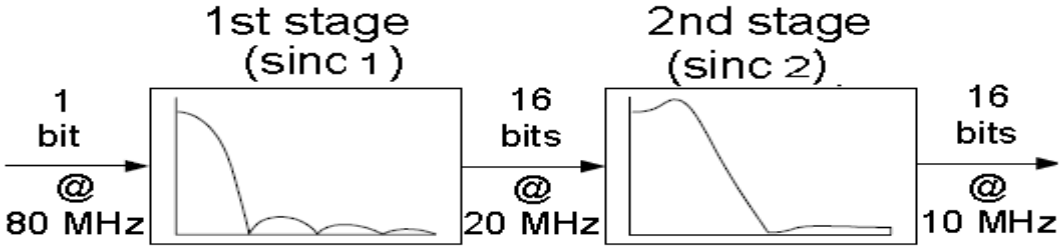

Fig. 4 Two-stage filter architecture

Frequency domain representation of input signal and floating Point output signal are shown below:

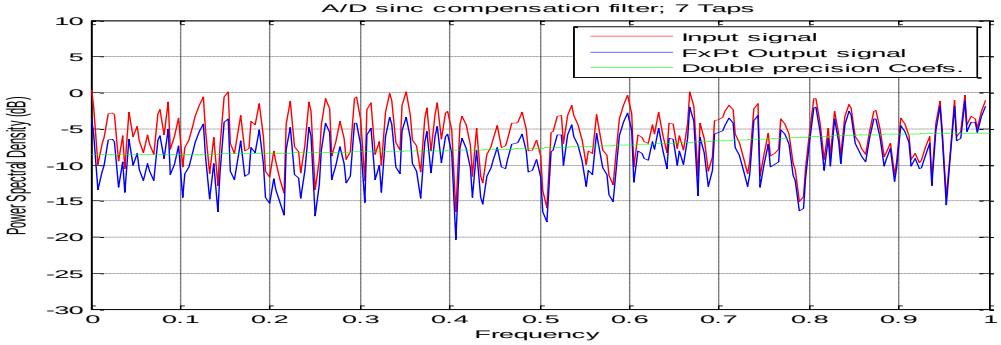

Fig. 5 A/D sinc Compensation Filter (7 taps) with Fixed Point

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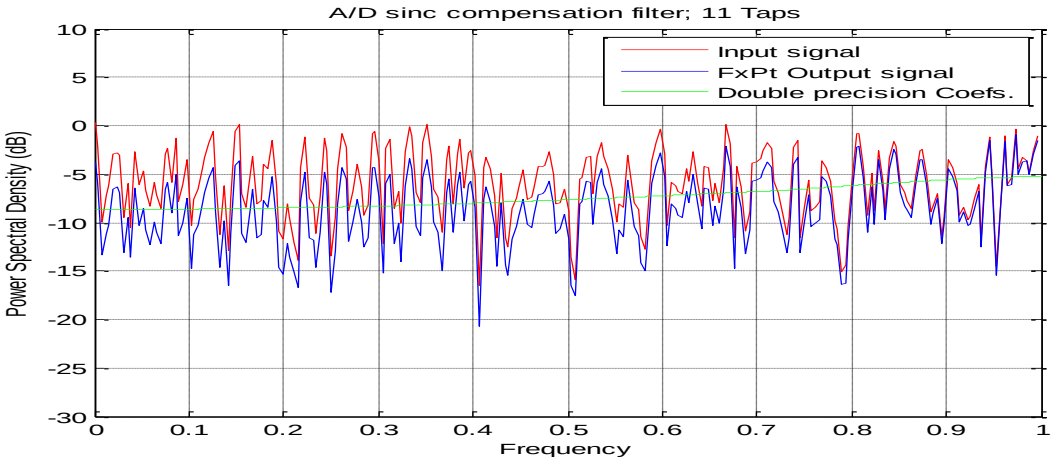

Fig. 6 A/D sinc Compensation Filter (11 taps) with Floating Point

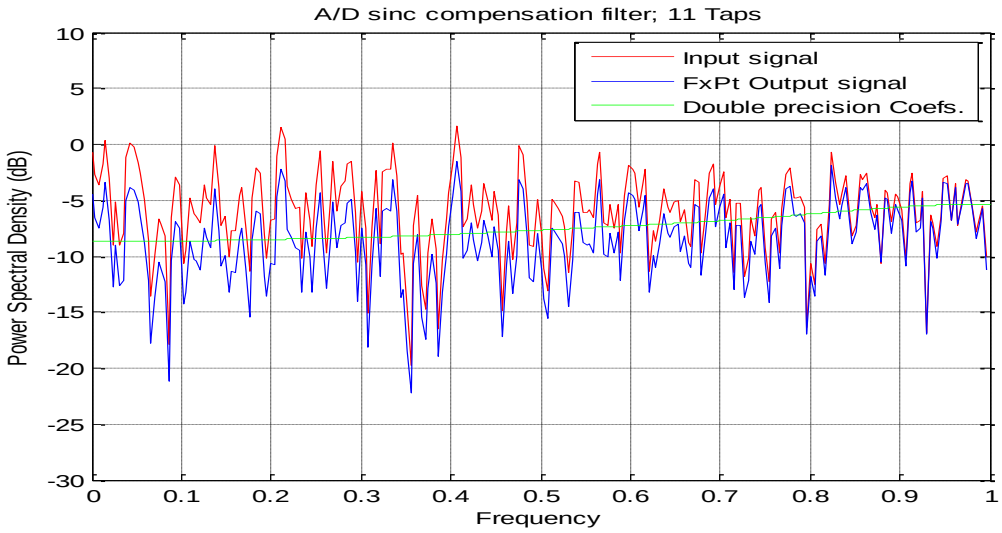

Fig. 7 A/D sinc Compensation Filter (11 taps) with Fixed Point

After successful simulation in MATLAB those digital filters are implemented into XILINX virtex2 pro FPGA. Using Simulink HDL coder VHDL codes of filters are generated and mapped into FPGA using Xilinx design tools. Reference sigma delta modulator portion is taken from FALCON digital communication trainer kit.

V. SIMULATION AND EXPERIMENTAL RESULTS

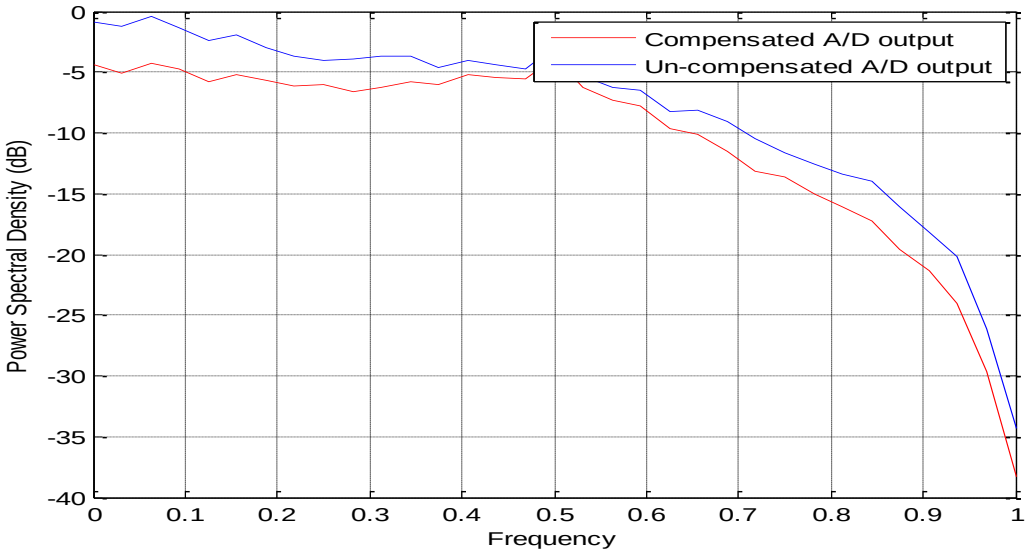

Fig. 8 A/D sinc Compensation Filter (7 taps Direct Form) with Floating Point

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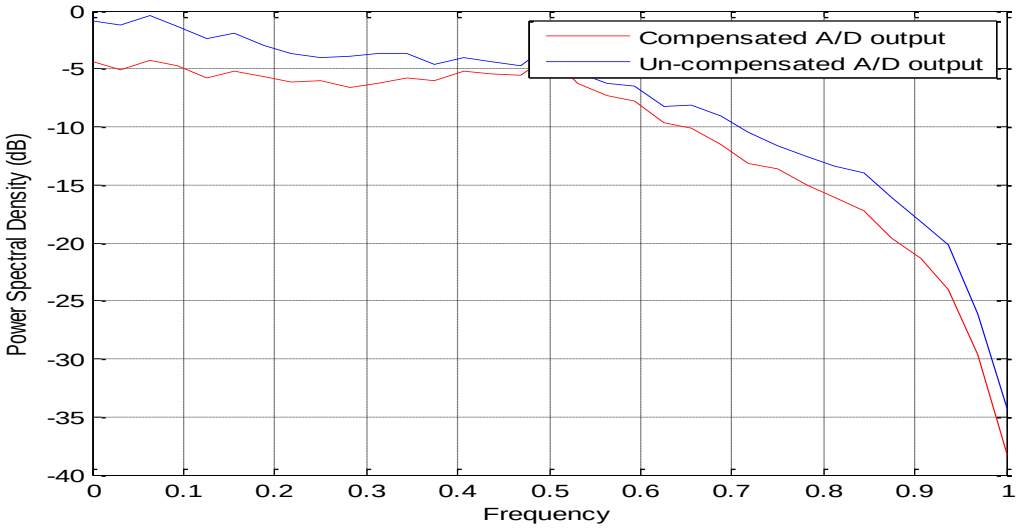

Fig. 9 A/D sinc Compensation Filter (7 taps Direct Form) with Fixed Point

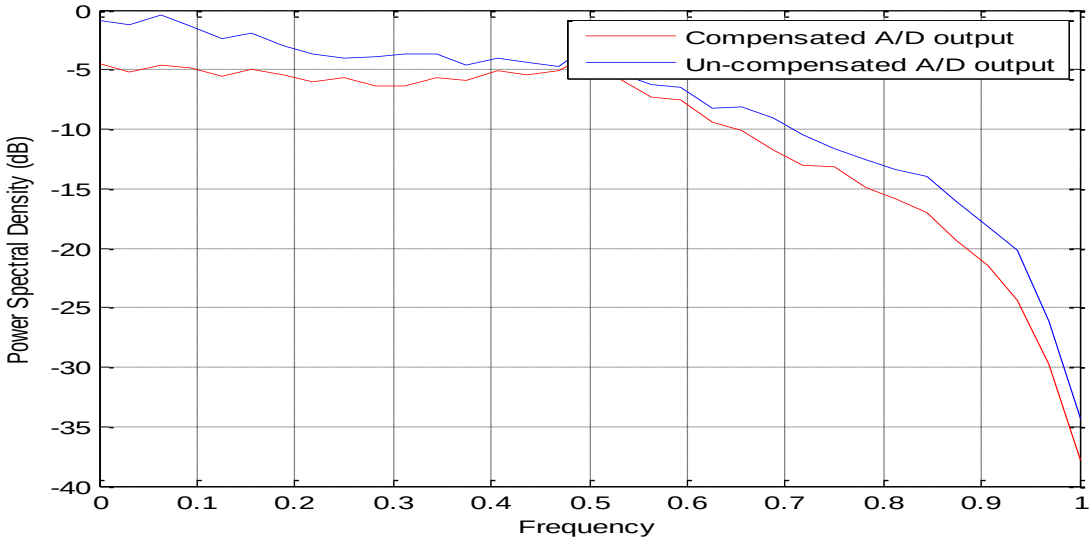

Fig. 10 A/D sinc Compensation Filter (11 taps Direct Form) with Floating Point

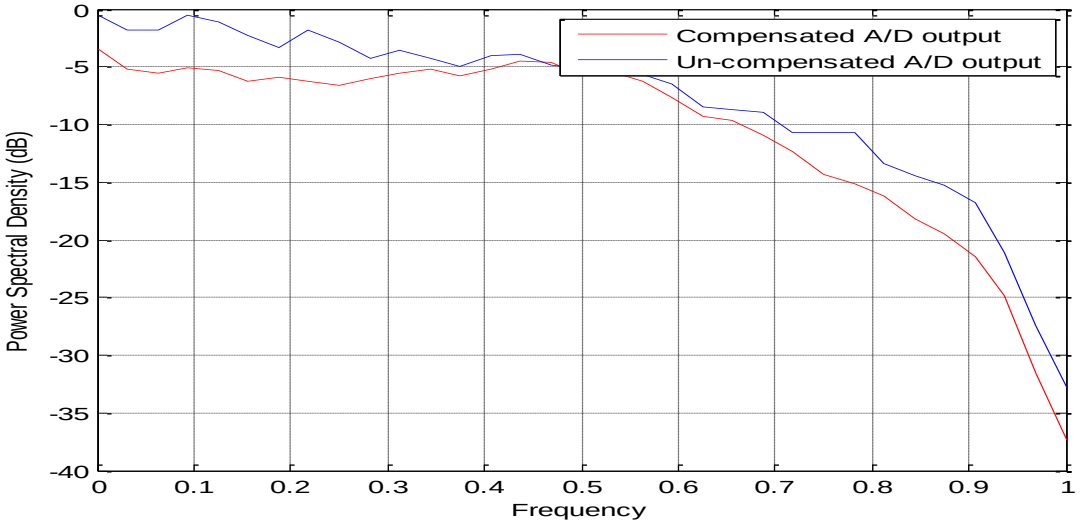

Fig. 12 A/D sinc Compensation Filter (12 taps Direct Form) with Fixed Point

Output of modulator is a single bit data, applied into FPGA board for digital filtering. Output of digital filter which is a multi bit digital data is displayed by using a PC based 34 channels Logic analyzer from HANTECH shown in Fig 13. Also the logic analyzer records the digital value into PC for offline processing.

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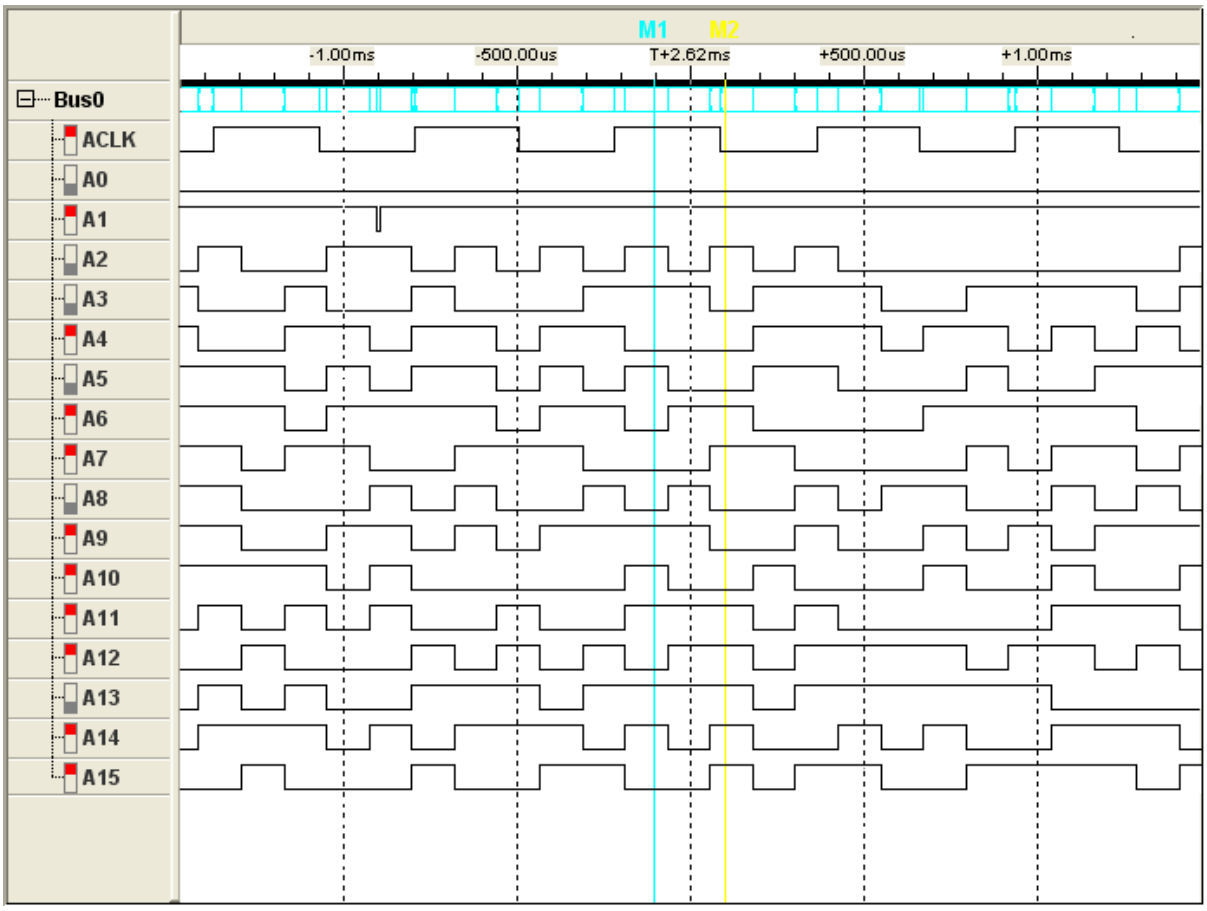

Fig. 13 Output of logic analyzer

Table 1. Number of configurable logic blocks required (after placement and routing), 7 Taps

Information	Count	Percentage Use
Slices	231 of 13696	1%
Slice Flip-Flops added for Registered Inputs	17	
Slice Flip Flops	307 of 27392	1%
4 input LUTs	281 of 27392	1%
bonded IOBs	0 of 556	0%

Table 2. Number of configurable logic blocks required (after placement and routing), 11 Taps

Information	Count	Percentage Use
Slices	340 of 13696	2%
Slice Flip-Flops added for Registered Inputs	17	
Slice Flip Flops	440 of 27392	1%
4 input LUTs	509 of 27392	1%
bonded IOBs	0 of 556	0%

VI. CONCLUSION

In this paper, Sinc Compensation Filter for single bit sigma-delta A/D converter was proposed.. The A/D sinc Compensation Filter with 7 taps and 11 taps Direct Form are successfully implemented successfully implemented into Xilinx virtex 2pro series FPGA. The results with floating point and fixed point are given in detail.

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