Design and Simulation of FPGA based Digital System for Peak Detection and Counting

Amitkumar Singh[*], S.K. Dubey   **M.G. Bhatia**
Department of Physics   *Ameya Centre of Robotics*
University of Mumbai, India   *Andheri, Mumbai, India*

Abstract— Field Programmable Gate Array's (FPGAs) are especially popular for prototyping integrated circuits designs. This paper describes the simulation of Peak detector and counter circuit based on FPGAs technology. Complete circuit was designed by writing appropriate program in Very High Speed Integrated Circuit Hardware Description Language (VHDL) & ISE foundation 6.1. The designed system was simulated using Modelsim simulator SE f.A maximum frequency of 190.513MHZ was reached with a minimum period of 5.249ns. 12 out of 3584 slices were used. Our system can be implemented on Xilinx Spartan 3 XC3S400~4pq208.

Keywords— VHDL, FPGA, Peak detector, Analog to digital converter, Counter, Pulse height analysis.

I. INTRODUCTION

Traditionally electronic system for particle detector has been made of almost all analog components as shown in fig. 1. In nuclear physics experiment nuclear particle interact with detector and produces a voltage pulse. The height of pulse is proportional to the energy deposited by nuclear particle in detector [1]. By measuring the height of pulse, energy of particle can be estimated and the process in known as Pulse height analysis. But signal that comes out of detector is very weak of the order of millivolt. To amplify this signal, it is passed through preamplifier. Preamplifier is analog circuit that receives the weak signal generated by detector and produces amplified signal. This analog signal is fed to an analog low pass filter which is applied to limit the frequency range of analog signal prior to sampling process. Signals coming out of analog filter are converted in to digital signals by analog to digital converter (ADC). Now these digital signals are forwarded to analog peak detection and counting system for the measurement of appropriate parameters.
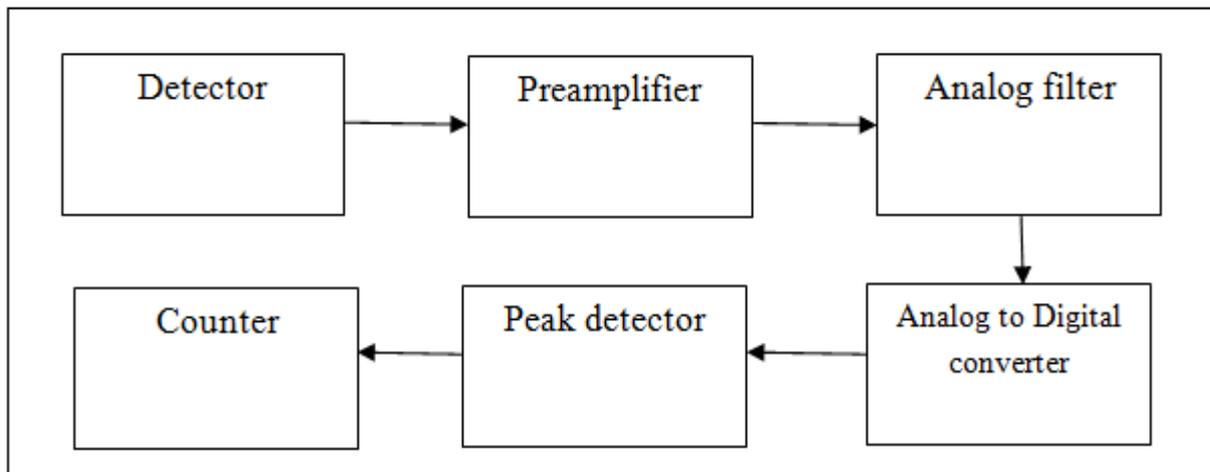

Fig.1 Function block of traditional electronic system for particle detection

Emerging high level hardware description and synthesis technologies in conjunction with Field Programmable Gate Array's (FPGAs) have significantly lowered the threshold for hardware development, opportunities exist to integrate these technologies into a tool for exploring and evaluating micro-architectural designs [2]. FPGAs are a semiconductor device containing programmable logic components and programmable interconnects. FPGAs are a particular family of integrated circuits intended for custom hardware implementation, with the key property of being capable of reconfiguration for an infinite number of times [3]. The use of hardware description languages (HDLs) allows FPGAs to be more suitable for different types of designs where errors and components failures can be limited.

Embedded circuits can be designed using Very High Speed Integrated Circuit Hardware Description Language (VHDL) and can be implemented on FPGAs. Because of their advantage of real-time in-circuit reconfigurability, the FPGAs based digital systems are flexible, programmable and reliable [4] [5]. In modern FPGA devices, differential input buffers are good comparators within a sufficiently large range of input voltage levels, since they are designed to be

compatible with various differential signalling standards. Many comparator based measurement methods using FPGAs are achievable [6]. It is possible to design a circuit as small as gates to as complex as microprocessor by using FPGAs [7].

In this paper, Digital system for Peak detection and counting was designed by writing appropriate program in VHDL on Xilinx ISE 6.1 platform and simulated using Modelsim simulator. Our designed system consists of Peak detection unit, 16-bit Counter unit and Tristate buffer unit.

II. SYSTEM ARCHITECTURE

In this paper, we present the FPGA implementation of simple peak detection and counting system, using limited resources. The designed system was implemented by using ISE foundation 6.1 and VHDL. Fig. 2 shows functional block diagram of our peak detection unit, 16-bit counter unit and Tristate buffer unit. The logic circuit for designed system is divided into three parts: the Peak detection unit, 16-bit Counter unit and Tristate buffer unit.
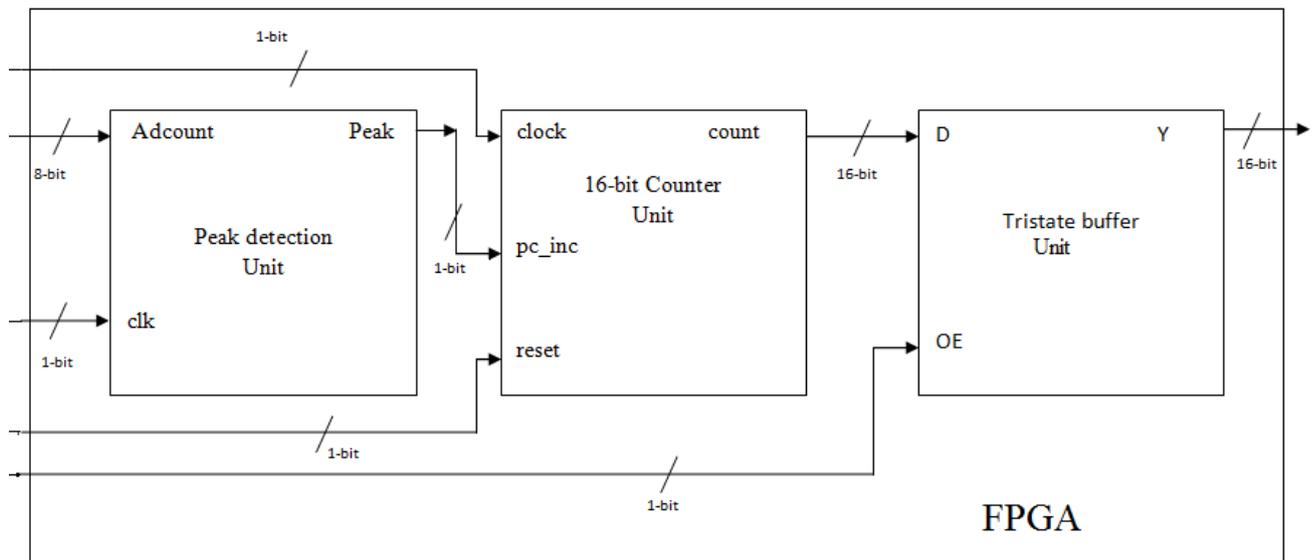

Fig. 2 Function block diagram of Peak detection and 16-bit counting system

A. Peak detection Unit
Peak detection unit is responsible for peak detection operation. Fig. 3 shows the schematic diagram of peak detection unit.

Fig. 3 Schematic diagram of Peak detection unit

The function of this block is to receive data from ADC and then detects the peak pulse signals. In this simulation model peak detector is designed to have a 3.5v or 10110010 binary threshold values. If the input signal is more than or equal to 3.5v or 10110010 binary the output of peak detector is logic 1 and if input signal is less than 3.5 v the output of peak detector is logic 0 . Threshold value can be changed by changing data of the threshold value in VHDL program.

B. 16-bit Counter Unit
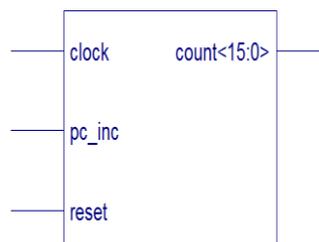Fig. 4 shows the schematic diagram of 16-bit counter unit.

Fig. 4 Schematic diagram of Counter unit

Function of this block is to accept the logical data from Peak detection unit and count the number of peaks. It is able to perform 65536 i.e. 1111111111111111 in binary counts after that it resets to 0 i.e. 0000000000000000 in binary.

C. Tristate buffer Unit
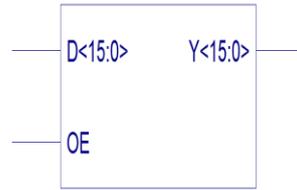*Fig. 5 shows the schematics diagram of 16-bit Tristate buffer unit.*

Fig. 5 Schematic diagram of Tristate buffer unit

Function of this block is to accept the data from counter unit and pass it to output Y, when OE pin is high. The content of this unit can be passed to external data output port by asserting output enable line OE of Tristate buffer unit.

III. IMPLEMENTATION AND VERIFICATION
All the units in our system were designed. These units were described in VHDL-modules and synthesized using ISE foundation 6.1. The functionalities of each unit was verified by Modelsim simulator. Finally all the units were combined together and once again tested using Modelsim simulator.

A. Peak detection Unit
Simulation result of Peak detection unit is shown in fig. 6. Simulation shows that when the input is more than 3.5 v or 10110010 binary the output of peak detection unit is logic 1.
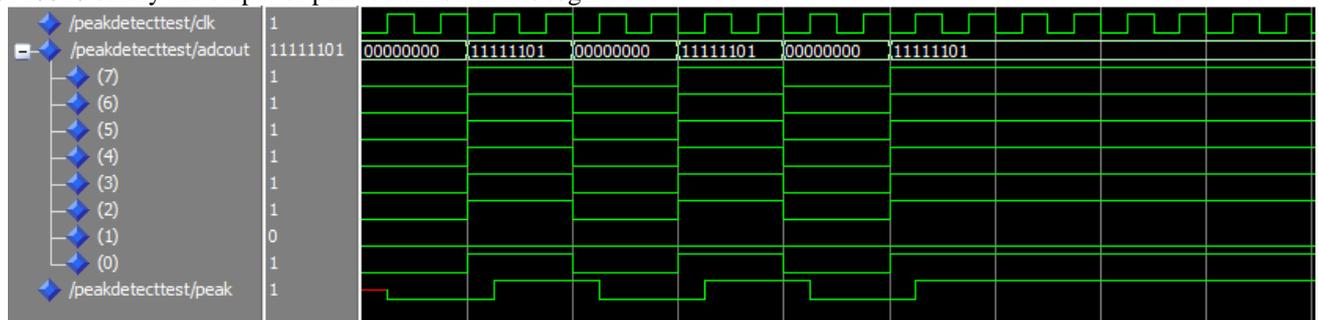

Fig.6 Peak detection unit simulation

B. 16-bit Counter Unit
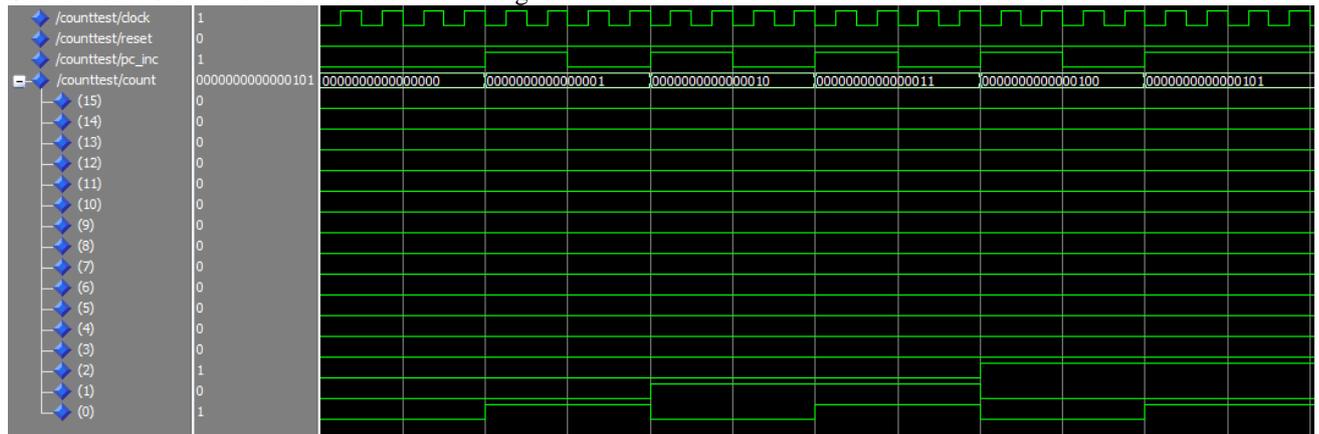Simulation result of counter unit is shown in Fig. 7.

Fig. 7 Counter unit simulation

C. Tristate buffer Unit
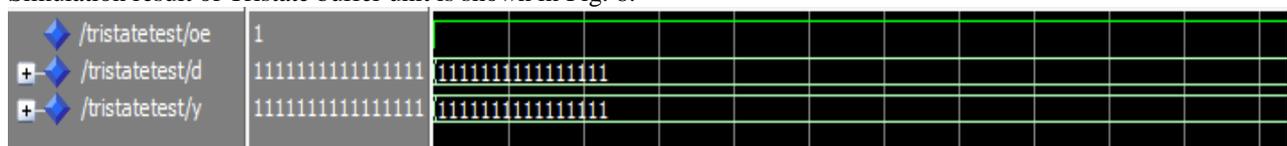Simulation result of Tristate buffer unit is shown in Fig. 8.

Fig. 8 Counter unit simulation

D. Peak detection unit, 16-bit Counter unit and Tristate buffer unit

Once the Peak detection Unit, 16-bit Counter Unit and Tristate buffer unit were simulated they were combined and a final digital system was constructed. Simulation result and Synthesis report for finally designed system is shown below in Fig. 9 and Table 1.

Fig. 9 final digital system simulation

TABLE 1
SYNTHESIS REPORT OF FINAL DIGITAL SYSTEM

Number of Slices	12 (0%)
Maximum Frequency	190.513MHz
Minimum period	5.249ns

IV. CONCLUSION

We have successfully simulated digital system for peak detection and counting, on Modelsim simulator using the VHDL language. Our digital system is made of peak detection unit 16-bit counter unit and Tristate buffer unit. Designed system has a maximum frequency of 190.513 MHZ and 12 slices were utilized. Our System can be implemented on Xilinx Spartan 3 xc3s400~4pq208 using ISE foundation 6.1 and VHDL language.

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