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Relative Techniques with Histogram Technique for Estimation of Different Testing Strategy of ADC

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Abstract: Various improved method for Analog to digital converter (ADC) testing are evaluated. The ADC static and dynamic parameters i.e. offset error, gain error, NOB and nonlinearity errors like INL, DNL are obtained from sine-wave histogram test. Therefore, the relationships among these parameters are analyzed. With the appropriate approximation in the reference sine wave histogram and the estimation of the ADC parameters, the realization of an ADC output analyzer.

Keywords: ADC testing; DNL; INL; Gain error, Offset error, Histogram technique.

I. INTRODUCTION

Testing and characterizing Analog to Digital Converter (A/D Converter or ADC) is still a challenging issue for mixed signal device manufacturers and designers, both in terms of time and cost. Generally the goal of such procedure is to verify in a short time whether a given ADC meets its performance requirements. As known, many techniques in the time, frequency and amplitude o been proposed for ADC testing. ADC is an important device widely used in many electronics applications like: instrumentation systems, communication system, medical Instrumentation, radar system and military applications for interfacing analog electronics with digital electronics. Dynamic testing using sine wave input based on histogram method is an important activity for characterization of an ADC. These parameters attest the capacity of the ADC to perform its intended function [1] [2]. ADCs are rarely used alone, but are often included in more elaborate systems. The performance of the ADCs will affect the performance of the system where it is included and the precision with which the ADC parameters are known is necessary to compute the precision of the final result of the system using it. Standard histogram technique is popular method which estimates the parameters of an ADC. The main aim of dynamic testing is to determine functional parameters of an ADC which are responsible for the accuracy, resolution, speed and linearity of the conversion process. Sophisticated test instruments needed for testing high resolution and high speed ADCs are costly, complex and bigger in size.

II. GENERAL HISTOGRAM TEST SETUP MODEL

Histogram technique is achieving more popularity due to complete characterization of ADC with high accuracy and high resolution. For dynamic testing of ADC, the common input stimulus are full-scale sinusoidal and triangular signals. But triangular wave testing is relatively less popular due to higher distortion present in generation. In dynamic testing of ADC, the functional parameters are highly dependent on the type of input signals as in figure 1.

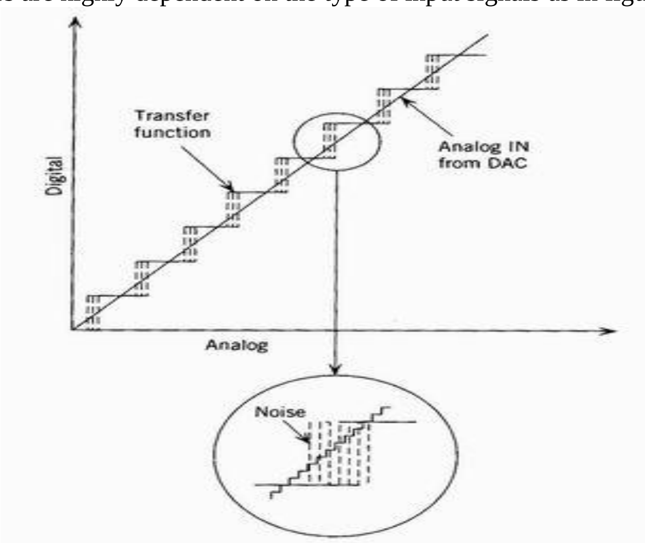

Fig. 1 ADC static test result

Histogram technique is achieving more popularity due to complete characterization of ADC with high accuracy and high resolution. For dynamic testing of ADC, the common input stimulus are full-scale sinusoidal and triangular signals. In dynamic testing of ADC, the functional parameters are highly dependent on the type of input signals. Ideal ADC model as shown in figure 2.

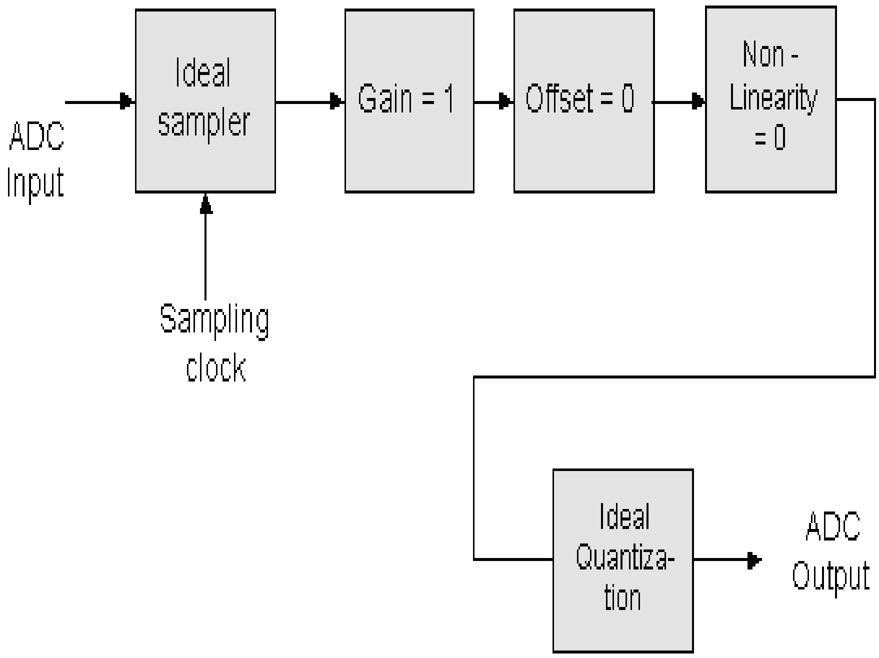

Fig. 2 Ideal ADC model

III. ESTIMATION OF DIFFERENT TESTING STRATEGY OF ADC

Histogram method is one of the popular techniques for ADC testing. This revels the offset error, gain error, nonlinearity error and ENOB of an ADC under test. A full scale sine wave is input to the ADC under test and large numbers of samples are taken at specified sampling frequency and transfer to the computer. Frequency of sine wave is selected to non coherent with sampling rate of the ADC. Histogram is constructed between frequencies of occurrence of a ADC code. For an ideal ADC fixed number of occurrence of each code exists which depends upon parameters like input frequency, sampling frequency and number of samples. Transfer function is described as follows [3]-[4].

$$G \times T[k] + V_{os} + \varepsilon[k] = Q \times (k-1) + T_1$$

Using conventional least- squares estimation technique; we get G and Vos as,

$$G = \frac{Q(2^N-1)\left(\sum_{k=1}^{2^N-1} kT[k] - 2^{(N-1)}\sum_{k=1}^{2^N-1} T[k]\right)}{(2^N-1)\sum_{k=1}^{2^N-1} T^2[k] - \left(\sum_{k=1}^{2^N-1} T[k]\right)^2}$$

$$V_{os} = T_1 + Q(2^{(N-1)}-1) - \frac{G}{(2^N-1)}\sum_{k=1}^{2^N-1} T[k]$$

G is the Gain, Vos is the offset, T1 is the ideal value corresponding to T[1], T[k] is the input value is the ideal width of a code bin. ε[k] is the residual error .

Dynamic performance evaluation of high speed ADCs was investigated and it was found that the accuracy of ultra high speed ADC decreases at higher frequencies. A new dynamic test method was proposed for determination of nonlinearity and effective resolution of A/D converters [5]-[8]. DNL values were computed by deviation of actual histogram from ideal histogram. ENOB was determined by combination of histogram and least square error minimization techniques [9]-[13]. A new method with sine wave histogram was presented for estimation of dynamic error function [14]. After that a Built-in-self test (BIST) scheme using the histogram test technique was proposed which discusses the viability of a BIST implementation for the sinusoidal histogram technique used for ADC testing [15]. ADC histogram test [16] using small amplitude triangular waves was carried out which exploits the use of small amplitude triangular waves. Proposed methods show that the new technique can perform the test in a small time fraction of standard one, for the same accuracy level. The accuracy of ADC sine wave histogram testing is analyzed [17] under the quasi-coherent sampling using through analysis and determine the estimation accuracy. Francisco Andre et al [18] have proposed an approach for the study of the gain error, offset error and variance of the number of counts of the histogram and the cumulative histogram. The exact knowledge of this variance allows for a more efficient test of ADCs and a more precise determination of the uncertainty of the test.

Table I: Summary of various parameter of ADC

Name of authors	Year of Publication	Name of Techniques	ADC parameters computation	Remarks
F A Zais and SBeemand	2000	BIST Histogram	DNL, INL, ENOB and offset and gain error	Histogram BIST technique is used
R Holicer and L MIchael	2001	Histogram	DNL	Exponential stimulus are used
S Acunto and P Arpia	2003	2-D- Histogram	INL	2-D used for error compensation
A Cruz Serra and P Ramos	2004	Histogram and spectral analysis	INL and DNL	Nose Signal are used as stimulus
Dr D K Mishra	2005	Histogram	DNL, INL and ENOB	Probability computation &code transition level used
Francisco Andre Correa Alegria	2005	Ramp histogram	Transition Voltage	Over drive require for lower value
Linus Michaeli,Peter Michalko,Jan Saliga	2006	Triangular histogram	DNL,INL	Simple estimation of ADC nonlinearities without need of high accuracy of instrument
Niclas Bjorsell,Peter Handel	2006	Gaussian histogram	INL,DNL	Accuracy increases for fixed sample length
Francesco Adamo,Filippo Attivissimo, Nicola Giaquinto	2007	Measurement of hysteresis cycles	Dynamic Nonlinearities	Simple solution to measure nonlinearities
Henrik F.lundin,Peter Handel,Mikael Skoglund	2007	MMSE –Optimal additive static correction	SINAD.ENOB,DNL	Results are improved
Hsin-Wen Ting,bin-Da Liu,Soon-Jyh Chang	2008	Sine - Wave histogram	DNL,SNR .Offset error	Measurement were performed with good output
Esa Korhonen,Juha Kostamovaara	2008	Standard Histogram test method	DNL,INL	Good accuracy with lower Db of stimulus signal
F.Alegria, A.Cruz Serra	2009	Independently based histogram	INL,DNL.SNDR,ENOB	For 8 bit ADC experiment give good result over FFT method
S.C. Vora & L.Satish	2010	Non linear Ramp histogram	Nonlinearities	Significant reduction in the influence of source nonlinearity can be achieved.
R.S.Gamad and D.K.Mishra	2011	Code transition level	DNL,INL,ENOB	Effect of overdrive and additive noise on ENOB for 5bit ADC
Jingbo Duan	2011	Linearity & spectral test	SNR	This method does not required accurate sinusoidal stimulus
Zhongiun Yu	2012	New algorithm to taste linear ADC	Precision, error	Reduce ADC linearity test cost
Jingbo Duan	2012	Built-in-self test	Offset and gain error	Low cost with good accuracy

IV. FUTURE TRENDS OF TECHNOLOGY

Current research includes search of high resolution approach used with BIST .Recently histogram technique is used to improve design to get better estimation of ADC functional parameter which in turn give proper determination of A\D conversion accuracy. Dynamic testing of an ADC is done to determine functional parameters through simulation. As mentioned earlier, an algorithm developed [19] through simulation is equally suitable for testing a real ADC. In future work one can test a real ADC (8 bit CMOS/Bipolar flash ADC) by connecting in application and applying sine wave/triangular wave or application input through arbitrary waveform generator. ADC output can be fed to a computer after sampling ADC by a clock generator circuit. The ADC output code collected by computer can be stored in the memory of the computer and different ADC parameters can be computed by using histogram methods already available in the literature or by methods proposed in this work. The experimental results can be compared with the simulation results and analysis of the results can be done.

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