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High Performance Circuit Level Design For Multiplier

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***Abstract*— Addition is one of the fundamental arithmetic operations, which is used extensively in many VLSI systems such as application-specific DSP architectures and microprocessors. The adders determine the overall performance of the circuits in most of those systems. This paper introduces a novel low power and high-speed 8-Transistor 1-bit full adder cell, which is proposed. In this design, a novel low power and high speed 8-Transistor 1-bit full adder cell have six MOS transistors and multiplexer using two MOS transistors are applied to minimize the transistor count and reduce the power consumption and delay. The power dissipation and delay of the new design against other designs are analyzed via HSPICE simulations. The results feature that the proposed adder has both lower power consumption and high-speed operation. The combination of low power and low transistor count makes the new 8T full adder cell a viable option for an efficient design.**

***Keywords*— Full-adder design, low power, CMOS circuit, multiplexer, very large-scale Integration (VLSI)**

I. Introduction

The design of Multiplier, full adders forms the basic building blocks of all digital VLSI circuits has been undergoing a considerable improvement, being motivated by three basic design goals, viz. minimizing the transistor count, minimizing the power consumption and increasing the speed. Great effort has been concentrated on low-power microelectronics due to high-speed development of laptops, portable systems and cellular networks. Adder is the core element of complex arithmetic circuits as it is used in the automatic logic unit (ALU), in the floating-point unit, and for address generation in case of cache or memory access. The extensive use of this operation in arithmetic functions attracts many researchers to investigate in this field. The full adder design in static CMOS, with complementary pull-up PMOS and pull-down NMOS networks is the most conventional one but it requires as many as 28 transistors. The transmission function full adder (TFA) cell is based on the transmission function theory and it has 16 transistors. In the design is further reduced to only 14 transistors using the lower power XOR design and transmission gates. In most of the twenty full-adder cells were novel circuits at that time. They were formed from combinations of various XOR/XNOR, Sum and Cout modules. All of above circuits can operate with full output voltage swing. To pursue even fewer transistor count and lower power consumption, pass transistor logic (PTL) can be used in lieu of transmission gate. A new full adder called static energy-recovery full-adder (SERF) uses only 10 transistors. It has been reported to be the least power consuming. Note that in PTL, the output voltage swing may be degraded due to the threshold loss problem. In other words, the output high (or low) voltage is deviated from the Vdd (or ground) by a multiple of threshold voltage Vt.

However, the circuits based on PTL are certainly useful in building up larger circuits such as multiple-bit input adders and multipliers. In this paper, a new low-power and high-speed full adder cell using only 8 transistors is presented, namely new 8T full adder. In order to demonstrate the efficiency of the new design, some general characteristics of the new design, such as power consumption and delay, against other different types of five full adder cells are performed.

II. Previous Work

The full adder function can be described as follows: The addition of two 1-bit Inputs A and B with forestage carry Cin calculates the two 1-bit outputs Sum and Cout, where

$$Sum = A \text{ xor } B \text{ xor } Cin \quad (1)$$

$$Cout = A \text{ and } B + Cin \text{ and } (a \text{ xor } B) \quad (2)$$

The above equations can be rewritten as

$$Sum = (A \text{ xnor } B) \text{ xnor } Cin \quad (3)$$

$$Cout = (A \text{ xnor } B) \text{ and } Cin + (A \text{ xnor } B) \text{ and } A \quad (4)$$

From equation (3) and (4), we can easily identify two basic modules needed in implementing the full adder function, i.e., XNOR and 2-to-1 multiplexer.

III. New 8T Adder Design

The proposed new 8T full adder (fig.1) cell requires only 8 transistors to realize the adder function. The design is based on a modified version of a CMOS inverter and a NMOS transistor. When the input B is at logic low, the inverter on the left functions like a normal CMOS buffer. Therefore the

output Y is same as that of input A. When the input B is at logic high, the inverter on the left acts as normal CMOS inverter and output is the complement of the input A. The operation of the whole circuit is thus like a 2 input XNOR gate. However, when A= 0 and B=1, voltage degradation due to threshold drop occurs across transistor M3 and consequently the output Y is degraded with respect to the input. The voltage degradation due to threshold drop can be considerably minimized by increasing the W/L ratio of transistor M3. The proposed full adder circuit (fig. 2) which uses two XNOR and one multiplexer, it's give the less delay product compare to 8 T Full Adder based on XOR. Requires only eight transistors—the one with the least transistor count learned so far from the literatures. In the following section, analyses and simulations will be conducted to compare proposed adder with other designs in various circuit characteristics

IV.Multiplier design using proposed full adder

High-speed multiplication is another critical function in a range of very large scale integration (VLSI) applications. Multiplications are expensive and slow operations. Multiplication is an important basic arithmetic operation and less common operation than addition, but it is still essential for microprocessors, digital signal processors and graphic engines. Multiplication is logically carried out by a sequence of addition, subtraction and shift operations. Therefore, high-speed multiplication can be achieved by having a high-speed multiplier.

Tree topologies are very fast structure for summing partial products. In a tree, counters are connected mostly in parallel although trees are faster than arrays; they both use the same number of counters to reduce the partial products

In all the cases, the design of different types of multiplier structures
1.Array multiplier
2.Wallac tree multiplier
3.Baugh woogly multiplier
4.Braun multiplier

V. D Flip-Flop

In digital circuits, a flip-flop is a term referring to an electronic circuit that has two stable states and thereby is capable of serving as one bit of memory The D flip-flop is the most common flip-flop in use today. It is better known as delay flip-flop. In this filter design one D flip-flop consumption of power is 15.02mw. Power consumption is increased due to the number of tap. Ever since its very inception, the semiconductor

VI. The Results of Simulation and Comparison

In this paper, several different designs are included for performance comparison. With proposed new 8T adder. Altogether eight adders are analyzed with respect to number of transistors used, their respective power dissipation and delay including the proposed NEW 8T adder. In this research work, the following 9 different adders are designed namely, 14 Transistor Full Adder, 20 Transistor Full Adder, 28 Transistor Full Adder, Conventional Full Adder, Transmission Functional Full Adder, Transmission Gate Full Adder, Static Energy Recovery Full Adder, NEW Full Adder and new 8T adder. The 28T full adder mentioned in Section I, which is used as basis of comparison in many literatures. The SERF, The design is claimed to be extremely low power because it dose not contain direct path to the ground and can re-apply the load charge to the control gate (energy recovery). The CLRCL (complementary and level restoring carry logic), features lower operating voltage, higher computing speed and lower energy operation. The design adopts inverter buffered XOR/XNOR designs to alleviate the threshold voltage loss problem. All the schematics are based on 0.18-μm technology with a 1.2V supply voltage, and are simulated using HSPICE. In order to analyze the compare the performance of the proposed new 8T adder with previously reported adders, extensive simulation studies have been carried out on the different types of adders. Each circuit is simulated with the same testing conditions. The net lists of those adders are extracted and simulated using HSPICE. From the simulation results, it is found that the proposed new 8T adder has correct logic function at supply voltage 1.2V, but it suffers from the threshold loss problem when the supply voltage is below 1.2 which can be reduced by sizing the transistor M3.The following table 2 shows the delay comparison of different adder cells.

The results of the comparative study show that the performance of the 8T full adder is somewhat poorer than the 10T full adder proposed, in regard to its average power dissipation. However, the delay of the proposed adder is much less compared to any other adder shown in the table 2. The net effect is that our proposed 8T full adder shows a much better power-delay product (PDP) compared to any other adders mentioned in literature. It is evident that the proposed 8T full adder occupies the minimum silicon area on chip amongst all the full adders reported so far. The small silicon area of the proposed full adder makes it potentially useful for building compact VLSI circuits on a small area of chip. The proposed 8T full adder has the smaller figures in higher output load. From comparison of different designs, the proposed new 8T adder is a good candidate to build large circuits, such as multipliers with low power consumption. Digital Fir Filter using Wallac tree multiplier give the better performance among all types of multiplier in respect delay and power consumption. Moreover, the small area of this adder can reduce the area of these systems.

VII. Figures and Tables

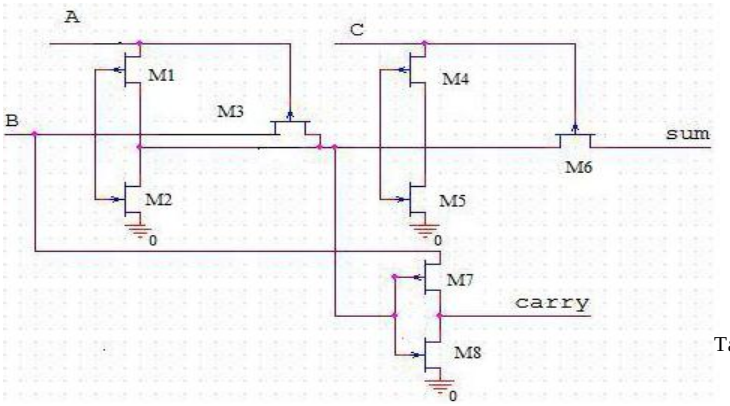


Fig. 1: Existing 8 Transistor XOR Full Adder

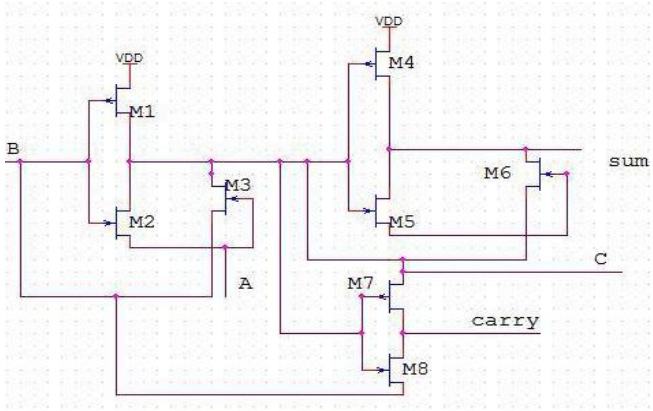


Fig. 2. – Proposed 8 Transistor XNOR Full Adder

Table 1 : Number of Transistor observation

Adder Type	Number of Transistors
14 Transistors Full Adder	14
20 Transistors Full Adder	20
28 Transistors Full Adder	28
Conventional Full Adder	32
New Full Adder	14
SERF	10
Transmission Functional Full Adder	16
Transmission Gate Full Adder	24
New 8T	8

Table 2: Delay observation for 1.2v

Adder Type	Delays (ns)
14 Transistors Full Adder	3.6
20 Transistors Full Adder	3.7
28 Transistors Full Adder	3.6
Conventional Full Adder	3.9
New Full Adder	2.4
SERF	2.2
Transmission Functional Full Adder	3.9
Transmission Gate Full Adder	5.0
New 8T	0.184

Table 3: Power dissipation observation for 1.2v

Adder Type	Power Dissipation (in mW)
14 Transistors Full Adder	256
20 Transistors Full Adder	315
28 Transistors Full Adder	196
Conventional Full Adder	170
New Full Adder	163
SERF	220
Transmission Functional Full Adder	650
Transmission Gate Full Adder	427
New 8T	0.11508

Table 4: Delay observation for 1.2v

3 Transistor	Delay (ns)
Existing 3 Transistor XOR	0.317
Proposed 3 Transistor XNOR	0.263

Table 5: Power dissipation observation for 1.2v

3 Transistor	Power dissipation (μw)
Existing 3 Transistor XOR	65.268
Proposed 3 Transistor XNOR	0.185

Table 6: Delay observation for 1.2v

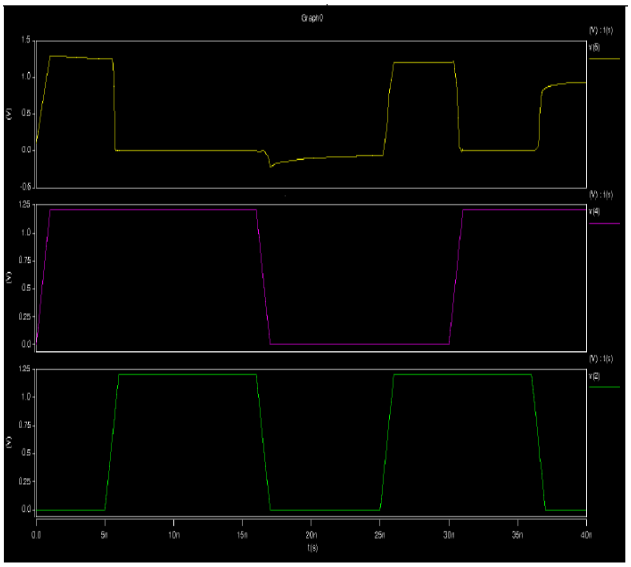
8 Transistor Adder	Delay (ns)		
	Sum Delay	Carry Delay	Total Delay
Existing 3 Transistor XOR	0.02	0.27	0.29
Proposed 3 Transistor XNOR	0.064	0.12	0.184

Table 7: Power dissipation observation for 1.2v

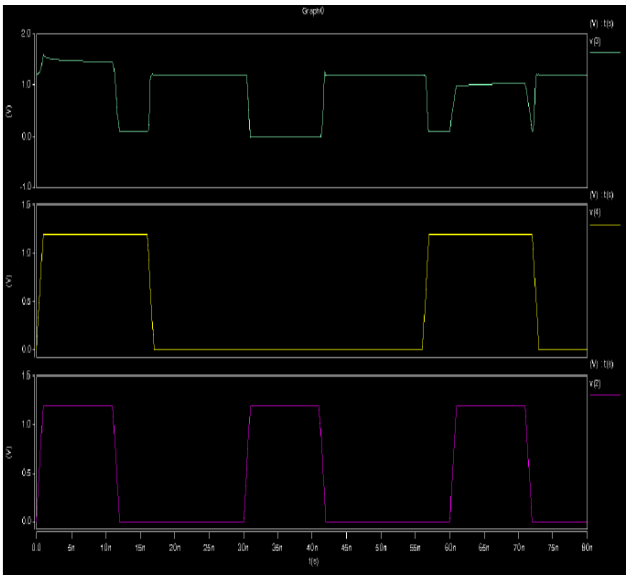
8 Transistor Adder	Power dissipation (µw)
Existing 3 Transistor XOR	115.08
Proposed 3 Transistor XNOR	0.376

Table 8: Observation table for Multiplier

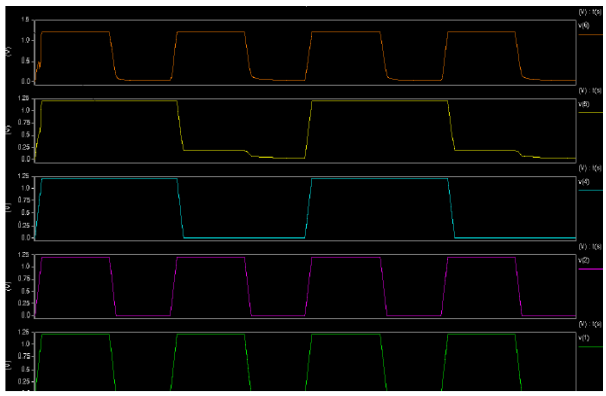
Multiplier	Power dissipation due to existing adder(µw)	Power dissipation due existing full adder (µw)
Array multiplier	115.77	0.7272
Wallac tree multiplier	62.01	0.6510
Braun multiplier	509.5	505.8
Baugh woogly multiplier	291.6	209.4



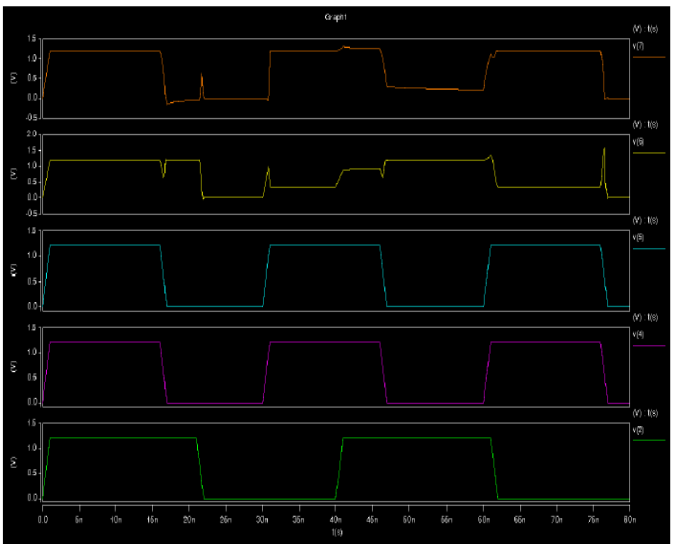
1.Simulation of 3 Transistor XOR



2.Simulation of 3 Transistor XNOR



3. Simulation of 8 Transistor XOR Adder



4. Simulation of 8 Transistor XNOR Adder

VIII. CONCLUSION

The current work proposes the design of an 8T full adder, which is by far the full adder with the lowest transistor count. The proposed XNOR gate also has a much less delay and hence much less power delay product than its peer designs. Using the XNOR gate an eight- transistor adder has been realized using the conventional logic equations of the full adder circuit. The designed adder is found to give better performance than most of the adders mentioned in literature so far as the power-delay product is concerned. The proposed full adder can operate at low voltages, yet giving quite a good speed. The design of digital FIR Filter using wallac tree multiplier based on the proposed full adder is giving good performance.

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