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Multi-Valued Logic Applications in the Design of Switching Circuits

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Abstract—

In this paper we review the development & advantages of multi valued logic. The multi valued logic has been object of research over last few decades. Since 1971 there have been annual symposiums on multi valued logic.
The use of non binary logic or discrete-analog signal processing is not out of the question if the multiple-valued hardware algorithms are developed for fast parallel operations. While today digital electronics is implementationaly binary, multiple-valued logic (like Ternary) has been becoming increasingly more important in hardware implementations of sophisticated algorithms. In particular, data-path & switching logic may benefit significantly from multiple-valued design, because faster & more energy-efficient arithmetic become feasible. Multiple valued logic offers important advantages like more information can be processed over given set of lines to reduce the burden of interconnections & there by switching Nevertheless the subject area of multiple-valued logic is a very necessary one to research, without it no developments to supplement the binary will occur.

Keywords— ***Multi valued logic, Switching logic, Binary, Ternary, Interconnections***

I. INTRODUCTION

The principle areas of MVL research are multiple-valued algebras, multiple-valued semiconductor circuits and multiple-valued network synthesis. These three areas have a considerable degree of interaction and overlap; for example realistic network synthesis relies upon the availability of a relevant semiconductor circuits, and these circuits in turn should represent the operators used in formal algebras [1].The development of technology for large-scale system integration seems to continue also in the future at a rapid pace, however, now devices are so fast that these can be considered as switching in no time with an increasing density of chips, the number of inter chip connections is greatly increased as more and more functions are put on the same chip [2].

Multi valued logic offers important advantages like more information can be processed over given set of lines to reduce the burden of interconnections & there by switching [3]. The information content per interconnection can be raised from the present binary level to multilevel by multi valued logic [4].

The advantages of MVL are the use of fewer operations, potentially fewer gates and the reduction in the number of interconnections & switching such as buses where a

bus line operating under a MVL system can contain more information than a binary equivalent. The reduction of dynamic power dissipation in VLSI applications is a major challenge for today's engineers. In modern VLSI systems, a large proportion of power is consumed by interconnect & switching [5]. But key issue in MVL systems is development of superior multi valued hardware algorithms and appropriate devices.

II. MULTI-VALUED LOGIC SWITCHING CIRCUITS

The most generally used switching circuit components today are two-valued or binary. The electrical conditions controlling these switching circuit components are also generally two-valued or binary. But integrated circuits can now handle multiple valued signals & switching at high speed rather than binary signals, especially at data communication level because of the reduced interconnections & switching [6].

Utilization of multi valued logic (MVL) reduces the number of signals involved in the communication, increasing their information content. In such a way, an interconnection-limited design can be realized with MVL like for the asynchronous circuits and comparable performance than a classical binary design may be obtained [7]. Among various types of MVL, the ternary logic receives more attention than others because of lower interconnection cost estimation and a simple electronic circuit implementation method [8].

III. RELATED WORK

a) The early developments in Multi-valued Logic:

Alexander showed that the most efficient radix for implementation of switching system is natural base (e = 2.71828). Thus it seems likely that the best integral radix is 3 rather than two. Stanley L. Hurst (1988) has taken review of the work in Multi-valued Logic. He mentioned that the early research work is mainly in multi-valued algebra. Later the attempts were made to formulate efficient multiple-valued logic circuits, using circuit concepts based upon:

- Bipolar ECL technology
- Bipolar I2L technology and

- Unipolar CMOS technology.

Other technologies which have been considered for MVL are charge-coupled-device CCD technology and opto-electronic technology.

Prabhakara C. Balla and Andreas Antoniou[1984] have proposed a low power dissipation MOS ternary logic family, which is comprised of a set of ternary inverters, NOR gates, and NAND gates. Higuchi and Kameyama have shown that the realization of combinational and sequential logic functions is possible using a ternary logic element which they refer to as the T-gate. In addition, they have proposed an implementation of the T-gate using bipolar transistors, and considered its application to the synthesis of combinational as well as sequential logic circuits. Mouftah and Smith have proposed an alternative implementation of the T-gate using MOS technology, but the difficulty was the synthesis of an N-variable combinational logic circuit requires (3N – 1)/2 T-gates consequently, the complexity of the logic circuit increases rapidly as the number of variables is increased. This appears to be a major limitation of ternary logic design based on the T-gate.

J.S. Wang, C. Y. Wu, M. K. Tsai (1988) has developed a ternary logic and its circuit structures implemented by simple ternary gates (STGs), with positive or negative ternary inverters connected to all the input terminals [9]. The parameters of the Half Adder circuit developed by him are:

Voltage Swing	DC power dissipation	Power × Delay
1 0 +1	165.6 µW	1.84 PJ

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R. Mariani, F. Pessolan & R. Saletti has given new approach, the "complete model", to CMOS Multiple Valued (MVL) Ternary Logic[10]. This logic uses standard technology processes and requires only an extra power supply more than binary CMOS circuits. As application of this approach, a general purpose asynchronous circuit is designed with complete model ternary logic elements. The simulation performed by them on this circuit gives the fallowing results & it shows that, it has a larger swing than the STI:

VH = 5 V, VI = 2.5 V and VL = 0 V,
Power supplies VDD = 5 V and VSS = 0,

ΔVIL = 1.36 V, ΔVIH = 1.34 V,
NMH = 0.91 V and NML = 0.98 V.

R.Mariani, R.Roncella, RSaletti & P.Terreni have described the realization of Delay-Insensitive (DI) asynchronous circuits with a CMOS ternary logic. General purpose delay-insensitive circuits are designed with standard ternary logic elements. Using the DI Asynchronous Ternary Logic, adder structures, the Bit-Serial Adder (BSA) and the parallel Ripple-Carry Adder (RCA) are built with ternary logic complex gates. Following table summarizes the design and simulation results in terms of transistor number, average addition time and average energy per operation for 32 bit operands have been used for power consumption evaluation.

Adder	MOS (n.)	Avg. Addition Time(ns)	Avg. Energy per operation (pJ)
BSA	118	147.2	6.28
RCA	1760	33.5	31.6

A multiple-valued multiple-rail encoding scheme for asynchronous data transfer between modules is proposed by Tomohiro Takahashi, Takahiro Hanyu (2004). The use of this multiple rail encoding makes it possible to reduce the dynamic range in a single wire. If signal levels per wire are reduced, the asynchronous data transfer between modules can be performed more efficiently with maintained data-transfer capability.

b) Conventional RT/RT Encoding & Hybrid Ternary Encoding

Eun-Ju Choi, Je-Hoon Lee and Kyoung-Rok Cho (2006) proposed new data encoding methods RT/NRT(Return to Ternary/ Non Return to Ternary) encoding and hybrid ternary one [11]. Conventional ternary encoding makes all data lines to intermediate to generate completion signal.

In RT/NRT encoding, however, data lines with transferring zero do not change to intermediate value in order to reduce the switching activities.

In hybrid ternary encoding, it needs only two half-swing to transfer 2-bit data.

Conventional RT/RT Encoding

D1	1	V1	1	V1	0	V1
D2	0	0	0	0	1	V1
D3	1	V1	0	0	1	V1

RT/NRT Encoding

D1	1	V1	1	V1	0	V1
D2	0	V1	0	V1	1	V1
D3	1	V1	0	V1	1	V1

Hybrid Ternary Encoding

I/P D0 D1	Hybrid ternary
Invalid	ZZ
00	0Z
01	Z1
10	1Z
11	Z0

X. W. Wu & Prof. F.P. Prosser has reviewed the main difficulties and advantages in developing CMOS ternary circuits. They proposed the CMOS ternary circuits using resistors. These CMOS ternary circuits contains passive devices (resistors), which take up too much chip area and increase the power dissipation, output impedance and delay of the circuit. Also, the resistors are difficult to fabricate in a CMOS VLSI circuit. Thus, ternary circuits containing resistors have poor performance as compared with their binary counterparts [12, 13].

IV. MVL for reducing the interconnections

With an increasing density of chips, the number of inter chip connections is greatly increased as more and more functions are put on the same chip; thus, the size and performance of the chip is mostly dominated by wiring rather than devices. One of the most promising approaches to solve the interconnection problems is the use of multiple-valued logic (MVL) inside the VLSI chip. The number of interconnections can be directly reduced with multiple-valued signal representation. The reduced complexity of interconnections makes the chip area and the delay much smaller [14,15].

From the view point of reduction of interconnections, advantages of K-valued logic system in submicron VLSI is chip density. The chip area in submicron VLSI is almost determined by the interconnections. In K valued logic the number of interconnections can be reduced to1 / $\log_2$ K in comparison with binary logic. If this effect can be applied to 2-dimensional geometry, the reduction ratio becomes $1/(\log_2 K)^2$. The total area of interconnections is determined by the number of interconnections and their length. The interconnection length is also determined by the complexity of the interconnections, so that it is clear that the use of MVL is very useful for compact VLSI implementation.

Other advantages of K-valued logic system in submicron VLSI are

- ***Interconnection delay:***

The resistance and capacitance of contacts and interconnecting lines are currently a practical limitation on scaling of minimum geometries. Let the resistance and capacitance per unit length in the interconnections be R and C, respectively. The interconnection delay t is determined by

$t \alpha RCL^2$

where L is the interconnection length. It is well known that the resistance per unit length in interconnections R becomes a factor of S times larger with the geometry scaling factor *S*, while the Capacitance C is almost unchanged. Therefore, it is very important to decrease the interconnection length L in submicron VLSI. MVL makes the complexity of interconnections reduced, so that the total length of interconnections and the interconnection delay can be greatly decreased [2].

- ***Power dissipation:*** In submicron VLSI the dynamic power dissipation is determined mainly by the interconnection capacitance. Therefore, MVL is also useful for low power dissipation.
- ***Noise*:**

Crosstalk noise is a significant problem in submicron VLSI, because the distance between interconnections becomes extremely small. The most direct solution is to make the distance large. This is possible if the density of interconnections is reduced by MVL.

V. Conclusion:

Looking back over the past few decades, much of the older work in multi valued logic is theoretical concerned with its functional algebra. Hence it must be admitted that multiple-valued logic has not displaced conventional binary logic in commercial applications to any significant extent. The development of technology for large-scale system integration & evolution in processing and design methodology has led to an increase in chip density and t o a corresponding increase in complexity. However, there come new limitations caused by interconnection problems.

There is continues research for the development of superior multiple-valued hardware & devices to resolve these limitations. A great wealth of engineering experience available with binary systems, it is difficult to supplant it with higher-valued logic unless very obvious advantages are found.

Nevertheless the subject area of multiple-valued logic is a very necessary one to research, without it no developments to supplement or supplant the binary will occur. The activities of the past few years provide a sound foundation for future work.

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