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Systematic Design of High-Speed and Low-Power Domino Logic

Ms. Rakhi R. Agrawal*
Electronics and Telecommunication
Sipna's college of Engineering and Technology,
Amravati, India
Email:rakhi5788@gmail.com

Dr. S.A.Ladhake
Principal, Sipna's college of Engineering and Technology, Amravati
Amravati, India

Abstract: Dynamic Domino logic circuits are widely used in modern digital VLSI circuits. Because it is simple to implement, low cost designs in CMOS Domino logic are presented. Compared to static CMOS logic, dynamic logic offers good performance. Wide fan-in logic such as domino circuits is used in high-performance applications. Domino gates typically consume higher dynamic switching and leakage power and display weaker noise immunity as compared to static CMOS gates. This paper compares static CMOS, domino logic design implementations. For the comparison of static CMOS and DOMINO logic we will see various design of Domino logic gates and as well as design of logic circuits using Domino logic gates.

Keywords – Dynamic; Domino; CMOS; Very Deep submicron technology; High speed; Low Power.

I. INTRODUCTION

Dynamic circuits are widely used in custom circuit design to achieve higher speed, smaller area and potentially lower power consumption due to glitch-free operation. There are also difficulties in designing and verifying this class of circuits. However, Domino logic circuits can implement only non-inverting logic; the synthesis of a Domino logic circuit typically involves the conversion to a unate representation from the original binate logic network. Synthesis of domino circuits is more complicated than that of static circuits. The added complexity is due to domino logic's monotonic nature which forces it to implement only non-inverting functions. Therefore, domino logic can only be mapped to a network of non-inverting functions, where needed logic inversions must be performed at either primary inputs and/or primary outputs. Dynamic logic is over twice as fast as normal logic; it uses only fast N transistors. Static logic is slower because it uses slow P transistors to compute logic. Dynamic logic is harder to work, but if we need the speed there is no other choice. There are also difficulties in designing and verifying this class of circuits. Dynamic circuitry can become highly sensitive to clock skew, charge sharing etc. Domino logic has created a substantial interest due to its performance and CMOS power consumption. It runs 1.5-2 times faster than static CMOS logic because dynamic gates present much lower input capacitance for the same output current and a lower switching threshold.

II. CONCEPT OF DOMINO LOGIC

Dynamic logic requires two phases, the first phase is set up phase or pre charge phase, in this phase the output is unconditionally go to high (no matter the values of the inputs A and B). The capacitor which represents the load capacitance of this gate becomes charged. During the evaluation phase, CLK is high. Popular implementation of dynamic logic is domino logic. Domino logic is a CMOS based evaluation of the dynamic logic techniques which are based on the either PMOS or NMOS transistors. It was developed to speed up the circuits. The dynamic gate outputs connect to one inverter, in domino logic. In domino logic, cascade structure consisting of several stages, the evaluation of each stage ripples the next stage evaluation, similar to a domino falling one after the other. Once fallen, the node states cannot return to "1" (until the next clk cycle), just as dominos, once fallen, cannot stand up. The structure is hence called domino CMOS logic.

Domino logic is the most popular dynamic logic. It runs 1.5-2 times faster than static CMOS logic because dynamic gates present much lower input capacitance for the same output current and a lower switching threshold. Domino circuits are in function very similar to the

clocked CMOS circuit. In Domino logic a single clock is used to precharge and evaluate a cascaded set of dynamic logic blocks. This circuitry incorporates a static CMOS buffer into each logic gate as shown in Figure 1. During the precharge phase (CK=0) all output nodes all (N') of the dynamic gates are precharged to high, through the transistor MP, and thus the outputs (N) of the corresponding buffers are precharged to low. Since all transistors of subsequent dynamic gates are fed from such buffers, these will be turned off during the precharge phase.

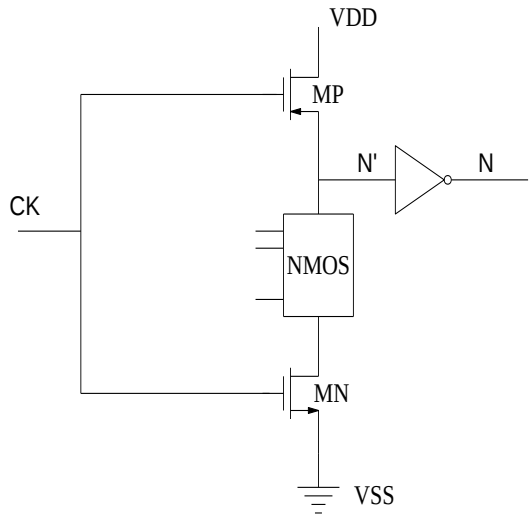


FIGURE 1. A DOMINO LOGIC CIRCUIT.

Next, during the evaluation phase, nodes N' are either discharged through transistor MN or they remain high, according to the realized function. Thus the outputs N of the buffers either go to high or remain low, respectively. It should be noted that in Domino logic the transition of nodes N is always from low to high and it is rippled through the logic from the primary inputs lo the primary outputs. Since there are cascaded logic blocks, the evaluation of a stage causes the next stage to evaluate arid so on. Obviously, any number of logic stages may be cascaded, provided that they can be evaluated within the evaluate phase of the clock. In this paper Domino logic design is used for better performance with a smaller number of transistors. In a novel Domino logic design precharged by clock and data has been proposed that also presents high performance and reduced area requirements.

III. PROPOSED WORK

To design VLSI implementation of domino logic circuits we first led down the target parameters from required specification. And also studied each and every aspect of target parameters and as well as their dependency. We analyze the earlier documents / papers for better design guidelines. We select two-three fix topology for initial trials simulation and comparing these initial results with expected target specification and after taking final decision on topology we go for full custom design. We design various Domino logic gates and as well as design of logic circuits using Domino logic gates.

Here, for the comparison we are going to design the CMOS basic gates. In this work, we tried to show a design methodology to design domino logic circuits; as well as experimental results validating this methodology. After designing each block of the gates of CMOS and DOMINO we will show the comparison between the CMOS and DOMINO technologies and try to distinguish that how the DOMINO logic circuits designs are low power and high speed than CMOS designs.

IV.RELATED WORK

Dynamic logic (or sometimes clocked logic) is a design methodology in combinatorial logic circuits, particularly those implemented in MOS technology. Dynamic logic, when properly designed, can be over twice as fast as static logic. It uses only the faster N transistors, which improve transistor sizing optimizations. Static logic is slower because it has twice the capacitive loading, higher thresholds, and uses slow P transistors for logic. Dynamic logic can be harder to work with, but it may be the only choice when increased processing speed is needed. The operating period of the cell when its input clock and output are low is called the precharge phase or cycle. The next phase, when the clock is high, is called the evaluate phase or cycle.

INVERTER

First, we will see the basic circuit of CMOS Inverter (logic gate), a logic gate also called a NOT gate. The truth table is shown below (TABLE: 1).

TABLE: 1

INPUT A	OUTPUT NOT A
0	1
1	0

Figure 2 shows the Inverter of CMOS logic which is using one PMOS transistor and one NMOS transistor. In this when the input A is '0', the NMOS transistor is OFF and PMOS transistor is ON. Thus the output is pulled up to '1' because it is connected to V_{DD} but not to GND. Conversely, when A is '1', the NMOS transistor is ON,the PMOS is OFF and the output is pulled down to '0'. This is summarized in the truth table. Where Figure 3 shows the Inverter of DOMINO logic, it is same as the

CMOS. But it also using one PMOS transistor and one NMOS transistor as well as it consists of clock as mentioned before that it is a clocked logic. The simulation results of both the CMOS and DOMINO designs are shown below in Figure 4 & 5 respectively. This results can be checked with the help of the truth table of the inverter. From the result it is directly compared that DOMINO design is very low power technology. As the current is near 350 µA and 100 µA of CMOS and DOMINO technologies respectively.

INVERTER

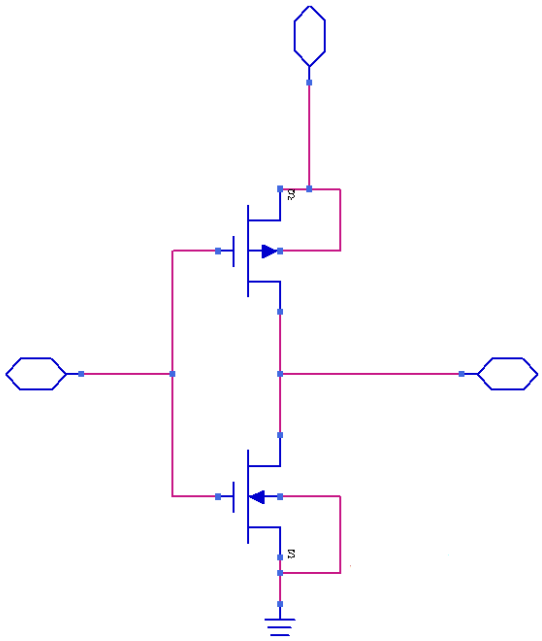


FIGURE 2

DOMINO INVERTER

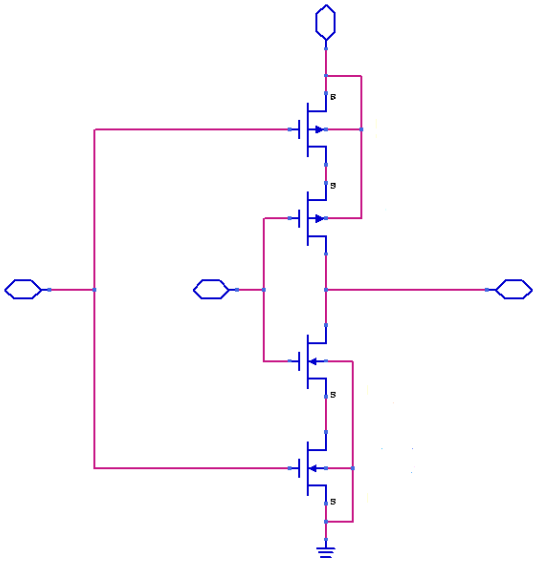


FIGURE 3

SIMULATION RESULTS

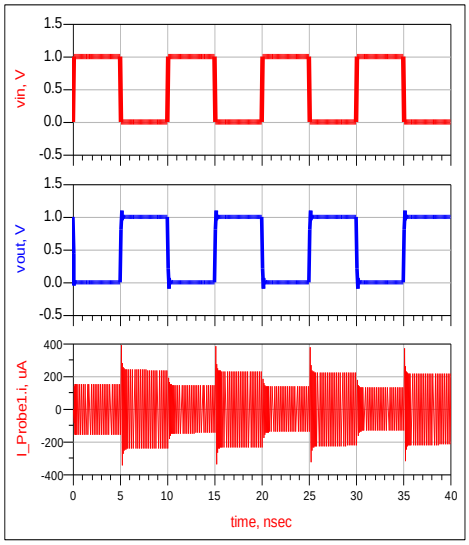


FIGURE 4

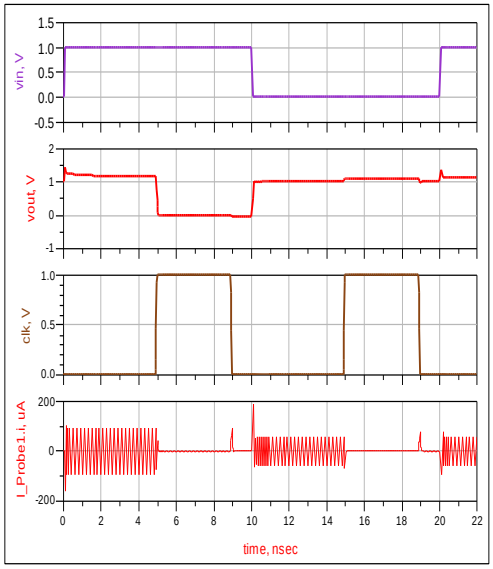


FIGURE 5

AND

The AND gate is an electronic circuit that gives a high output (1) only if all its inputs are high. A dot (.) is used to show the AND operation i.e. A.B. Bear in mind that this dot is sometimes omitted i.e. AB. Here is the truth table of AND gate (TABLE: 2).

2 Input AND gate		
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

TABLE: 2

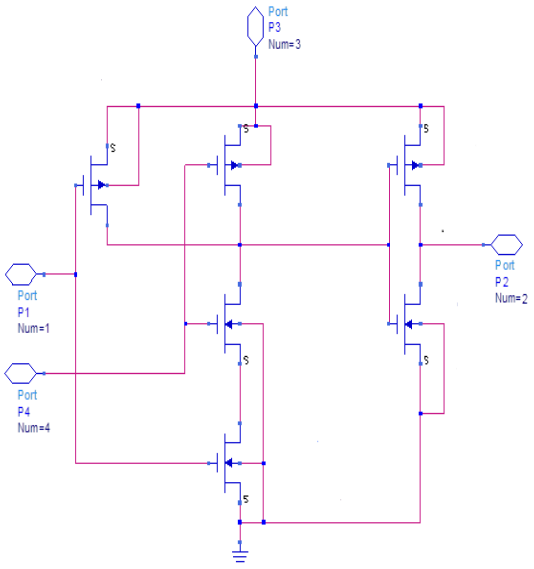


FIGURE 6

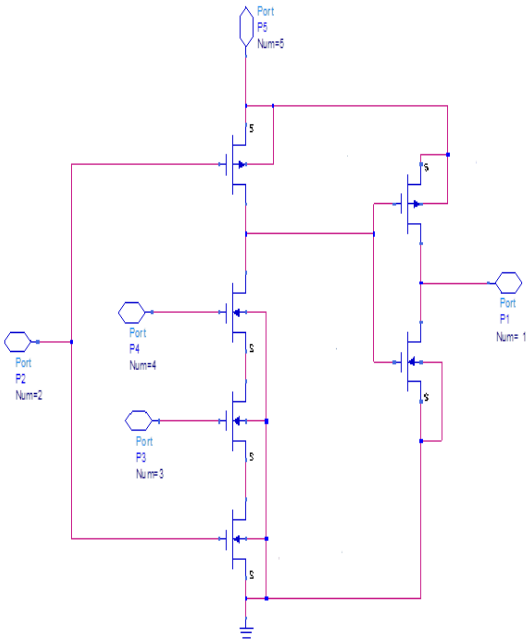


FIGURE 7

SIMULATION RESULTS

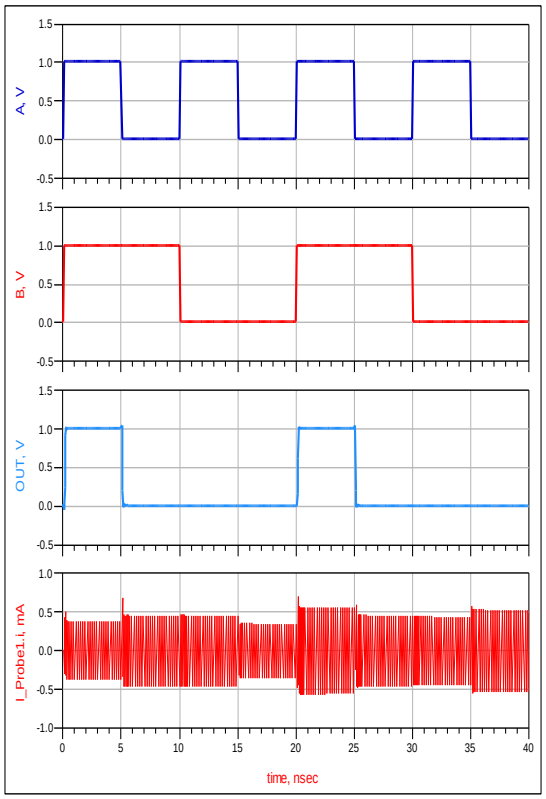


FIGURE 8

As figure 6 and figure 7 showing the circuit diagram of AND gate. And figure 8 and figure 9 shows the simulation results of CMOS AND gate and DOMINO AND gate respectively. From the simulation results itself shows that domino logic circuits are low power and having high speed than that of the basic CMOS logic technology. Here the figure 8 which is the result of basic CMOS logic AND gate having the current in 0.5mili-ampere (mA) and figure 9 which is the result of domino logic having the current in 0.5micro-ampere (µA). This results you can verify with the given truth table of AND gate (TABLE : 2) .

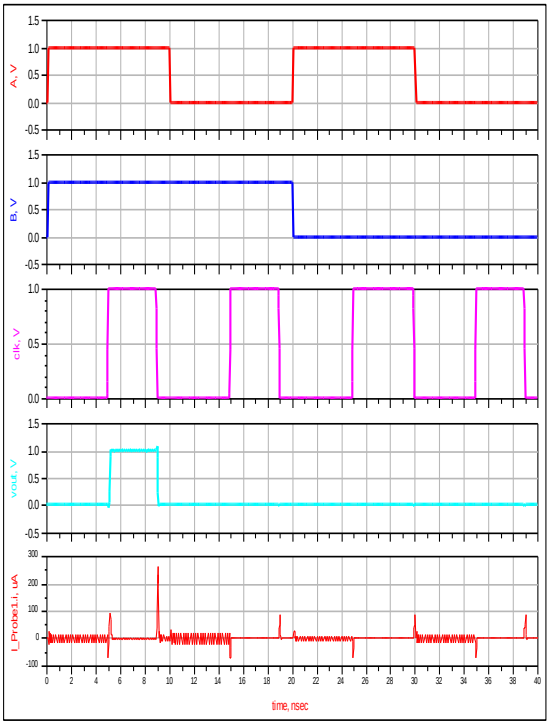
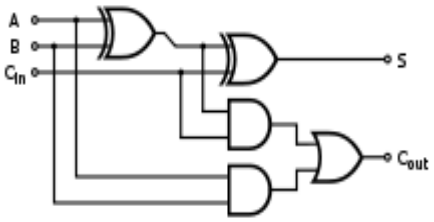


FIGURE 9

FULL ADDER

Full-adder is a digital circuit to perform arithmetic sum of two bits and a previous carry. It is represented in the diagram below. The circuit involves two half-adders & one gate. Alternately 2 XOR gates, 2 AND gates and 1 OR gate.



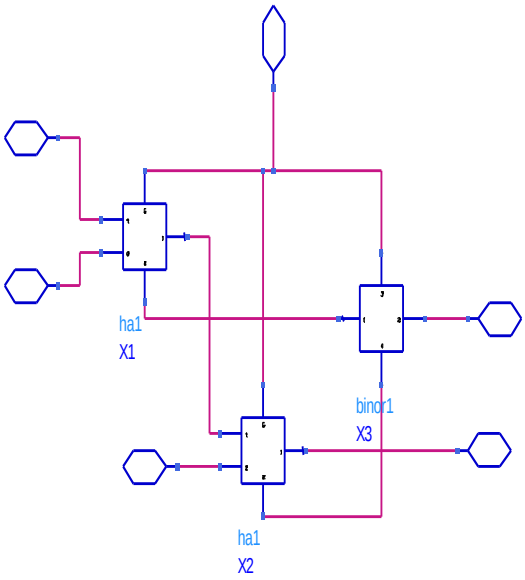


FIGURE 10 : 1-bit Full Adder

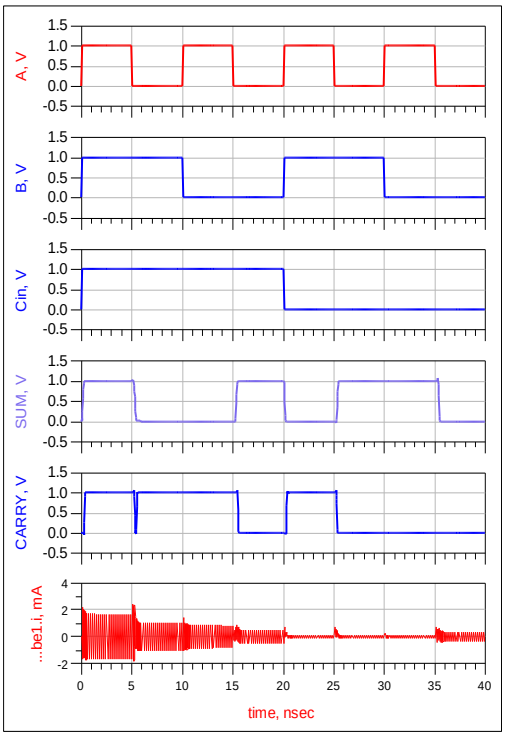


FIGURE 11

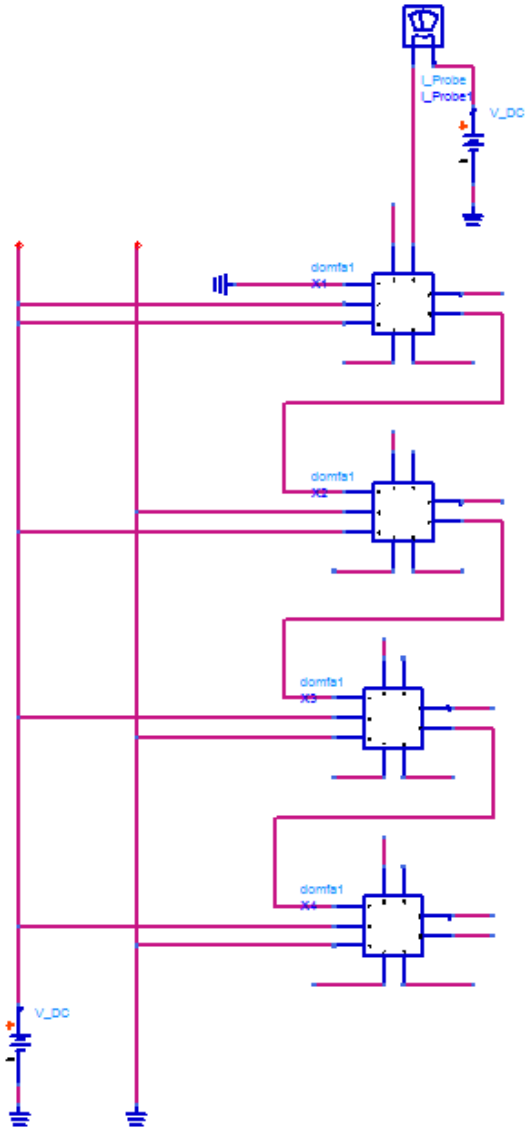


FIGURE 12 : 4-bit Full Adder

For making Full Adder circuit, first we have designed half adder in both the technologies. For designing the half adder we also needed AND, XOR gate too that's why we have designed all the basic gates for both the technologies. Figure 10 and Figure 12 shows 1-bit full adder in CMOS and 4-bit full adder in DOMINO technologies respectively. And their simulation results are shown in Figure 11 and 13 respectively. From these we can conclude that if 1 bit full adder of CMOS technology gives 2mili-ampere and in DOMINO technology gives 1mili-ampere for 4-bit full adder. In that case we can say that 4-bit full adder in CMOS technology will increase four to five times power than that of DOMINO technology.

DOMINO 4-BIT FULL ADDER

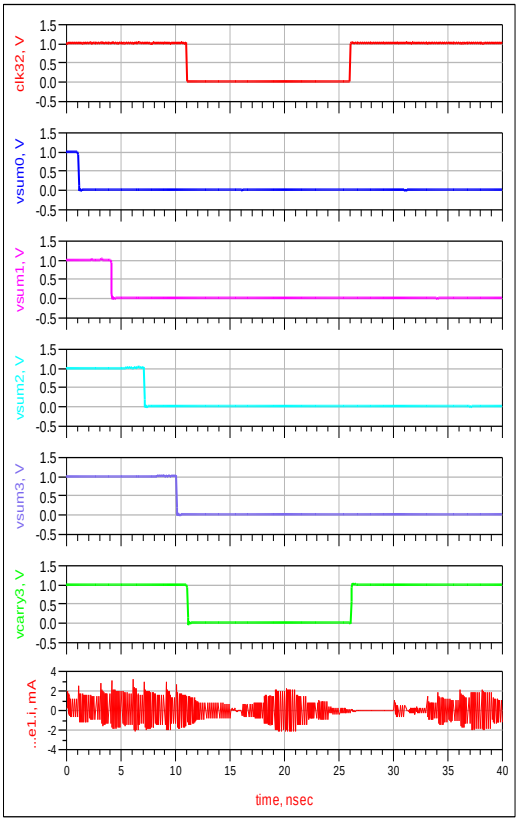


FIGURE 13

From these results we can conclude that DOMINO technology is more efficient and very low power with having high speed that any other technology. Thus we can say Domino circuits have offered an improved performance in speed and power when compared with CMOS circuit. As it is observed from the results that Domino circuits offer better solution for the low power and high speed than CMOS circuits.

V.CONCLUSION

This paper has presented a design methodology for Domino logic circuits. Domino logic circuits have become extremely popular in the design of today's high performance processors because they offer fast switching speeds and reduced areas. In this paper, comparison of CMOS Logic circuits and DOMINO Logic circuits of various design of Domino logic gates and as well as design of logic circuits using Domino logic gates have been explored. In this work, an attempt has been made to simulate AND gate, Full adder by using the proposed techniques. Domino circuits have offered an improved performance in speed and power when compared with CMOS circuit. As it is observed from the results that Domino circuits offer better solution for the low power and high speed than CMOS circuits. Hence, it is concluded that the proposed design of DOMINO Logic will provide a platform for designing high performance and low power digital circuits.

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