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Silicon on Insulator MOSFET Development from Single Gate to Multiple Gate

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Abstract- This paper describe the developments in SOI MOSFET with single gate, double gate, triple gate as well as gate all around structures. The bulk Si MOSFET has been the main device forming the backbone of the development of ultra high density ICs. In order to reduce parasitic capacitances Silicon-on-insulator (SOI) technology used.. The double-gate (top and bottom gate) silicon-on-insulator (SOI) MOSFET and the gate-all-around (GAA) device are the most suitable device structures for suppressing short-channel effects such as drain-induced barrier lowering (DIBL) and sub threshold slope degradation. The nano MOSFETs are the requirement of nano electronics .The gate all around MOSFET used in silicon Nano wires.

KEY WORDS:MOSFET, SOI, DIBL

I. INTRODUCTION

In the traditional MOSFETs as scaling comes down the performance of device degrades. MOSFET scaling continues to take transistors to smaller and smaller dimensions while advances in nanoscience provide fascinating possibilities for new electronic technologies. To increase the performance of the device SOI (Silicon on Insulator) technology developed . The first SOI transistor developed in year 1964. These were partially depleted devices fabricated SOS (Silicon on Sapphire) substrate. SOS technology was successfully used for numerous military and civilian applications [2] and is still being used to realize commercial HF circuits in fully depleted CMOS [3–5]. The substrate is replaced by silicon di oxide . IC manufacturers attracted towards SOI technology used in memory chips and microprocessors .Variations on the partially depleted SOI MOSFET theme include devices where the gate is connected to the floating body. These devices, which have been called' voltage-controlled bipolar-MOS device'' [6], ''hybrid bipolar-MOS device'' [7,8], ''gate-controlled lateral BJT''[9], ''multiple-threshold CMOS'' [10], ''dynamic threshold MOS'' [11], or ''variable-threshold MOS'' [12] have ideal sub threshold characteristics, reduced body effect, improved current drive, and superior HF characteristics FULLY-depleted (FD) SOI MOSFETs are very attractive for sub-100 nm CMOS applications because of their steep sub threshold slope and a low body effect coefficient. SOI microprocessors with a 22% speed improvement over bulk have been reported recently [1]. FDSOI MOSFETs with a gate length of 50 nm and a switching speed less than a picosecond's [2] have been reported. To minimize short channel effects and to maintain full depletion if the doping concentration in the channel region is increased, the silicon film thickness must be scaled down with gate length. While devices made in films thicker than 20 nm have excellent mobility and current drive characteristics [2], If a metal gate is used instead of N polysilicon the doping concentration in the film can be reduced, while allows for fully depleted operation in thicker silicon films. This decrease of doping concentration, however, degrades the short channel characteristics and sub threshold slope through an increase of penetration of the drain electric field lines in the channel region [4], [5]. To avoid the electric field lines started at the drain from terminating under the channel region, special multiple-gate structure devices have been reported. Such multiple-gate devices include double-gate and triple-gate structures such as the quantum wire [6], the FinFET [7] and -channel SOI MOSFET [8], and quadruple-gate devices such as the gate all-around (GAA) device [9], the DELTA transistor [10], vertical pillar MOSFETs [11], and Pi-gate SOI MOSFETs [12]. It is well known that the double-gate (top and bottom gate) silicon-on-insulator (SOI) MOSFET and the gate-all-around device are the most suitable device structures for suppressing short-channel effects such asDIBL and sub threshold slope degradation [9], [13], [14].

II. DOUBLE GATE SOI MOSFET

Figure 1. Shows the basics model of double gate SOI MOSFET, Double-gate *SOI MOSFET* has two gates simultaneously controlling the charge in the thin silicon body layer, allowing for two channels for current flow. Because *SOI* film is thin, a direct charge coupling exists between the front and back gate invariably [6], influencing the terminal

characteristics of the device. The device can be operated in several ways [7]:

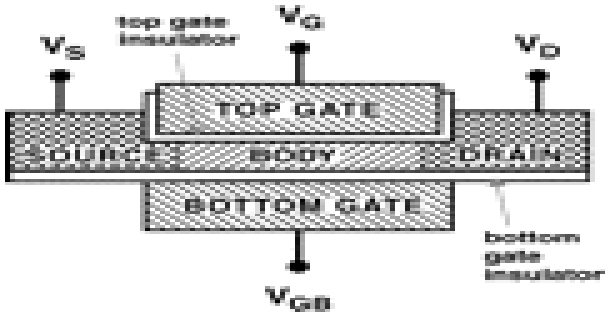

Fig. 1 Basics model of double gate

Front channel alone conducting, the back channel being either depleted or accumulated. (A) Both channels conducting .(B) both or either of the channels being in weak or strong inversion. The current-voltage characteristics of the device with the front channel in strong inversion and the back channel either in accumulation or in depletion has been modeled analytically. Since *SOI* films are thin, the electrical properties of *MOSFETs* fabricated are inherently influenced by the charge coupling between the front and back gates. Due to extremely small device dimensions, low voltage operation will be mandatory where the low threshold voltage is required [32]. Sasaki and Togei [33] studied the variations in the threshold voltage of *SOS* (silicon on sapphire) *MOSFET* as a function of epitaxial film thickness. Worly derived an analytical model for the threshold voltage of an *SOS* transistor in which charge coupling between the front and the back gates occurs as in *SOI MOSFET*, but only the back silicon surface is depleted. Sano et. al. [35] developed a rigorous numerical model for threshold voltage *(Vth)* that includes a dependence on the back gate bias. Wei Ma and Savas Kaya measured the impact of device physics on double-gate, silicon-on-insulator and bulk metal oxide field effect transistor as shown in figure 1.11, in terms of drain current, transconductance and output conductance. It was observed that:

• Drain current, so as the transconductance is high in case of *DG* as compared to *SOI* and bulk *MOSFET*, as shown in figure 1.11 (a) - (b). Also gd reduces more rapidly in *SOI* and *DG MOSFETs*, which have a thinner active *Si* layer, hence a lower output conductance. For Vds > 0.5 V, gd remains relatively flat in *SOI MOSFET*, while *DG* and bulk *MOSFETs* have comparable response, except lower value of gd in the former case, as shown in figure 1.11 (c).

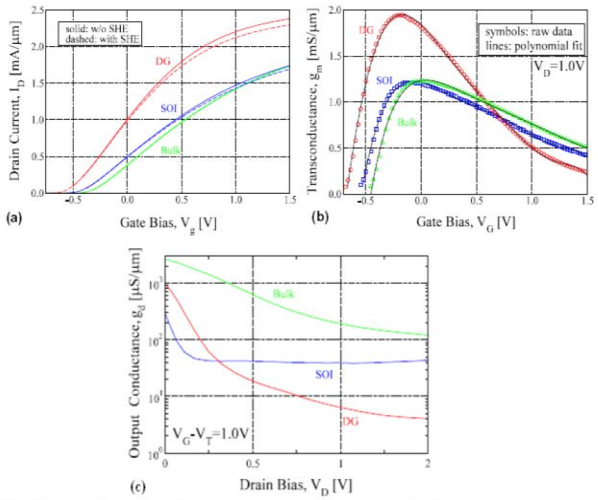

Fig 1.11 (a) I_d–V_g characteristics (b) Corresponding transconductance curves for the same devices (g_m) (c) Drain-bias dependence of g_d is typically low in saturation but non-zero. Source: Wei Ma and Savas Kaya [64]

It was observed that the *DG* transistor shows the best *SCE* control and performance. Some of the performance outcomes are given below:

• *DG* transistors exhibit the best electrical results in terms of *SCEs* and saturation

Currents for both *nMOS* and *pMOS* transistors, as shown in figure 1.12.

• *DG* devices exhibit a low symmetrical threshold voltage Vth adjusted to 0.45 V.

Conversely, the *GP* architecture shows a very high threshold voltage due to the

influence of the grounded back gate, as shown in figure 1.13.

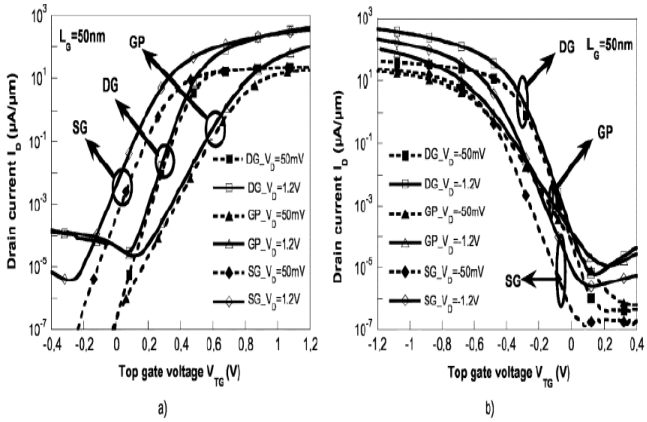

Fig. 1.12 Drain current versus gate voltage for SG, DG, and GP (Ground Plane) transistors with a gate length of 50 nm for both (a) nMOSFETs and (b) pMOSFETs. Source: Julie Widiez et. al.[65]

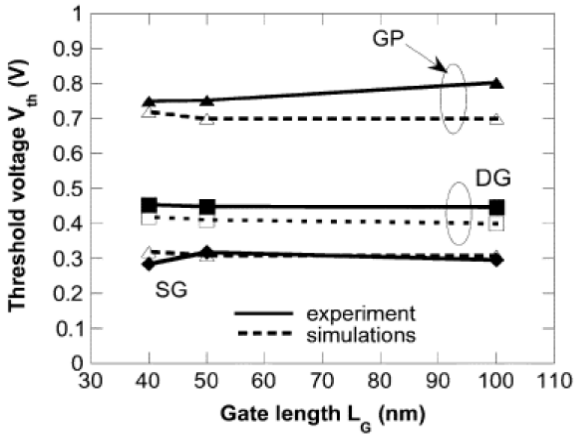

Fig. 1.13 Threshold voltage as a function of the gate length at V_{ds} = 50 mV for nMOS devices. Dashed lines are simulations. Source: Julie Widiez et. al.[65]

III. TRI-GATE SOI MOSFET

The tri gate transistor is ideal for use in fully depleted transistor applications. The tri gate MOSFET include a thin semiconductor body formed on an substrate. A gate dielectric formed on top surface and side wall of semiconductor body. A gate dielectrode is formed on dielectric on the top surface of semiconductor body and the sidewalls of semiconductor body. Source and drain regions formed on semiconductor body on opposite side of gate electrode .Because the gate electrode and gate dielectric surround the semiconductor body on three sides ,the transistor essentially has three separate channel and gate .The gate width of a transistor is equal to sum of each of the three sides of semiconductor body. Figure 2(a) and (b) shows the model tri gate transistor.

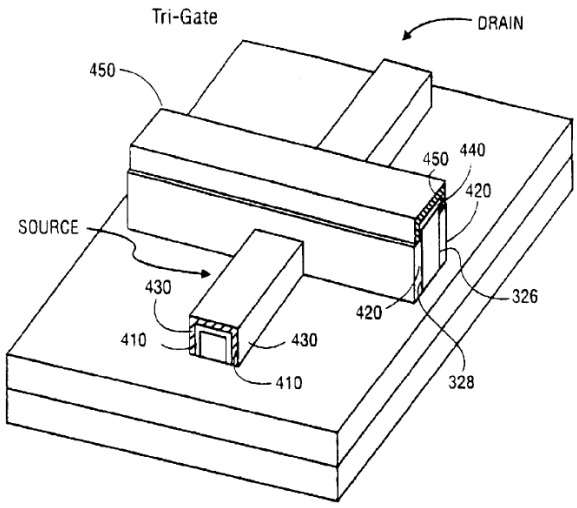

Figure 2.(a)

In the case of single-gate FDSOI devices, the silicon body thickness (tsi) needs to be about a third to a half of the electrical gate length in order to maintain full substrate depletion under gate control ([8], [9]).Scaling this device to 30 nm gate length dimensions, for example, requires a 3-thickness uniformity of 1 nm on a silicon film thickness of 10 nm, which is presently hard to achieve. For non-planar double-gate FinFET devices, the transistor structure most often considered for future scaled transistors [10], the thickness requirement for the silicon between the two gates is relaxed to approximately the electrical gate length, or two-thirds the physical gate length since each gate controls half the body thickness [11]. The experimental results of tri-gate CMOS transistors with 60 nm physical gate lengths (Lg). Lg=60 nm was chosen because the technology is mature enough to make a valid comparison with bulk devices at gate lengths significantly shorter than 60 nm, research devices are unoptimized, and it becomes difficult to compare the benefits offered by various transistor architectures. We find that these devices show the highest ever reported performance for non-planar MOS devices or both n- and p-channel transistors for scaled threshold voltages . We find also that tri-gates are competitive with a similarly-scaled, aggressive bulk CMOS technology at the same technology node.

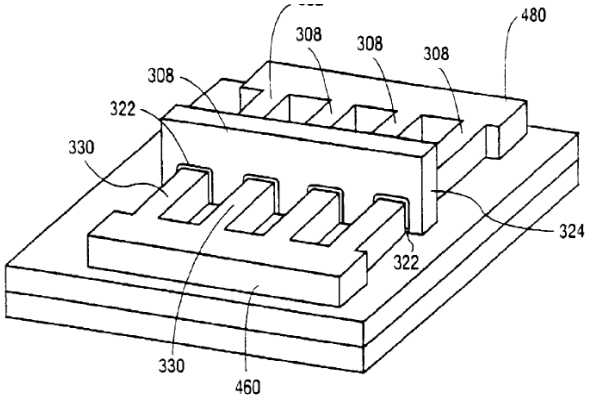

Figure 2(b) completed tri gate MOSFET.

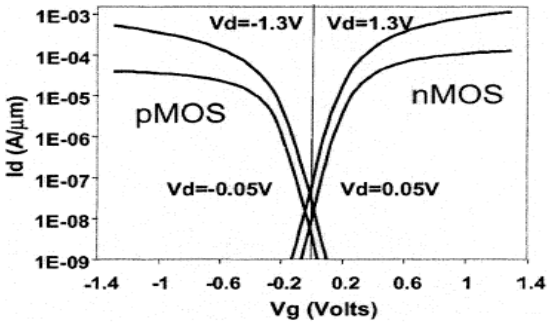

Figure 3. I –V characteristics of 60 nm gate length NMOS and PMOS transistors. The current I is normalized to the width (Z) in all cases.

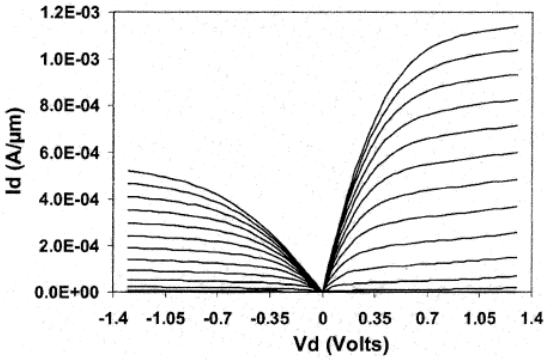

Figure 4. The gate voltage was ramped to 1.3 V in increments of 0.1 V.

IV .CONCLUSION

The SOI MOFET s are now days used in nano electronics . In the development of nano wire the gate all around are cyndrical structure used . MULTIGATE Si-based devices such as trigate or gate-all-around (GAA) Nanowire (NW) MOSFETs are promising candidates for aggressively scaled CMOS due to their excellent electrostatics, low power consumption, and immunity to short channel effects

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