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Low Power Level-Up Shifter for Reduction of Static Power Dissipation in CMOS Technology

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***Abstract*—Static power dissipation is increases with the scaling in threshold voltage and expected to become important part of total power consumption. In the present work, a new configuration of level shifters for low power application in 0.25µm technology has been presented. The proposed circuits utilize the merit of stacking technique by which there is reduction in leakage power. In this work a new level-up shifter designed at ultra low core voltage and has wide range of I/O voltage. The circuit is designed using 0.25µm CMOS process. Proposed level shifter uses stacking technique to reduce static power dissipation with a little addition in area. Less static power dissipation allow level shifter suitability for wide I/O interface voltage applications in CMOS Technology with very little power dissipation.**

***Keywords*—CMOS, Static Power Dissipation, Level Shifter Threshold voltage, Ultra Low Core Voltage and Stacking Technique.**

1. INTRODUCTION

As demand of handheld device like cellular phones, multimedia devices etc. are increasing and we are approaching towards portable device having small size which requires large battery life. But power dissipation has become most important design concern for VLSI circuits and system in low power devices [2],[3]. With increase in power consumption, reliability problem also rises and cost of packaging goes high [7]. Transistor dimension should be scaled down to achieve high performance and density. But power dissipation is also altered by this scaling. Power dissipation in VLSI circuit consists of dynamic and static power dissipation. Dynamic power has two components i.e. switching power due to the charging and discharging of the load capacitance and this is due to on and off of transistor. The static power of CMOS circuits is determined by the leakage current when the input voltage is less than threshold voltage and transistor is off state (standby mode) but there is leakage of current from drain to ground Power that should be minimized. Power Conumption of VLSI circuits can be reduced by scaling supply voltage and capacitance [8]. But with the reduction in supply voltage, problems of small voltage swing, insufficient noise margin and leakage currents originate [9]. With the development of technology leakage power has become significant component of total power dissipation [10], [11]. Most of the given power is consumed during operation in the form of leakage. This is surely a big obstacle in integration process. So leakage power component must be given due concern if present trends of scaling to be achieve.

2. CONVENTIONAL LEVEL SHIFTER

Level shifter is an interfacing circuit which can interface low core voltage to high input-output voltage. The level shifter allows communication between different modules without adding up any extra supply pin. The conventional level shifter using cross-coupled PMOS load is shown in Fig.1 (a).Thick gate oxide transistor was used for N11, N12, P11 and P12 to overcome high voltage stress. cross-coupled P11, and P12 provides positive feedback action which result in fully VDD2 voltage at output node, means by using level shifter we can interface two blocks having different voltages. The conventional level shifters have drawback of delay variation due to different current driving capabilities of transistors, large power dissipation and failure at low supply core voltage [5].A very important phenomena in integration process is sub threshold current. Sub threshold current is the drain-source current when the gate-source voltage is under the transistor threshold voltage.MOS transistor models predict that when gate-source voltage is at or below the threshold voltage the transistor does not conduct and there should be is no current flow ideally but practically there is

leakage of current i.e. static power leakage from drain to ground i.e. wastage of power. This leakage is continuous and we cannot avoid it but by using suitable leakage minimizing circuit we can minimize this. Circuit diagram of conventional level shifter is shown in fig 1(a). If we have LOGIC 0 at input terminal then N11 and P12 are in saturation region and P11 and N12 Are in cut-off region. This will cause vdd2 at output node so by using level shifter we can interface low core voltage to high output voltage, but during this operation the static power dissipation (leakage) is occurring in N12 and P11 i.e. there is continuous flow of current from vdd2 to ground. We should adopt a technology to reduce this leakage. For this we have different technology like power gating, MTCMOS, stacking technique etc. by using different technique we can mitigate that static power dissipation.

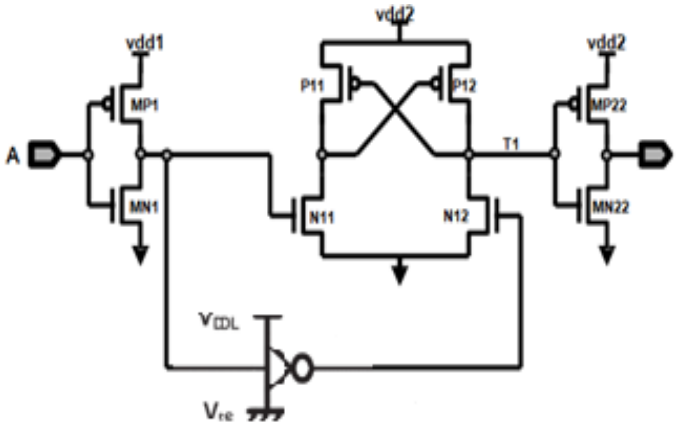

Fig 1(a) conventional level shifter

FOR PMOS –	FOR NMOS –
M=1	M=1
L=0.25 µm	L=0.25µm
W=2.5 µm	W=2.5 µm

Where, M=model no.
W=width of channel; L=length of channel

TABLE I
Observational table of conventional level shifter

vdd1 (VOLTS)	ST-LEAK 1 (pA)	ST-LEAK 2 (pA)	P(ST-LEAK1) (pW)	P(ST-LEAK2) (pW)	TOTAL POWER LEAK(pW)
2.5	10.2	30.6	25.5	76.5	102
2.6	10.5	30.6	27.3	79.56	106.86
2.7	11.2	30.6	30.24	82.62	112.86
2.8	11.4	30.6	31.92	85.68	117.6
2.9	12	30.6	34.8	88.74	123.54
3	12.3	30.6	36.9	91.8	128.7
3.1	12.5	30.6	38.75	94.86	133.61
3.2	12.8	30.6	40.96	97.92	138.88
3.3	13.4	30.6	44.22	100.98	145.2
3.4	13.7	30.6	46.58	104.04	150.62
3.5	14.2	30.6	49.7	107.1	156.8
3.6	14.5	30.6	52.2	110.16	162.36
3.7	15	30.6	55.5	113.22	168.72
3.8	15.5	30.6	58.9	116.28	175.18
3.9	15.8	30.6	61.62	119.34	180.96
4	16.2	30.6	64.8	122.4	187.2
				Total	2291.09
				Average	143.193125

Where
ST-LEAK1 – Static current leakage due to vdd1 (Pico ampere)
ST-LEAK2 – Static current leakage due to vdd1 (Pico ampere)
P(ST-LEAK2) – Static power leakage due to vdd1 (Pico watt)
P(ST-LEAK2) – Static power leakage due to vdd1 (Pico watt)

4. PROPOSED LEVEL SHIFTER

A similar and more practical technique for static power dissipation is stack effect. The term stack effect refers to the reduction of sub threshold leakage by stacking multiple FETs in series. The last device in the stack essentially appears as impedance to any leakage current, so the voltage at drain of last FET becomes non-zero.

$$V_T = V_{t0} + Y(\sqrt{VsB + 2\phi F} - \sqrt{2\phi F} \quad (2)$$

Vsb =Base-source voltage
ϕF =Work function

So by above equation [1] we can say that VsB reduces and it reduces threshold voltage, and hence reduces static power dissipation. Fig 2(a) shows stacking technique. And fig 2(b) shows modified level shifter with stacking technique by which NMOS having width W is replace by two transistor having width W/2.

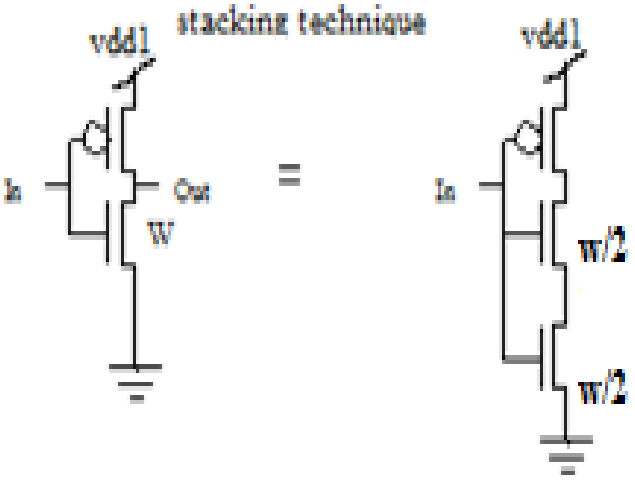

Figure 2(a) Stacking Technique

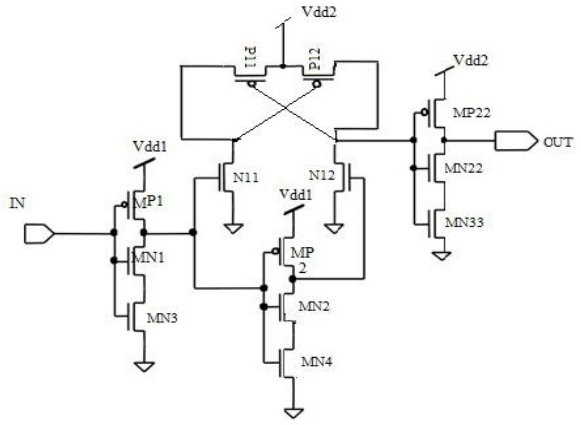

Fig 2(b) Proposed level shifter

FOR PMOS –	FOR NMOS –
M=1	M=1
W=2.5 µm	W=2.5 µm
L=0.125 µm	L=0.125µm

Where
M=model no.
W=width of channel
L=length of channel

TABLE II

Observational table of proposed level shifter (using stacking technique)

vdd1	P(ST-LEAK1) (pW)	ST-LEAK2 (pA)	P(ST-LEAK2) (pW)	P(ST-LEAK2) (pW)	TOTAL POWER LEAK (pW)
2.5	9.4	29.3	23.5	73.25	96.75
2.6	9.8	29.3	25.48	76.18	101.66
2.7	10.1	29.3	27.27	79.11	106.38
2.8	10.5	29.3	29.4	82.04	111.44
2.9	10.9	29.3	31.61	84.97	116.58
3	11.2	29.3	33.6	87.9	121.5
3.1	11.6	29.3	35.96	90.83	126.79
3.2	12	29.3	38.4	93.76	132.16
3.3	12.3	29.3	40.59	96.69	137.28
3.4	12.8	29.3	43.52	99.62	143.14
3.5	13.2	29.3	46.2	102.55	148.75
3.6	13.5	29.3	48.6	105.48	154.08
3.7	13.9	29.3	51.43	108.41	159.84
3.8	14.3	29.3	54.34	111.34	165.68
3.9	14.8	29.3	57.72	114.27	171.99
4	15	29.3	60	117.2	177.2
				TOTAL	2171.22
				AVERAGE	135.70125

By fig 2(c) we observe that as we apply stacking technique there is mitigation in static power dissipation.

6. Comparison graph

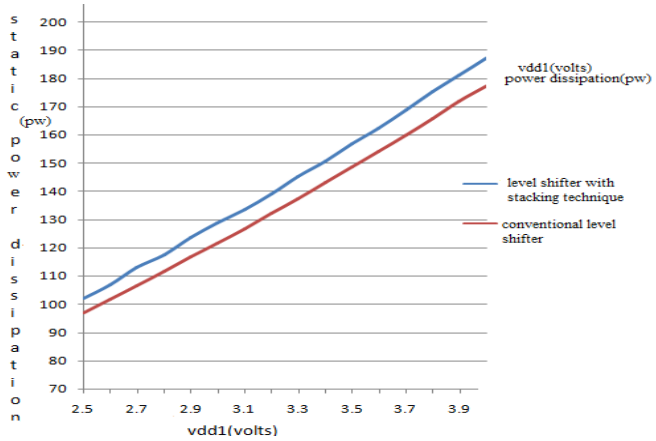

Fig 2(c) comparison between conventional level shifter and proposed level shifter

7. CONCLUSION

In present paper new circuits of level shifters is presented which shows improvement in static power dissipation. Proposed level shifter gives power consumption of 143.193 pw (average) in comparison of conventional level shifter which has static power dissipation i.e.135.193 pw (average). So we have conclude that by using stacking technique we can reduce static power dissipation by a 9.44% and it has been observed that with little increment in Area, power consumption has reduced considerably.

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