



www.ijarcsse.com

Volume 2, Issue 4, April 2012

ISSN: 2277 128X

International Journal of Advanced Research in Computer Science and Software Engineering

Research Paper

Available online at: www.ijarcsse.com

Implementation of MB-OFDM Transmitter Baseband Using FPGA Approach For High Speed Application

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Abstract-An enhancement to the FDM system, as MB-OFDM, has been proposed to reduce the complexity and power consumption without sacrificing performance. In this paper, we presented the detailed FPGA implementation of a complete-OFDM transmitter. The entire transmitter can be mapped onto a single FPGA chip. Multi-Band Orthogonal Frequency Division Multiplexing (MB-OFDM) is a suitable solution to implementation of high speed data transmission in ultra wideband spectrum by dividing the spectrum available into multiple bands. The baseband of transmitter is one of the most important parts in MB-OFDM system. The structure of MB-OFDM system transmitter is introduced in this paper and the design of transmitter baseband based on FPGA is described in detail. The design has been validated with Xilinx Vertex FPGA. The results show that all modules designed has achieved the expected purpose both in precision and resource, with simplicity and high efficiency and can meet the demand of MB-OFDM systems. The baseband of transmitter is one of the most important parts in MB-OFDM system. The structure of MB-OFDM system transmitter is introduced in this and the design of transmitter baseband based on FPGA is described in detail. Multi-Band Orthogonal Frequency Division Multiplexing (MB-OFDM) is a suitable solution to implementation of high speed data transmission in ultra wideband spectrum by dividing the spectrum available into multiple bands. The design has been validated with Xilinx Virtex or Altera FPGA. The results show that all modules designed has achieved the expected purpose both in precision and resource, with simplicity and high efficiency and can meet the demand of MB-OFDM systems.

Keywords: FPGA, High data rate, MB-OFDM, Wireless network.

I-INTRODUCTION

In early period or years, UWB communication systems have received significant attention from both the industry and the academia. In February 2002, the Federal Communications Commission (FCC) allocated 7,500 MHz of spectrum (from 3.1 GHz to 10.6 GHz) for use by UWB devices [1][2]. This ruling has helped to create new standardization efforts, like IEEE 802.15.3a [3], that focus on developing high speed wireless communication systems for personal area network. Orthogonal Frequency Division Multiplexing (MB-OFDM) is a suitable solution to implementation of high speed data transmission in ultra wideband spectrum by dividing the spectrum available into multiple bands. The baseband of transmitter is one of the most important parts in MB-OFDM system. The structure of MB-OFDM system transmitter is introduced in this paper and the design of transmitter baseband based on FPGA is described in detail. The design has been validated with Xilinx Vertex FPGA. A multi-band orthogonal frequency division multiplexing (MB-OFDM) ultra wideband (UWB) system is being considered for the physical layer of the new IEEE wireless personal area network (WPAN) standard, IEEE 802.153a [3]. The standard aims at the high data

transmission rates. Field programmable gate array (FPGA) technology is not only a key technology in digital system, but also plays an important role in application specific integrated circuit (ASIC) design field because of its design flexibility, and higher integration [5]. The technical line for the implementation of MB-OFDM transmitter baseband module with Xilinx series FPGA is introduced in this paper. It has been proved by the simulation results that the design of MB-OFDM transmitter baseband based on FPGA has good characterizes such as simple structure, easy implementation, high reliability and so on. The design of MB-OFDM transmitter baseband based on FPGA is discussed also provides performance results of the MB-OFDM system based on Xilinx Vertex or Altera.

II- THE STRUCTURE OF MB-OFDM TRANSMITTER BASEBAND

Fig.1 shows the transmitter architecture for the MB-OFDM system, which is very similar to the architecture for conventional OFDM physical layer, except that the carrier frequency changes with the Time Frequency code (TFC) [6]. The whole system consists of three parts: baseband, RF front-end and transmitter antenna.

After scrambling, encoding, puncturing and bit interleaving, the binary serial data shall be mapped into constellation points according to the Gray-coding. Here, continuous modulation such as Quadrature phase-shift keying (QPSK) is recommended. Then the stream of complex symbols is mapped into coefficients of Inverse Fast Fourier Transform (IFFT)[7], the modulated signal is achieved. Zero-padded suffixes (ZPS) are appended to the modulated signal and then modulate this signal to various sub-band through RF front-end. Finally, the modulated signal on various sub-band is transmitted.

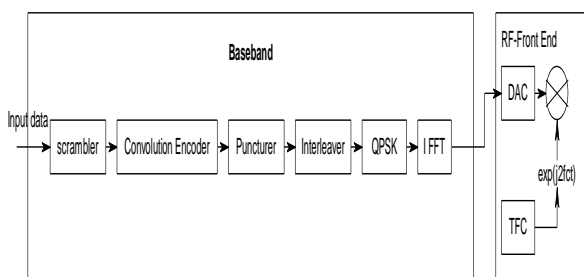


Fig :Structure of MB-OFDM Transmitter Baseband

The baseband is the core of a transmitter system for MB-OFDM system. A Zero-Padded suffix is appended to eliminate ISI and capture sufficient multi-path energy to minimize the impact of inter-carrier interference (ICI).A time-frequency kernel is used to specify the centre frequency for transmission of each OFDM symbol. In the receiver, the channel estimation sequence (CES) in preamble and the pilots picked out from the OFDM symbols are used for channel estimation [6].

Scrambler

In telecommunications, a scrambler is a device that transposes or inverts signals or otherwise encodes a message at the transmitter to make the message unintelligible.

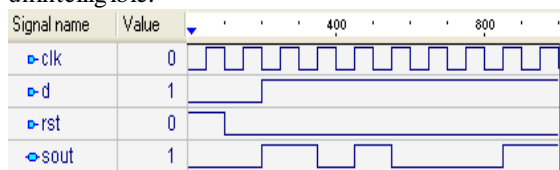


Fig. simulation result of scrambler

Convolution encoder

Convolutional encoder is one of the channel codes which can improve the reliability of channel and overcome the effect of noise [8]. The structure of convolutional encoder can be described in Fig.

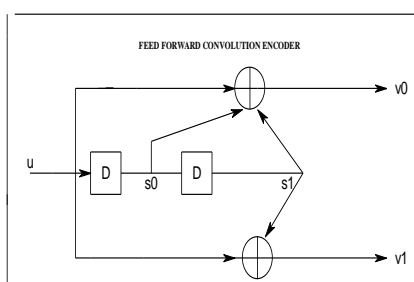


Fig: Convolution encoder

Output /simulation of feed forward convolution encoder, when input is 1011010100

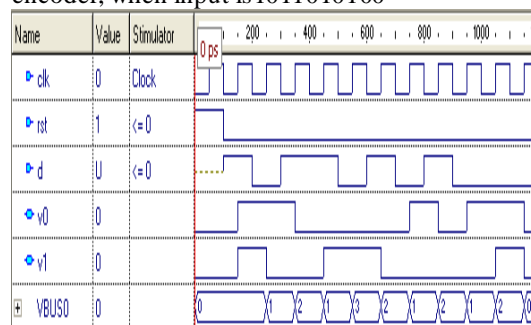


Fig: simulation result of feed forward convolution encoder

Puncture

The principle of puncturing is a process by which a few parity bits are deleted in order to improve the code rate. Suppose L or NL bits of the output for convolutional encoder, the puncturing matrix P with NL symbols is defined as a binary array, where “1” denotes the data that is sent out and “0” denotes the data that is deleted.

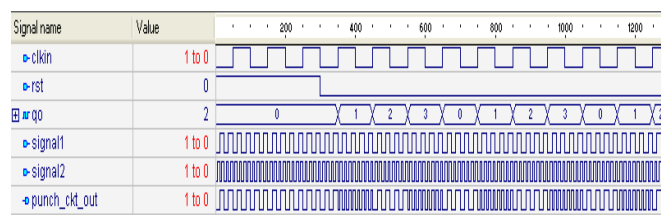


Fig. Simulation Result of Puncture

Random Interleaver

This interleaver scheme uses a fixed random permutation scheme to map the information sequence to the permutation order. A random interleaver scheme is shown below in Fig.

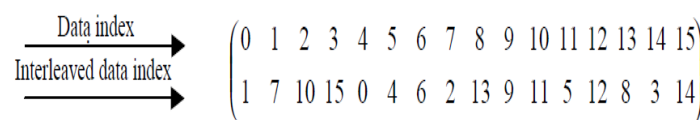


Fig. Random Interleave.

Output /simulation of pseudo random interleaver , when input is 11010010

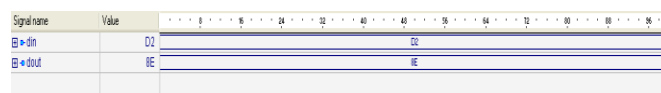
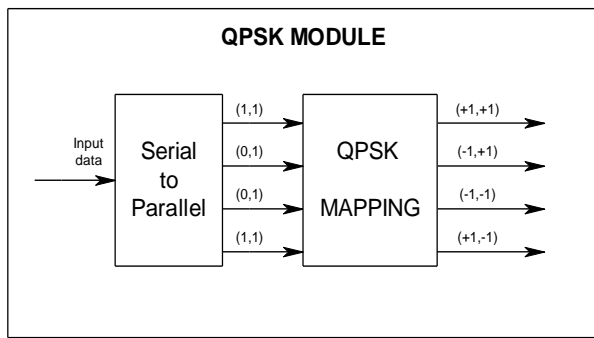


Fig . Simulation Pseudo Random Interleaver.

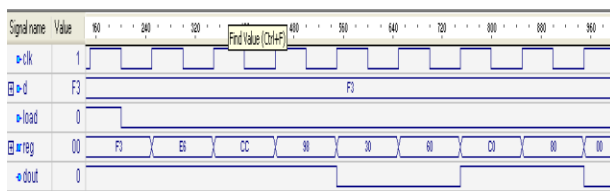
QPSK

The coded and interleaved binary serial input data shall be divided into groups of two bits and converted into a complex number representing one of the four QPSK constellation points.



Output /simulation of QPSK , when input is 10101010

Parallel to Serial



IFFT/FFT

IFFT is a core of the baseband of MB-OFDM transmitter. The bit streams will be modulated on various frequencies carrier by IFFT. In many applications high-speed performance is required. For this purpose, conventional multi-carrier techniques are usually chosen, but these results in the lowering of spectrum efficiency. The speed enhancement is the key contribution of the main processing blocks in OFDM system. This proposed work will provide high speed data transmission in ultra wideband spectrum by dividing the spectrum available into multiple bands.

Signal name	Value
in0	0
in1	1
in2	0
in3	1
X0	2
X1	4
Xi2	1
Xr2	5
Xr3	5
Xi3	5

Fig. Output /simulation of IFFT , when input is 0101

CONCLUSION

The results show that all modules designed has achieved the expected purpose both in precision and resource, with simplicity and high efficiency and can meet the demand of MB-OFDM systems. The development platform for Xilinx Virtex FPGA is used and VHDL language is selected, each module of transmitter baseband for MB-OFDM is realized in this paper. The simulation results indicate that the timing of each module is true. There are number of software for writing VHDL code like Altera, Xilinx, Active HDL etc. In FPGA implementation we have to do both things simulation and FPGA realization in that case /for that there is a need of FPGA kit either Xilinx or Altera. The

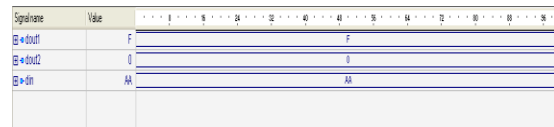
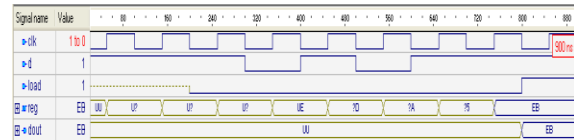


Fig. Simulation of QPSK

Serial to parallel converter



results can meet the requirement of MB-OFDM system. It provides the basis for the design of MB-OFDM system.

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