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Development of Data Acquisition and Analysis System on Virtex 5

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Abstract— ***This paper presents the development of Virtex5, Field Programmable Gate Array (FPGA) FPGA based data acquisition and analysis system. The system consists of data sampling and acquisition followed by Fast Fourier Transform Processor. The output Transformed data is read on host PC via RS232 for plotting and analysis. 'C' and MATLAB codes are developed for testing and verification and the FPGA subsystems are developed in VHDL.***

Keywords*— *FPGA, Data Acquisition, FFT, VHDL, ADC

I. Introduction

Data acquisition and analysis is a very common practice in the field of communication. Frequency analysis plays an important role in communication system design. Fourier transform is the most commonly used technique to convert time domain signal to frequency domain [1]. It is well known that the calculation of Fourier Transform involves many complex multiplication and additions. This makes it time consuming as the number of points goes on increasing. FFT algorithm reduces the computation complexities and speeds up the computation [1]. Parallel processing is a key factor for the fast computation. FPGA is a device which gives freedom of true parallel processing with high clock speed and at low power cost. Flexibility and customization in design makes FPGAs a first choice for the high speed data acquisition and processing systems

This paper deals with the design of a very simple data acquisition and analysis system. Current system acquires a data with rate of 100 MSPS. The data is stored in an internal block RAM and input to FFT block for frequency analysis.

II. System Architecture

The overall system consists of high speed ADC interface card, Virtex 5 FPGA, Serial interface RS232, switches for mode selection and LEDs for indication.

A .Overview

A 14 bit ADC LTC 2255 samples and digitizes the signal with sampling rate of 100 MSPS [2]. FPGA internal Block RAMs are used to store the 1024 points data. Sampled data is then fed to FFT core which produces the transformed data in the form of real as well as imaginary component. Real and imaginary component are stored in different block RAMs. Each block RAM is read via RS232 port on host machine. An application is developed in 'C' which converts the hex data to an integer and MATLAB code is developed for plotting the FFT output in the 0 to Fs/2 range. Switches are used for the triggering the processes and the LEDs indicate completion of certain processes. The block diagram given below gives an idea about the overall system architecture.

B. System functionality

Basically, system is working in 4 different processes data acquisition, FFT computation and data read out and plotting

1) Data sampling and acquisition process: In data sampling and acquisition process ADC samples the data at 100 MSPS with resolution of 14 bit. The sampled data is in the 2's compliment hex format. FFT required a 16 bit signed data. To get the 16 bit data signed data 14th bit was checked and copied to 15th and 16th bit. The first 1024 samples are stored in the block RAM. Reset switch triggers the acquisition process and LED glows after the completion of data storage.

2) FFT computation process: In this process sampled data is fed to FFT core which computes 1024 point FFT of the given data set. The output of FFT core is in the form of real and imaginary 27 bits, 2's compliment hex format, which is stored in two different blocks RAMs. One push to on switch triggers the FFT start signal and an LED is switched on to indicate that the computation is done and data is stored in block RAMs.

3) Data read out and plotting: This process is associated with the data reading on host PC and plotting. DIP switch setting is used to decide to read the data via RS 232 port. The data obtained by FFT core is 27 bits, signed hex data. RS 232 port can send data only in single byte format thus 5 bits are appended to MSB and make data 32 bit, 2' complement hex format. The Read process sends output data, byte by byte to transmit unit. The output data is then converted to an integer and MATLAB code is used to plot the data.

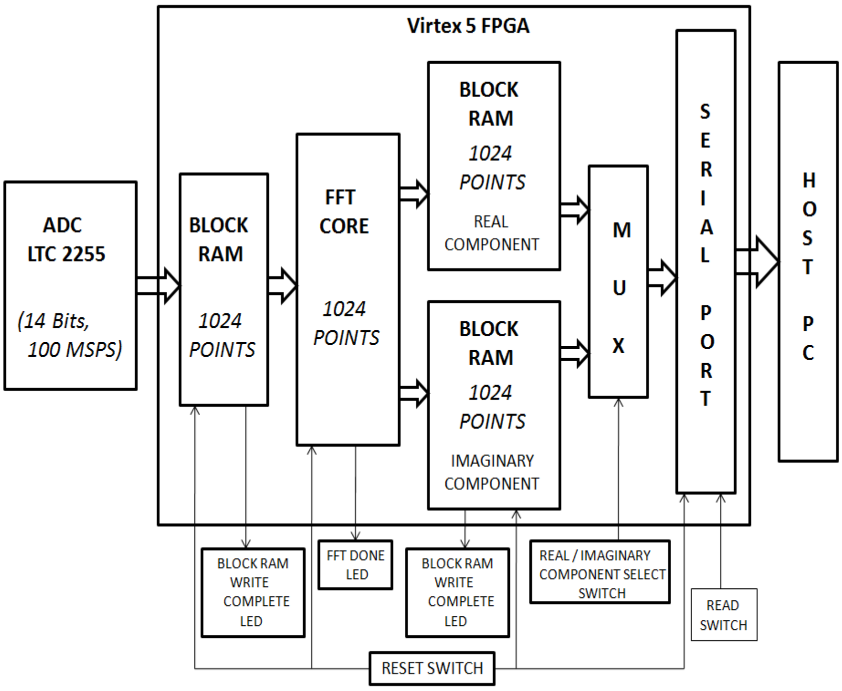

Fig.1 Block diagram of system

III. Testing And Verification

The main difficulty with the FPGA devices is testing and debugging the system. All the system component were tested module wise and then integrated to realize the whole system. There are test bench and waveform tools for simulation with some limitations.

A. *ADC calibration*

ADC calibration is necessary in every data acquisition system. ADC used in this experiment is LTC 2255 with 14 bit resolution. To test the ADC-FPGA interface ADC is calibrated with static voltage as well as dynamic signals. Figure 2 represents the expected values vs experimental results obtained. Linear graph shown below validates the interface.

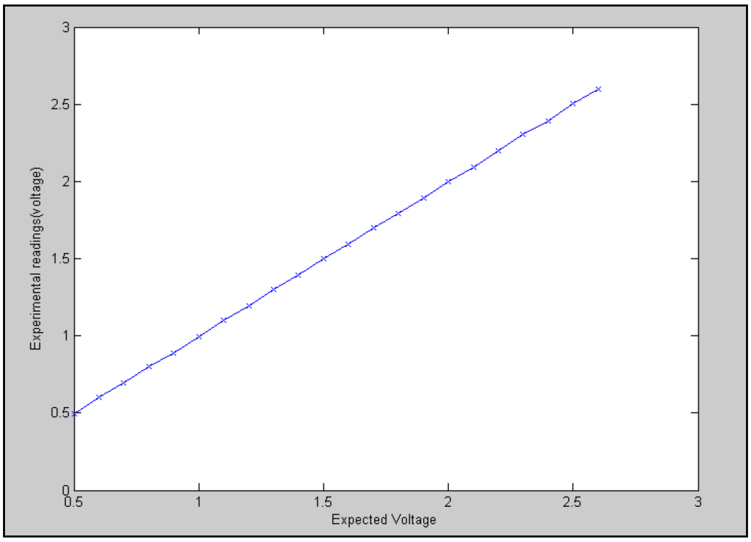

Fig.2 ADC calibration

B. *RS232 Port*

To test the RS232 port transmit module, first some known characters were sent and tested using storage oscilloscope. Later data was filled into block RAM and read back on PC to verify working of the transmit module. Receive module is also tested with the help of LEDs. The designed module is set with the baud rate of 9600.

C. Block RAM interface

Block RAM read / write operation was tested initially for small chunk of memory wherein switches were used for address generation and 8 bit data generation. LEDs were used for the data display. Once the interface is validated, serial port is used for the data entry and read out.

D. FFT core

FFT core is the main component of the design. FFT core is also tested initially for the 128 points. FFT core triggers on the FFT start signal which is given by the external switch. FFT core requires a 2's compliment hex data. To check the behaviour of the core a data for sine wave is generated by 'C' code and stored in the block RAM memory. On activating the start signal, FFT core fetches the data and computes the FFT. Output of the FFT core is again 2's compliment hex format [3] .

Results obtained by FFT core testing are then compared with the results obtained by the MATLAB *FFT ()* function for the same data set. In figure 3 the upper signal shows a time domain sinusoidal signal of frequency 20 Hz simulated and stored in the block RAM. Middle signal shows the results of MATLAB function and the last signal plot represents the results obtained by FPGA hardware.

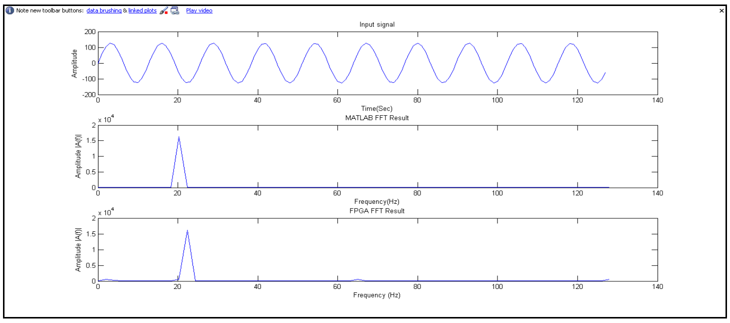

Fig. 3 Results of FFT core test 128 pt. FFT

To test the FFT core performance for non sinusoidal signals, 'C' code is developed which generates sine waves of 50 Hz, 230 Hz and 360 Hz and adds them together. The time domain mixed signal is represented by the upper plot in the fig.4. The time domain data set fed to the MATLAB *FFT()* function and FPGA hardware FFT core. The middle plot represents the results of MATLAB FFT function where as third plot represents the results obtained by the implemented FFT core in FPGA.

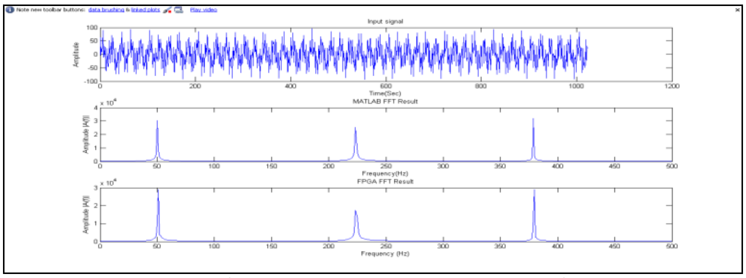

Fig.5 Results of FFT core test 1024 pt FFT (mixture of 3 signals)

The results comparison of FFT core output and MATLAB output gives certification of valid interface and implementation of core.

IV. Results

A Data acquisition and analysis system is realized by integrating all modules. This system is capable of showing the spectra of input signals with a bandwidth of 50 MHz. The system is tested for various signals with different frequencies. Figures shown below represent the outputs of the spectral analysis system.

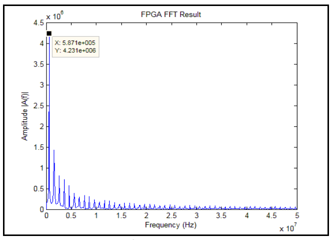

Fig 6 FFT of 500 KHz signal

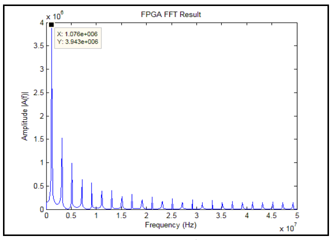

Fig.7FFT of 1MHz signal

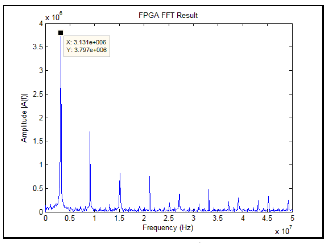

Fig 8 FFT of 3 MHz signal

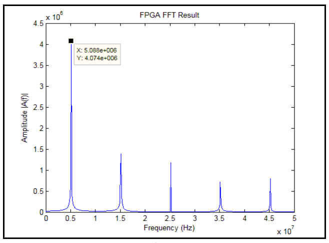

Fig 9 FFT of 5MHz signal

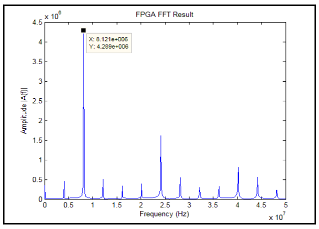

Fig 10 FFT of 10 MHz signal

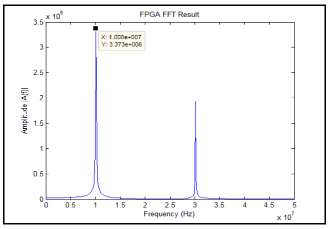

Fig 11 FFT of 10 MHz signal

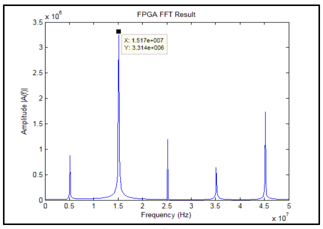

Fig 12 FFT of 18MHz signal

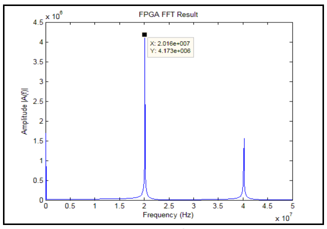

Fig 13 FFT of 20 MHz signal

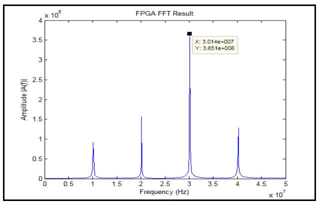

Fig 14 FFT of 30MHz signal

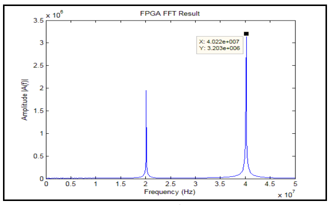

Fig 15 FFT of 40 MHz signal

FFT computation for different waveforms like sine, triangular, square, noise signal and arbitrary waveform (sinc function) were carried out. The following diagram shows the FFT plot for noise and Arbitrary waveform.

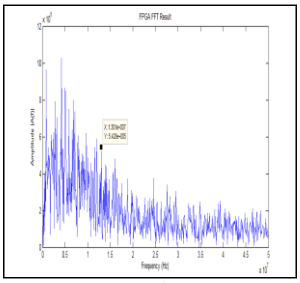

Fig 13 FFT of noise signal

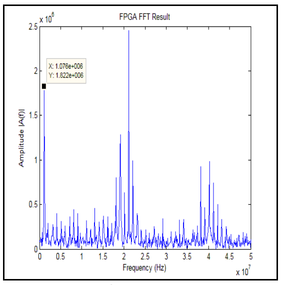

Fig 14 FFT of arbitrary signal

V. CONCLUSION

A Proposed data acquisition and analysis system is designed and implemented successfully on Virtex 5 FPGA [5]. Presently system consists of single channel for data acquisition, which works over a bandwidth of 50 MHz with 100 KHz spectral resolution. The testing and validation of a system is carried out with the help of various hardware and software tools. Currently the system operates under manual control. Spectral resolution can be increase by increasing a number of points for FFT computation. The whole system design language is VHDL; MATLAB is used only for the verification and plotting purposes which is one of the major achievements of the design team.

Proposed Data acquisition and analysis system is having a large number of applications. Presently work to make it fully automated and multichannel is underway

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