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Recent Survey for Bi-Directional Network on Chip Pipelined Architecture

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Abstract*— Bidirectional NOC architecture is efficient than the conventional architecture. In this paper BiNOC architecture allows each channel to transmit all direction and increases the bandwidth, reduces the access Latency and buffer size. We are using the pipelining architecture instead of parallel architecture. This reduces the size of the architecture with better result. It produces better transmission in the router with reduced traffic, also reduces the access latency 15% to 20% and enhances the performance through better resource utilization.

Keywords — ***Bi-NOC, Pipelining, Virtual channel allocator, Hi-speed VLSI.***

I. Introduction

Network-on-Chip (NoC) is an approach to design the communication subsystem between IP cores in a System On a Chip (SoC). NoCs can span synchronous and asynchronous clock domains or use unclocked asynchronous logic. This NoC brings an effective improvement over conventional busses and cross bar switches. The power requirement of the SoC is high where as it can be reduced by the NoC architecture. NoC is an developing paper in the field of VLSI. Since the use of emerging NoC architecture in VLSI it reduces the size of the architecture due to the reduced amount of buses and transmission lines. ." In a NoC system, modules such as processor cores, memories and specialized IP blocks exchange data using a network as a "public transportation" sub-system for the information traffic. The wires in the links of the NoC are shared by many signals. A high level of parallelism is achieved, because all links in the NoC can operate simultaneously on different data packets. The benefits in NoC is that an NoC is constructed to connect multiple point to point data link interconnected by switches , such that messages can be relayed from any source module to any destination module over several links, by making routing decisions at the switches. NoC provides separation between the computation and communication. The router in the NoC consists of conventional router and bidirectional router. In BINoC router each port can send the data as well as receive the data. This can connect to an point to point link or multipoint to multipoint link with one wire dedicated to each signal. The wires occupy much of the area of the chip, and in nanometer CMOS technology, interconnects dominate both performance and dynamic power dissipation, as signal propagation in wires across the chip requires multiple clock cycles. NoC links can reduce the complexity of designing wires for predictable speed, power, noise, reliability, etc. The NoC has the real challenges in the bidirectional NoC. In this BINoC router the ports are reconfigurable. The reconfiguration of ports is done by using the local information channel.

II. RELATED WORKS

The router architecture is able to sustain performance due to the fact that, statistically, not all buffers are used all the time. In our architecture it is possible to dynamically reconfigure different buffer depths for each channel. A channel can lend part or the whole of its buffer slots in accordance with the requirements of the neighboring buffers. To reduce connection costs, each channel may only use the available buffer slots of its right and left neighbor channels. This way, each channel may have up to three times more buffer slots than its original buffer with the size defined at design time [1]. This paper gives preferences to reduce the buffer size and also to reduce the power consumption. By using the reconfigurable router buffer depth will be reduced while comparing to the original router.

Using NoC architecture the power consumption can be reduced. the power consumption can be reduced both in input as well as output ports. This was described in [2] according to linear programming based techniques for synthesis of NoC architecture the total power consumption is equal to the sum of power consumed by cross bar switches, header etc,. The router usually has five input output ports. Any port can send a data also the same port can receive the same data; the power consumption rate varies with respect to injection rate at the processor. The power consumption at the output port is due to the presence of arbiter, FIFO and link controller. At the output port the contents of the packets are randomly generated, and the delay is also uniformly distributed within the mean delay interval. The physical link in the router also has power consumption when the packet is delivered. As we described above the router can connect to either point to point link or from multipoint to multipoint link [3] investigates bidirectional and multi drop transmission line interconnect for on chip high speed network. It consists of two differential amplifier which act both as transmitter and

receiver hence it is called as transceiver. The transmission lines have been widely used on printed circuit boards, cables and integrated circuits.

The problems in multi drop transmission line methods are couplers which usually consumes larger than the transmitter, the digital signal contain wide frequency components. The Characteristics of the multi-drop TL interconnect are evaluated by time-domain measurements. Pseudo-random bit sequence of 2 1 is input to Tx, and an output signal is measured by a digital oscilloscope. The obvious routing can be implemented on simple router hardware. Adaptive routing attempts to avoid hot spots by re-routing flows, but requires more complex hardware to determine and configure new routing paths. On chip bandwidth -adaptive networks to mitigate the performance problems of oblivious routing and the complexity issues of adaptive routing. The bisection bandwidth of network can adapt to changing network condition. In the typical virtual-channel router each output channel is connected to an input buffer in an adjacent router by a unidirectional link; the maximum bandwidth is related to the number of physical wires that constitute the link.

In an on-chip 2-D mesh with nearest neighbor connections there will always be two links in close proximity to each other, delivering packets in opposite directions [4].We can describe the implementation of bandwidth adaptive network in the form of two dimensional meshes with adaptive bidirectional links. The reconfiguration can be done rapidly in response to changing traffic demands. In the obvious routing path is designed using source and destination address [5]. An autonomous network reconfiguration system that enables a multi radio WMN to recover automatically from local link failures to preserve network performance [6]. This outperforms existing failure-recovery schemes in improving channel-efficiency by more than 90% and in the ability of meeting the applications' bandwidth demands by an average of 200%.Wireless mesh networks (WMNs) are being developed actively and deployed widely for a variety of applications, such as public safety, environment monitoring, and citywide wireless Internet services [7]. Switch-to-switch flow control algorithms, such as on-off, credit based and ack /nack mechanisms regulate the traffic flow *locally* by exchanging control information between the neighboring routers [8]. Switch to switch flow control does not regulate the actual packet rate directly at the traffic source level. On the other hand end to end flow control algorithm conserves number of packets injection rate at the source of message. The major drawback of end-to-end control algorithms is the large overhead incurred when sending the feedback information [9].

III. PROBLEM STATEMENT

Larger buffer sizes can ensure performance during the execution of different applications. While transferring the packet to the destination in the router it needs the larger buffer. This can be avoided by the many techniques. Also the ordinary router uses more power in the packet transfer, bigger caches and independent memory controllers. In the existing paper it uses the multiprocessor SoC, hence it has larger chip area, huge memory space, larger busses and number of transmission lines. Due to the transmission of packets in the same direction at the same time the packets forms the circular ring structure and due to the formation of the circular structure the dead lock condition occurs. To avoid the dead lock the circular structure should be broken.

IV. PROPOSED BINOC PIPELINED ARCHITECTURE

In the proposed architecture bidirectional router which can be dynamically reconfigure within the ports. The router has set of ports to communicate with the logic element such as local, East, West, North and south. It receives the incoming pockets and forwards them into appropriate ports. Buffers are present at various ports to store the packets temporarily. Control logic will be present to take routing decisions and arbitration decisions.

In this work we design a light-weight parallel router. The motivation is to reduce the area which also reduces the power consumed. We choose one of the popular methods of buffering called store and forward. The motivation behind choosing such a scheme is to have the simplest possible decoding logic, thereby, reducing both area and power. Establishment of connections is made automatically without any complex decoding logic. Each port consists of an input port, output port and the acknowledgement line. The packets will be sending to the output port while the output port is capable to accept the data from the input port, this will be processed based on acknowledgement line in each ports

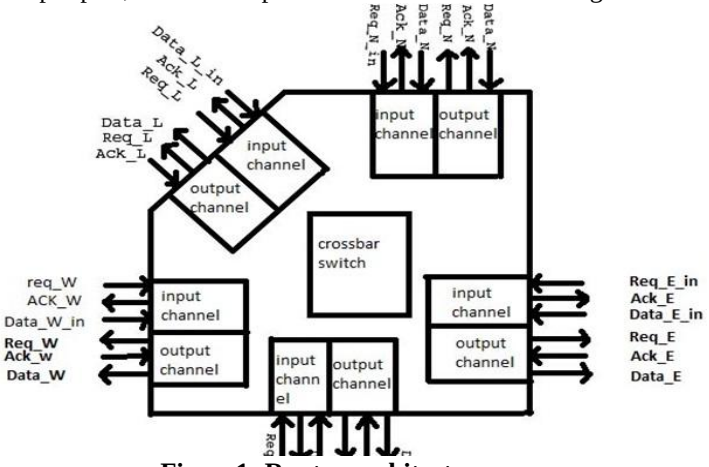

Figure1: Router architecture.

In the BINoC architecture it consists of bidirectional in out ports, virtual channel, cross bar switches, switch allocator, channel control and VC allocator.

A. Bidirectional Channel

Bidirectional channels are extensively used for supporting electronic design of SoC. The challenge in NoC is the distributed CDC protocol that would achieve certain criterias such as correctness, high performance and low cost. In bidirectional channel the proposed direction decision mechanism is centralized and the packets are configured according to application analysis results.

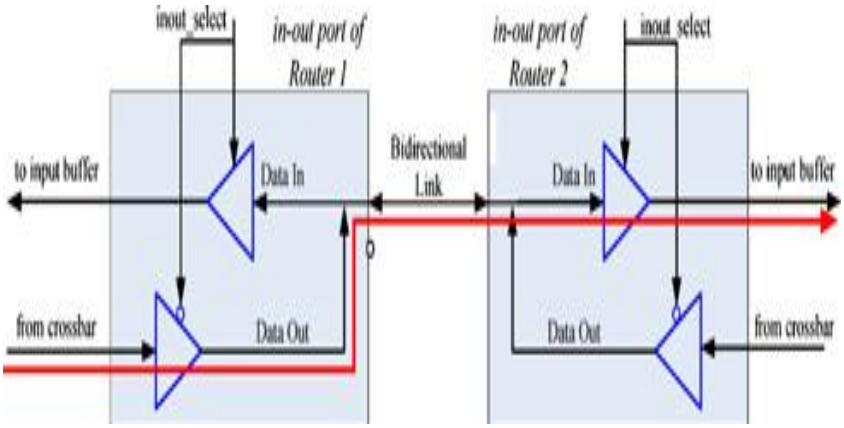

Figure 2: bidirectional link

B. In Out Ports

The in out ports used in the BINoC architecture is designed based on the priority. ie; one of the in out port is designed with high priority and the next in out port is designed with low priority. each ports are bidirectional ports hence a pair of routers will determine its own transmission direction based on channel control protocol. It has the feature of doubling the channel bandwidth, ie; if two channels sends the packets concurrently to the same port then the architecture doubles the channel bandwidth.

The use of input port and the output port are determined by using control channel. The control channel generates the in out select line. As long as the in out select signals assigned properly hence there is no chance of occurring conflicts and unpredictable situations.

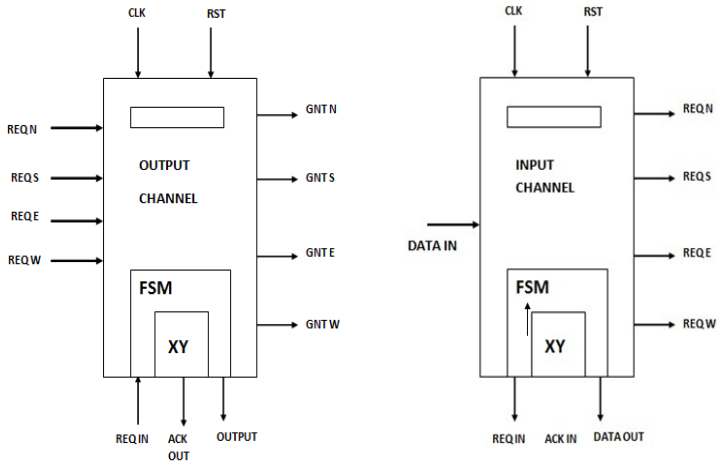

Figure 3: a) Output channel b) Input channel

C. Virtual Channel

The number of virtual channels for each connection and reduces the likelihood of blocking. Each cell is large enough to contain a virtual path and virtual connection identifier. These identifiers allow the cells to be transmitted over a single connection in any order (asynchronously). The router ``switches the labels'' as the cells arrive, hence the name *label switching routers*. The virtual channel consists of number of channels with a small buffer. Also it has an multiplexer and an de-multiplexer on either sides of the channel.

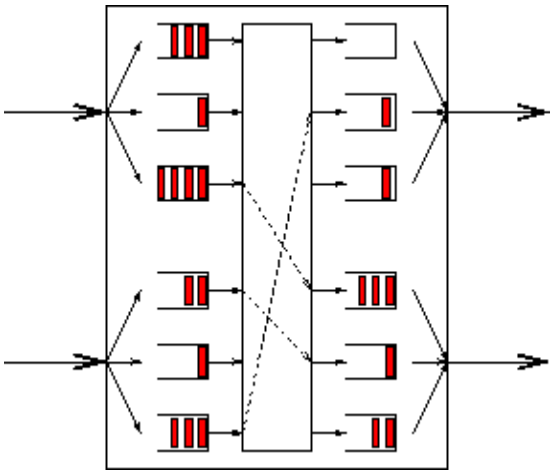

Figure 4: 3 virtual channel per connections

The virtual channel performs pipelining operation. The flits from the input port is stored at any of the channels and then it is processed and then the outputs are send to the output port which is ready to accept the flits. The packets are sending to output port based on the priority. In this, the channel to be processed is assigned by using virtual channel allocator. We share the VC buffers among the two bidirectional channels in each direction, there is no overhead in the VA stage compared to the conventional VC router design.

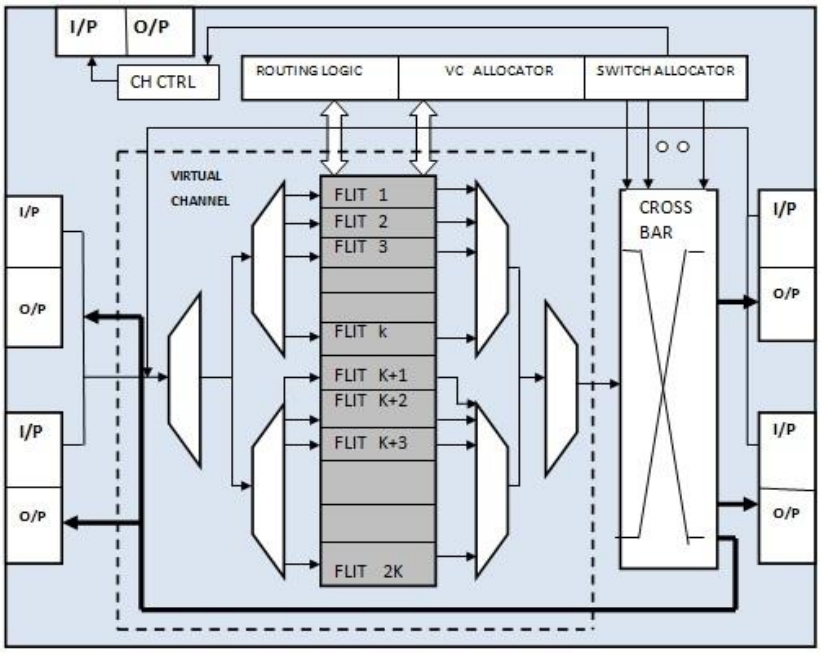

Figure 5: Proposed pipelined BINoC architecture.

D. Switch Allocator

The switch allocator allocates the time slots. This helps the crossbar switch to move the flits from the input VC to output. NoC contains arbitration, where the arbiter has equal number of input and output lines. In BINoC the channel bandwidth will increase from one packet to two packets. this can be done when the first stage arbiter is doubled to capable of accepting two request in each input direction. The cross bar switch has n number of input lines and n number of output lines, the switch allocator allocates the switches to be performed to get the output at the output port shown in the figure6.

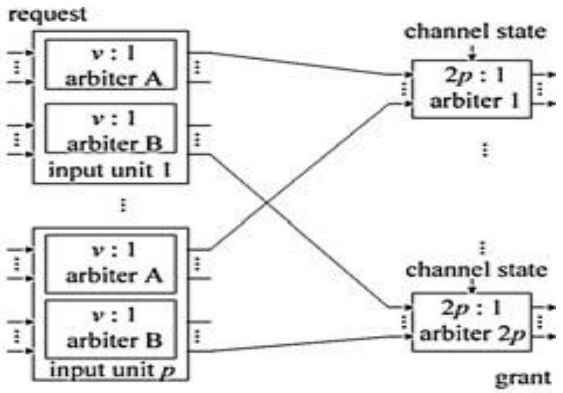

Figure 6: Switch Allocator

E. Dead lock Free

The dead lock condition occurs when number of senders waits to release the sources. many existing deadlock avoidance routing techniques, such as dimension-ordered and the turn-model-based routing algorithms

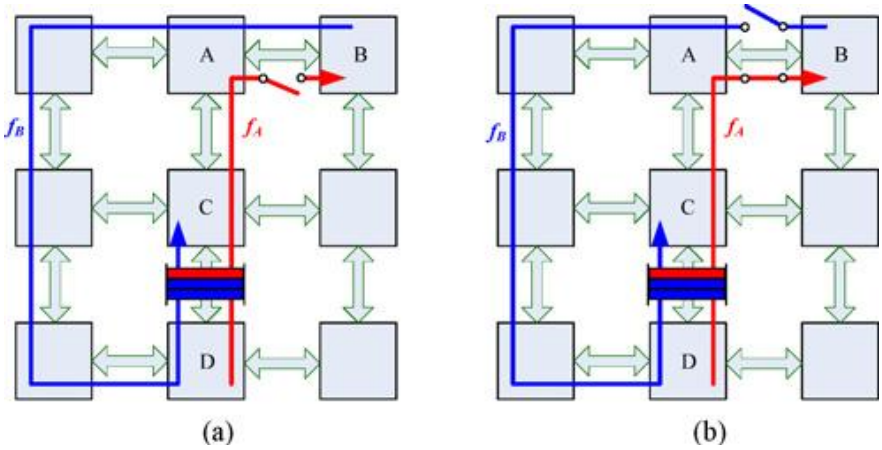

Figure 7: Deadlock

The figure 7(a) [10] shows that the possible dead lock conditions due to pressure based CDC. This requires ration available bandwidth among different flows according to their corresponding pressures. In other words, the two channels between nodes A and B will be configured as opposite direction in this case.

Figure 7(b) [10] says that In contrast, in BiNoC, flow *fA* will be able to gain both Bidirectional channel accesses between nodes A and B since the heavier flow *fB* in the opposite direction is blocked due to limited buffer space at node A; thus, the channel request From *fB* will be disabled as illustrated in Fig. 7(b). In other words, it is useless to allocate physical channel to *fB*. Thus, *fA* can be delivered by all physical channels between nodes A and B, which can help to relief congestion faster, until there is any available buffer space for *fB* to move forward.

V. CONCLUSION

Hence the bidirectional network on chip with the pipelining architecture increases the speed in the router. In this architecture the access latency can be reduced as 15 to 20%. This architecture does not contain the deadlock condition since the packet needs not to be waited for a long time to reach the output port. The usage of pipelining architecture is also an important reason for avoiding the deadlock in the architecture. The power consumption is low in the bidirectional router. This architecture has self reconfigurable; the reconfiguration is done on the directions based on the local information.

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