



## Comparative Analysis of TG Based 16 Bit Adders using 180nm Technology

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**Abstract**— Continuous scaling of the transistor size and reduction of the operating voltage has led to a significant performance improvement of integrated circuits. Low power consumption and smaller area are some of the most important criteria for the fabrication of DSP systems and high performance systems. In this paper there is try to determine the best solution to this problem by comparing a few adders.

In this project when we compare the power consumption of all the adders we find that carry look ahead and Carry bypass adder consume more power. The conventional full adder is built by 28 transistors. So, the transistor count is very high. The average power consumption and delay is very high. In this paper a new circuit which is made by mainly the TG technology. For the purpose of comparative analysis of TG based 8-bit different adder Design using 180nm technology, we use TANNER tool.

**Keywords**— Ripple Carry Adder, Carry Look-ahead adder, Carry Bypass Adder, TG based CMOS Logic Design Style.

### 1. INTRODUCTION

The adder is the most commonly used arithmetic block of the Central Processing Unit (CPU) and Digital Signal Processing (DSP), therefore its performance and power Optimization is of utmost importance. With the technology scaling to deep sub-micron, the speed of the circuit increases rapidly. At the same time, the power consumption per chip also increases significantly due to the increasing density of the chip. Therefore, in realizing Modern Very Large Scale Integration (VLSI) circuits, low-power and high-speed are the two predominant factors which need to be considered. Like any other circuits' design, the design of high-performance and low-power adders can be addressed at different levels, such as architecture, logic style, layout, and the process technology. As the result, there always exists a trade-off between the design parameters such as speed, power consumption, and area. The objective of our project is to design a lower-power and smaller area as a prime consideration [1]. The research efforts of the past years in the field of digital electronics have been directed towards the low power of digital systems. Recently, the requirement of probability and the moderate improvement in battery performance indicate power dissipation is one of the most critical design parameters day by day the demand of probability and mobility is increasing. Also the area of chip design is taken into consideration while talking about probability. Hence three most widely accepted parameters to measure the quality of a circuit or to compare various circuit styles are area, delay and power dissipation.

There are three major sources of power consumption in digital CMOS circuits, which are summarized in the following equation [1].

$$\begin{aligned} P_{total} &= P_{switching} + P_{short-circuit} + P_{leakage} \\ &= (\alpha_{0 \rightarrow 1} \times C_L \times V_{dd}^2 \times f_{clk}) + (I_{sc} \times V_{dd}) \\ &\quad + (I_{leakage} \times V_{dd}) \end{aligned} \quad (1)$$

The first term represents the switching component of power, where  $C$  is the load capacitance,  $f_{clk}$  is the clock frequency and  $\alpha_{0 \rightarrow 1}$  is the node transition activity factor. The second term is due to the direct path short circuit currents,  $I_{sc}$ , which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current,  $I_{leakage}$ , which can arise from substrate injection and sub threshold effects, is primarily determined by fabrication technology considerations. However, while supply voltage reduction is the most effective way to reduce the power consumption, such a reduction require new design methods for low-voltage and low power integrated circuits. Since an average of 15-20% of the total power is dissipated in glitching, low power can also be achieved by reducing the glitches of the circuit [1]. The deep submicron devices gives CMOS VLSI design a great chance to operate at higher speed, especially for digital signal processing. In our study, novel designs for a full adder will be proposed and verified. All nodes in the proposed full adder have a full-voltage swing and there is no static short-circuit current problem. The 8-bit carry-select adders were designed in a 0.4pm CMOS technology using 4 different circuit design styles. The performance is better than the previous designs as shown through simulation. This paper is organized

as follows. In Section 2, we will review the different adder architectures. Section 3 describes the performance parameters of 8 bit different adders. in Section 4, Final result is discussed and the conclusions are summarized in Section 5.

## 2. LOGIC DESIGN STYLES

Adder is the most commonly used arithmetic block of the Central Processing Unit (CPU) and Digital Signal Processing (DSP), therefore its performance and power optimization is of utmost importance. For arithmetic applications, following three different logic styles are used for a full adder design to achieve best performance results for adder design.

### 2.1 Ripple Carry Adder

In the figure 1, the full adder is built by 18 transistors by using TG technology. In this circuit the design process all simulations are run using Micron Technology's 0.18  $\mu\text{m}$  process models with typical n-channel and p-channel drive, a 1.8 V power supply. In the schematics all logic is designed using a different gate width for NMOS and PMOS and a minimum length of .18  $\mu\text{m}$  for NMOS and PMOS. With the help of below full adder 6-bit ripple carry adder is developed. In the circuit there are three inputs A, B, C and two outputs sum and carry.

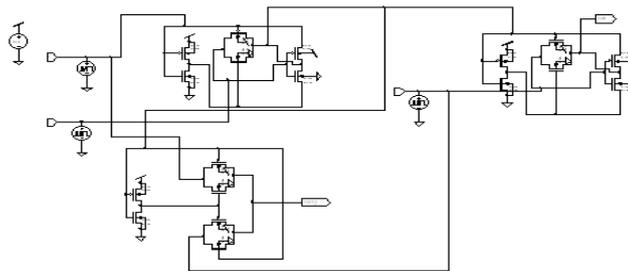


Fig 1: TG Based Full Adder

### 2.2 Carry Look-ahead Adder

In the figure 2, the carry look-ahead adder is built by 30 transistors by using TG technology. In this circuit the design process all simulations are run using Micron Technology's 0.18  $\mu\text{m}$  process models with typical n-channel and p-channel drive, a 1.8 V power supply. In the schematics all logic is designed using a different gate width for NMOS and PMOS and a minimum length of .18  $\mu\text{m}$  for NMOS and PMOS. With the help of below full adder 16-bit carry look-ahead adder is developed. In the circuit there are three inputs and two outputs.

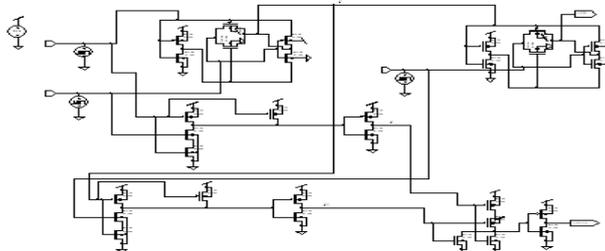


Fig 2: TG Based Carry Look-ahead Adder

### 2.3 Carry Bypass Adder

In the figure 3, the 2 bit carry bypass adder is built by 60 transistors by using TG technology. In this circuit the design process all simulations are run using Micron Technology's 0.18  $\mu\text{m}$  process models with typical n-channel and p-channel drive, a 1.8 V power supply. In the schematics all logic is designed using a different gate width for NMOS and PMOS and a minimum length of .18  $\mu\text{m}$  for NMOS and PMOS. With the help of below full adder 6-bit carry bypass adder is developed. In the circuit there are three inputs A, B, C and two outputs sum and carry.

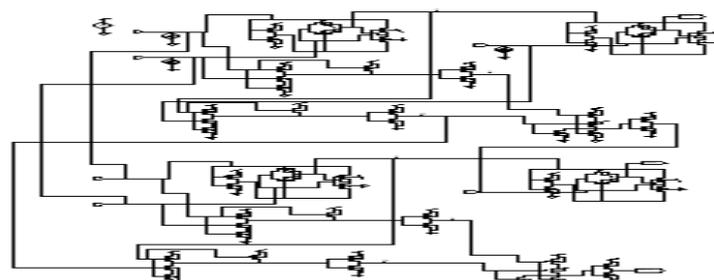


Fig 3: TG Based Carry Bypass Adder

### 3. ADDER ARCHITECTURES

Multiple-bit addition can be as simple as connecting several full adders in series or it can be more complex. How the full adders are connected or the technique that is used for adding multiple bits defines the adder architecture. Architecture is the most influential property on the computation time of an adder. This property can limit the overall performance. In general the computation time is proportional to the number of bits implemented in the adder. Many different adder architectures have been proposed to reduce or eliminate this proportional dependence on the number of bits. Several adder architectures are reviewed in the following sections.

#### 3.1 Ripple Carry Adder (RCA)

An n-bit ripple carry adder consists of 'n' full adders with the carry signal that ripples from one full-adder stage to the next, from LSB to MSB. It is possible to create a logical circuit using several full adders to add multiple-bit numbers. Each full adder inputs a  $C_{in}$  which is the  $C_{out}$  of the previous adder. Addition of k-bit numbers can be completed in k clock cycles. A 4-bit ripple carry adder structures is shown in figure 4.

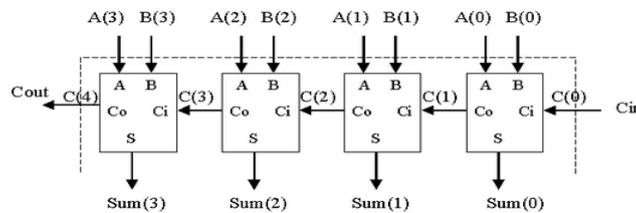


Fig 4: Structure of 4-Bit Ripple Carry Adder

The ripple-carry adder has many advantages like low power consumption, low area and simple layout. The drawback of the ripple carry adder is its slow speed because each full adder must wait for the carry bit to be calculated from the previous full adder.

#### 3.2 Carry Look-ahead Adder (CLA)

To reduce the computation time, faster ways to add two binary numbers by using carry look ahead adders. It is done by creating two signals (P and G) for each bit position, based on if a carry is propagated through from a less significant bit position (at least one input is a '1'), a carry is generated in that bit position (both inputs are '1'), or if a carry is killed in that bit position (both inputs are '0'). In most cases, P is simply the sum output of a half-adder and G is the carry output of the same adder. After P and G are generated the carries for every bit position are created.

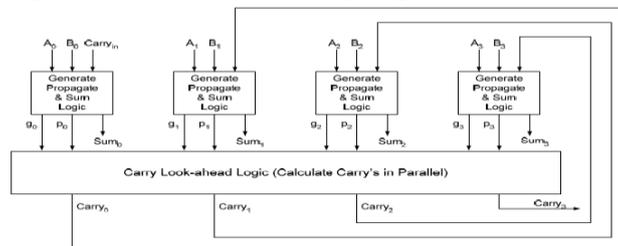


Fig 5: Structure of 4-Bit Carry Look-ahead Adder

These block based adders include the carry bypass adder which will determine P and G values for each block rather than each bit, and the carry select adder which pre-generates sum and carry values for either possible carry input to the block. On the other hand adder designs include the conditional sum adder, carry skip adder, and carry complete adder. In carry look-ahead architecture instead of rippling the carry through all stages (bits) of the adder, it calculates all carries in parallel based on equation (2).

$$C_i = g_i + p_i C_{i-1} \tag{2}$$

In equation (2) the  $g_i$  and  $p_i$  terms are defined as carry generate and carry propagate for the  $i$ th bit. If carry generate is true then a carry is generated at the  $i$ th bit. If carry propagate is true then the carry-in to the  $i$ th bit is propagated to the carry-in of  $i+1$  bit. They are defined by equations (3) and (4) where  $A_i$  and  $B_i$  are the binary inputs being added.

$$g_i = A_i B_i \tag{3}$$

$$p_i = A_i \oplus B_i \tag{4}$$

#### 3.3 Carry Bypass Adder (CBA)

The carry-bypass or carry-skip adder is much like the RCA only it has a carry bypass path. This architecture divides the bits of the adder into an even number of stages  $M$ . Each stage  $M$  has a carry bypass path that

forwards the carry-in of the  $M_i$  stage to the first carry-in of the  $M_{i+1}$  stage. If the binary inputs are such that the carry would normally ripple (or propagate) from the input of the  $M_i$  stage to the input of the  $M_{i+1}$  stage, then the carry takes the bypass path. A multiplexer is inserted between each stage  $M$  of the adder to choose from the normal ripple path or the bypass path (see Figure 6).

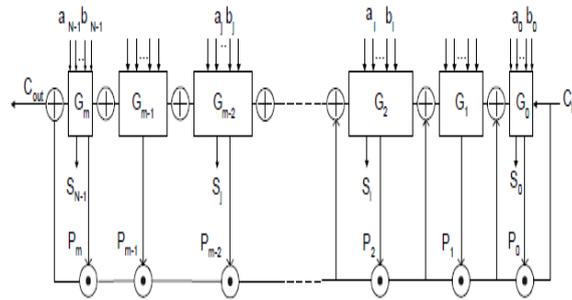


Fig 6: Structure of 4-Bit Carry Bypass Adder

In the figure the inputs to each full adder block are carry generate (gi) and carry propagate (pi). These signals will be discussed in more detail in the carry look-ahead adder discussion. When a bypass occurs it allows the  $M_{i+1}$  stage to start evaluating sums instead of waiting for the  $i$ th stage to ripple the carry through each bit of the stage.

#### 4. FINAL RESULT

The Table 1 is carried out by using a gate width of .64  $\mu\text{m}$  for NMOS and 1.7  $\mu\text{m}$  PMOS and a minimum length of .18  $\mu\text{m}$  for NMOS and PMOS. The result is carried out at 1.8v supply voltages and average powers consumed and delay at sum and carry output are finding out.

Design Style	No. of Transistor	Minimum length( $\mu\text{m}$ )	Width of NMOS( $\mu\text{m}$ )	Length of PMOS( $\mu\text{m}$ )	Avg. Power Consm. (watts)	Prop. Delay at sum (sec)	Prop. Delay at carry (sec)
RCA	294	0.18	0.64	1.7	$1.39 \times 10^{-4}$	$2.44 \times 10^{-9}$	$1.33 \times 10^{-9}$
CLA	484	0.18	0.64	1.7	$3.46 \times 10^{-4}$	$1.46 \times 10^{-7}$	$1.08 \times 10^{-9}$
CBA	484	0.18	0.64	1.7	$2.46 \times 10^{-3}$	$1.46 \times 10^{-7}$	$1.13 \times 10^{-9}$

Table 1. Performance parameters of 16 bit adders

From the above table it is concluded that TG based ripple carry adder has lesser no. of transistor count, so lesser be the area, less average power consumed and less power delay at sum and output as compare to TG based carry look-ahead adder and TG based carry bypass adder.

#### 5. DISCUSSION AND CONCLUSION

It has been observed that TG Based Ripple Carry Adder (RCA) logic design style exhibit better characteristics (power dissipation and area) as compared to other design styles. So, RCA logic style can be used where power and high speed low and lesser area is the prime aim. Whereas, TG Based Carry Look-ahead Adder (CLA) and TG Based Carry Bypass Adder (CBA) consumes more power than RCA. From Table 1 it is also concluded that propagation delay at sum and carry output of TG Based RCA is also less than that of TG Based CLA and TG Based CBA.

In this thesis we conclude that power dissipation in TG based RCA adders are very less as compare to TG based CLA and TG based CSA.

#### 6. ACKNOWLEDGMENTS

Our thanks to the experts who have contributed towards the development of template.

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