A Review on: Floorplanning – Based Design Methodology

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Abstract: A circuit is usually laid out according to a set of layout rules. A layout conforming with the given set of design rules is called a legal layout. The measure of the quality of a given solution to the circuit layout problem is the efficiency with which the circuit can be laid out according to the formal design rules dictated by the VLSI technology. Main objective of this review is to study the various techniques for wire length minimization, power minimization & delay minimization.

Keywords: chip, floorplan, circuit, integrated circuits.

I. INTRODUCTION

The size of present-day computing systems demands the elimination of repetitive manual operations and computations in their design. This motivates the development of automatic computing systems. To achieve this task, a basic understanding of the design problem and full knowledge of the design process are essential. Only then could one hope to efficiently and automatically fill the gap between system specification and manufacturing. Automation of a given (design) process requires an algorithmic analysis of it. The availability of fast and easily implementable algorithms is essential to the discipline[2].

In order to take full advantage of the resources in the very-large-scale integration (VLSI) environment, new procedures must be developed. The efficiency of these techniques must be evaluated against the inherent limitations of VLSI. Previous contributions are a valuable starting point for future improvements in design performance and evaluation[1].

II. CIRCUIT LAYOUT

Physical design (or layout phase) is the process of determining the physical location of active devices and interconnecting them inside the boundary of a VLSI chip (i.e., an integrated circuit). The measure of the quality of a given solution to the circuit layout problem is the efficiency with which the circuit (corresponding to a given problem) can be laid out according to the formal (design) rules dictated by the VLSI technology. Since the cost of fabricating a circuit is a function of the area of the circuit, techniques regarding circuit layout aim to provide layouts with a smaller area. Also, a smaller area means less defects, hence a higher yield. These layouts must have a special structure to guarantee their wirability (using a small number of planes in the third dimension).

A circuit is usually laid out according to a set of layout rules (or geometric designing rules). These layout rules are somewhat a form of minimum allowed values for some separation, width and overlaps, are a reflection of the constraints imposed by the latest technology. The expression of these values is a function of a parameter, that is...
dependent on the technology. The parameter \( x \) approximately denotes the maximum possible accidental displacement. (In the early 1980s, \( x \) was about 3 microns; in the early 1990s, submicron fabrication became feasible.) A layout conforming with the given set of design rules is called a legal layout.

Other criteria of optimality, for example, wire length minimization, power minimization, delay minimization, and via minimization also have to be taken into consideration. In present-day systems, delay minimization is becoming more critical. The focus is on to design circuits that are fast while having small area.

III. VLSI TECHNOLOGY

a) MOS - The most prevalent VLSI technology is metal-oxide-semiconductor (MOS) technology. The three possibilities of functional cells (or subcircuits) are p-channel MOS (PMOS), n-channel MOS (NMOS), and complementary MOS (CMOS) devices. PMOS and NMOS are not used anymore. CMOS offers very high regularity and often achieves much lower power dissipation than other MOS circuits. VLSI technology offers the user a new and a range of complex "circuits being off the shelf" (circuits being predesigned), whereas VLSI design processes are such that own special circuits of considerable complexity can be designed by system engineers. This provides an improved degree of freedom for designers.

b) Photolithography - Photolithography is used to pattern the layers of an integrated circuit. Photoresist (PR) is placed on the wafer surface and the wafer is spun at high speed to leave a very thin PR coating. A photosensitive chemical (PR) is used with a mask to define areas of wafer surface by exposure to ultraviolet light. The mask consists of opaque and transparent materials patterned to define areas on the wafer surface. It is the pattern of each mask that an engineer designs.

c) Cell Placement - Cell placement in VLSI layout is an important phase in VLSI design. The VLSI cell placement problem involves placing a set of cells on a VLSI layout for a given netlist. The netlist provides the connectivity between every cell and a library containing layout information for each cell type. The information regarding layout includes the height and width of the cell, the location of each node. The primary goal of cell placement is to determine the best location of each cell so as to minimize the wirelength of the nets connecting the cells together and the total area of the layout. With standard cell design, the layout is organized into rows having equal height, and the required placement should have equal length rows.

IV. CHARACTERISTICS OF FLOORPLANNING

Figure 2: Example of Floorplan

a) Floorplan design is an important step in the physical design process of VLSI circuits. A floorplan \( F \) is a subdivision of an enclosing rectangle by horizontal and vertical line segments into non-overlapping rectangles. A rectangle not subdivided by any line segment is called a basic block.

b) Given a circuit \( C = (M, N) \) represented by a hypergraph, the floorplanning problem is to determine the approximate location of each module in a rectangular chip area. The floorplanning problem in chip layout is analogous to floorplanning in building design where there is a set of rooms (modules) and the approximate location of each room must be determined based on some proximity criteria.

c) An important step in floorplanning is to decide the relative location of each module. A good floorplanning algorithm should: minimize the total chip area, make the subsequent routing phase easy; and improved performance, by, for example, reducing signal delays.

V. OPTIMIZATION ALGORITHMS

- Simulated Annealing: Simulated annealing is a technique used to solve general optimization problems, floorplanning problems being among them. This technique is especially useful when the solution space of the problem is not well understood. Simulated annealing examines the configurations of the problem in sequence. Each configuration is
actually a feasible solution of the optimization problem. The algorithm moves from one solution to another, and a global cost function is used to evaluate the desirability of a solution.

- **Genetic Algorithm:** Genetic algorithm operates on the principle of survival-of-the-fittest, in which weak individuals die before reproducing, whereas stronger ones survive and bear many offspring and breed children, that often inherit qualities that are, in many cases superior to their parent’s qualities. The operators Reproduction, crossover and mutation are used to create a new and better population. Genetic algorithm not only provides an alternative approach to problem solving, it also outperforms other traditional methods.

- **Memetic Algorithm:** The memetic algorithms can be viewed as a marriage between a population-based global technique and a local search made by each of the individuals. It is a special kind of genetic algorithms with a local hill climbing. As in genetic algorithms, memetic algorithms are a population-based approach. They have shown that they are orders of magnitude faster than traditional genetic algorithms for some problem domains. Under a memetic algorithm the population is initialized at random or using a heuristic.

- **PSO:** Many engineering design problems can be formulated as constrained optimization problems. Heuristic methods are quite suitable and powerful for obtaining the solution of engineering optimization problems. Particle Swarm Optimization (PSO) is a relatively new heuristic approach utilized for engineering optimization problems due to its simple principle and ease of implementation. Particle swarm optimization (PSO) is a bio-inspired metaheuristic that was proposed by James Kennedy and Russell Eberhart in 1995.

Other properties of PSO include:

1. PSO performs a population-based search, using particles to represent potential solutions within the search space. Each particle is characterized by its position, velocity, and a record of its past performance.
2. At each flight cycle, the objective function is evaluated for each particle, with respect to its current position, and that information is used to measure the quality of the particle and to determine the leader in the sub-swarms and the entire population.
3. The PSO algorithm is a relatively recent optimization algorithm, which is quite simple, since it only consists of two rules for obtaining a new solution from a previous one.

- **ACO:** In order to deal with the slow convergence of PSO, various hybrid methods are developed. Adding some abilities of one method to the PSO algorithm improves the performance of the resulted algorithm. Recently, heuristic particle swarm ant colony optimization (HPSACO) is proposed by the authors. HPSACO utilizes a particle swarm optimization with passive congregation (PSOPC) algorithm as a global search, the idea of ant colony approach (ACO) worked as a local search and the harmony search (HS) utilized to handle the boundary constraints.

   The method based on hybrid PSO and the ACO, is called particle swarm ant colony optimization (PSACO), which has been originally introduced by Shelokar et al. for solving the continuous unconstrained problems and recently utilized for the design of structures by the authors. The heuristic particle swarm ant colony optimization algorithm (HPSACO) is resulted from combining PSACO and HS.

- **Hybrid:** Heuristic algorithms are suitable tools to determine the optimum solutions of the engineering problems. But, their applications are limited by the high computational cost of the slow convergence rate. In order to deal with the deficiency of the global optimization methods, hybrid algorithm based on the particle swarm optimization with passive congregation (PSOPC), the ant colony algorithm (ACO), and the harmony search (HS) approach. HPSACO, is developed. HPSACO utilizes a PSOPC algorithm as a global search, whereas the idea of the ACO functions as a local search, and updating the positions of the particles is performed by a pheromone-guided mechanism.

**VI. LITERATURE SURVEY**

The various optimization algorithms used for floorplanning-based design methodology are described below:

**A. Multi-Objective PSO (MOPSO) Algorithm**

In this paper author S. Lalwani in 2013 describes numerous problems encountered in real life that cannot be actually formulated as a single objective problem; hence the requirement of Multi-Objective Optimization (MOO) has arisen several years ago. Due to the complexities in such type of problems powerful heuristic techniques were needed, which has been strongly satisfied by Swarm Intelligence (SI) techniques. Particle Swarm Optimization (PSO) has been established in 1995 and became a very mature and most popular domain in SI. Multi-Objective PSO (MOPSO) established in 1999, become an emerging field for solving MOOs with a large number of extensive software, variants, literature, applications and codes. This paper reviews all the applications of MOPSO in miscellaneous areas followed by the study on MOPSO variants [1].

**B. Memetic Programming Approach**

This process is provided by Dr. R. Vararatharajan in 2012. The classical floorplanning that usually handles only block packing to minimize silicon rate, therefore, modern floorplanning could be formulated as a fixed outline floorplanning. Whereas it uses some algorithms such as B-TREE representation, other being adaptive fast simulated annealing plus simulated annealing, on comparing above three algorithms the better efficient solution came from adaptive fast simulated annealing, which leaded to faster and more stable convergence to the desired solutions of the floorplan, but the results are not an optimal solution, for getting an optimal solution it’s necessary to choose effective algorithm. Summing global
and local search is a strategy used by many optimization strategies. Memetic algorithm is an evolutionary algorithm that includes one or more local search phases within its evolutionary phase. The algorithm combines a hierarchical design technique, constructive techniques, genetic algorithms and advanced local search to solve VLSI floorplanning problem[5].

C. Hybrid Genetic Algorithm

Floorplanning is the first stage of the very large scale integrated-circuit (VLSI) physical design technique, in this the resultant quality of this stage is very important for successive design stages. If we see this from the computational point of view, we conclude VLSI floorplanning is an NP-hard problem. In this paper, Jianli Chen in 2010, a hybrid genetic algorithm (HGA) for a non-slicing and hard-module VLSI floorplanning problem is presented. HGA uses an effective genetic search method to explore the search space and an efficient local search method to exploit information in the search domain. Experimental results on MCNC benchmarks show that the HGA is effective and promising in building block layout application[7].

D. Standard Cell Placement Techniques

Standard Cell Placement Techniques provided by Aaquil Bunglowala in 2008 are performance evaluation and comparison techniques for VLSI design. Heuristic approach is preferred as a solution to optimization of Non-Deterministic Polynomial hard (NP-hard) problems of sizes that are nontrivial because of speed limitations of exact optimization techniques. This paper, therefore, proposes to investigate recent heuristic techniques for solving the standard cell placement problems at physical design stage of VLSI design phase. The techniques considered are Simulated Annealing (SA), Hopfield Neural Network and Genetic Algorithm (GA). In addition to individual studies of the methods, a comparison in terms of solution quality and computing speed in connection with the standard cell placement problems has been done[15].

E. Genetic Algorithm and PSO

This paper proposed by Russell C. Eberhart in 1998 compares two evolutionary computation paradigms: genetic algorithms and particle swarm optimization algorithm. Operators of each paradigm are reviewed, on focusing how each affects search behavior in the problem domain. The goals of the paper are to provide additional insights into how each paradigm performs and to suggest ways in which performance might be improved by incorporating features from one paradigm into the other[23].

F. Immunity Based Genetic Algorithm

The genetic algorithm (GA) paradigm is a search procedure proposed by Isao Tazawa in 1996 for combinatorial optimization problems. As in most of other optimization techniques, the GA searches the solution space using a population of solutions. Whereas GA has an excellent global search performance, it is not effective for searching the solution space locally due to crossover-based search, and the diversity of the population sometimes decreases rapidly. Therefore to overcome these drawbacks, we propose new algorithm called Immunity based GA (IGA) combining features of Immune System (IS) with GA. Experimental results show that IGA performs better than GA[24].

VII. SUMMARY OF VARIOUS OPTIMIZATION ALGORITHMS

In the following Table, contains all optimization algorithms that are explained previously and also contains the method involved, their comparisons with other optimization algorithms, along with the drawbacks. The table containing all these is shown below:

<table>
<thead>
<tr>
<th>METHOD</th>
<th>OA USED</th>
<th>COMPARED</th>
<th>DRAWBACKS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memetic programming approach</td>
<td>Memetic algorithm</td>
<td>Simulated annealing</td>
<td>MA leads to faster &amp; stable convergence</td>
</tr>
<tr>
<td>GA &amp; PSO</td>
<td>GA</td>
<td>PSO</td>
<td>Performance might be enhanced by incorporating features from one paradigm into the other</td>
</tr>
<tr>
<td>Standard Cell Placement Techniques</td>
<td>Simulated Annealing</td>
<td>Hopfield neural network</td>
<td>% deviation decreases as the no. of cells and complexity increases</td>
</tr>
<tr>
<td>Immunity based GA</td>
<td>IGA</td>
<td>GA</td>
<td>IGA provides better solutions with higher probability as compared to GA</td>
</tr>
<tr>
<td>Hybrid Genetic Algorithm</td>
<td>HGA</td>
<td>GA,MA</td>
<td>HGA is effective and promising in building block layout application But, the runtime of MA is much longer than HGA.</td>
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</table>
VIII. CONCLUSION

VLSI design processes are such that own special circuits of considerable complexity can be designed by system engineers. This provides an improved degree of freedom for designers. Heuristic algorithms are suitable tools to determine the optimum solutions of the engineering problems. But, their applications are limited by the high computational cost of the slow convergence rate. The various optimization algorithms used for floorplann-based design methodology have been reviewed.

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