Comparison of 1 Bit Low Power-High Speed Designs Leakage Minimization Full Adder

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Abstract—Low power design has become one of the primary focus in Deep sub-micron technology (DSM). Optimization of speed, power & area can be achieved by using Gated Diffusion Input (GDI) technique. In paper a 11T based Adder with 8 & 16 input using GDI technique is proposed and it compared with various existing adder circuit for Average power, delay, Power delay product (PDP). Simulations are performed by using Cadence Virtuoso based on 180nm CMOS technology. Area has been evaluated by Microwind using TSMC BSIM 0.120μm technologies. In comparison with 28T, 10T, GDI, 8T adder cell module, the proposed adder cells demonstrate their advantages, including lower power consumption, higher speed and lesser delay. A comprehensive study and analysis of various Adder circuits have been presented in this paper a novel adder is developed which reduces the Average Power.

Keywords— Dual- Leakage power, GDI, SERF, tri-state inverters.

I. INTRODUCTION

It is time we explore the well-engineered deep submicron CMOS technologies to address the challenging criteria of these emerging low-power and high-speed communication digital signal processing chips. The performance of many applications as digital signal processing depends upon the performance of the arithmetic circuits to execute complex algorithms such as convolution, correlation, and digital filtering. Fast arithmetic computation cells including adders and multipliers are the most frequently and widely used circuits in very-large-scale integration (VLSI) systems. The semiconductor industry has witnessed an explosive growth of integration of sophisticated multimedia-based applications into mobile electronics gadgetry since the last decade. However, the critical concern in this arena is to reduce the increase in power consumption beyond a certain range of operating frequency. Moreover, with the explosive growth, the demand, and the popularity of portable electronic products, the designers are driven to strive for smaller silicon area, higher speed, longer battery life, and enhanced reliability. The XOR-XNOR circuits are basic building blocks in various circuits especially arithmetic circuits (adders & multipliers), compressors, comparators, parity checkers, code converters, error-detecting or error-correcting codes and phase detector. The semiconductor industry has witnessed an explosive growth of integration of sophisticated multimedia-based applications into mobile electronics gadgetry since the last decade. However, the critical concern in this arena is to reduce the increase in power consumption beyond a certain range of operating frequency. Moreover, with the explosive growth, the demand, and the popularity of portable electronic products, the designers are driven to strive for smaller silicon area, higher speed, longer battery life, and enhanced reliability. The XOR-XNOR circuits are basic building blocks in various circuit especially arithmetic circuits (adders & multipliers), compressors, comparators, parity checkers, code converters, error-detecting or error-correcting codes and phase detector.

To reduce the power consumption different logic design techniques like CMOS complementary logic, Pseudo NMOS, Dynamic CMOS, Clocked CMOS logic (C2MOS), CMOS Domino logic, Cascade voltage switch logic (CVSL), Modified Domino logic, Pass Transistor Logic (PTL) have been proposed [1-3]. Although Static CMOS Logic has been the most popular design approach for the past three decades, many attempts have been made to propose a better alternative to achieve lower power dissipation, smaller area and better performance reported in [4-5]. Circuit designed with transmission gate (TG) solves the problem of low logic level swing by using PMOS as well as NMOS but this implementation needs true and complemented control signal and requires more area than pass transistor logic. Pseudo-NMOS is simple and fast but reduces noise margins and increases power consumption. Pass-transistor logic is good for certain classes of circuits (MUX/adders). On the other hand, PTL implementations of logic gates such as NANDs and NORs were found to be slower and consume more power than CMOS implementations mainly because of the reduced output swings due to the threshold drop across a single-channel pass transistor.

The organization of the paper is as follows: The section II, describes Literature Survey work which consist of 28T, SERF, GDI, 8T Adder circuit. Section III, presents Proposed Methodology of full adders. Section IV deal with problem formulation. Section V presents simulation result using Cadence EDA. Finally the conclusion is presented in section VI.

II. LITERATURE SURVEY

A digital signal full adder cell is defined as a logical cell that performs an addition operation on three one-bit binary numbers. This cell produces a two-bit output which is carry and Sum. Full Adder cell is implemented in low
power and high performance data path circuit and complex communication systems [6]. In over survey we have seen the behavior of different adder circuit we have taken the conventional 28T adder and measure the response of the circuit. A close observation of the FA shows that \( C_{out} = A \) for six out of eight cases. Similarly, \( C_{out} = B \) for six out of eight cases. Since A and B are interchangeable, we consider \( C_{out} = A \). Thus, we propose a fourth approximation where we just use an inverter with input A to calculate \( C_{out} \) and Sum is calculated similar to approximation 1. This introduces two errors in \( C_{out} \) and three errors in Sum. In all these approximations, \( C_{out} \) is calculated by using an inverter with \( C_{out} \) as input.

A. Gate Diffusion Input (GDI)

The basic primitive of GDI cell consists of NMOS and PMOS as shown in Fig.2. A basic GDI cell contains four terminals – G (common gate input of NMOS and PMOS transistors), P (the outer diffusion node of PMOS transistor), N (the outer diffusion node of NMOS transistor), and D (common diffusion node of both transistors) [7]. Table 1 show how a simple change of the input configuration of the simple GDI cell corresponds to different Boolean functions. Referring to Table1 most of the functions are realized using the function F1 and F2 since they are possible to realize using CMOS p-well process.

![Fig.1. Symbol of GDI cell](image)

<table>
<thead>
<tr>
<th>N</th>
<th>P</th>
<th>G</th>
<th>Out</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>B</td>
<td>A</td>
<td>( \overline{A}B )</td>
<td>F1</td>
</tr>
<tr>
<td>B</td>
<td>1</td>
<td>A</td>
<td>( \overline{A+B} )</td>
<td>F2</td>
</tr>
<tr>
<td>1</td>
<td>B</td>
<td>A</td>
<td>( A+B )</td>
<td>OR</td>
</tr>
<tr>
<td>B</td>
<td>0</td>
<td>A</td>
<td>( AB )</td>
<td>AND</td>
</tr>
<tr>
<td>C</td>
<td>B</td>
<td>A</td>
<td>( \overline{AB+AC} )</td>
<td>MUX</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>A</td>
<td>( \overline{A} )</td>
<td>NOT</td>
</tr>
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Table 2. Logic function implemented with mgdi technique

<table>
<thead>
<tr>
<th>N</th>
<th>P</th>
<th>G</th>
<th>Out</th>
<th>Function</th>
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<tbody>
<tr>
<td>A</td>
<td>B</td>
<td>B</td>
<td>( A+B )</td>
<td>OR</td>
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<tr>
<td>B</td>
<td>A</td>
<td>A</td>
<td>( AB )</td>
<td>AND</td>
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<tr>
<td>B</td>
<td>A</td>
<td>C</td>
<td>( \overline{CA+CB} )</td>
<td>MUX</td>
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<tr>
<td>0</td>
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<td>A</td>
<td>( \overline{A} )</td>
<td>NOT</td>
</tr>
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</table>
The overall area and complexity of the circuit is minimized using GDI technique. Also improvements are observed in static power dissipation and logic level swing. Most of the functions which are complex (6-12 transistors) in CMOS, are very simple (only 2 transistors per function) in GDI design method.

**B. Static Energy Recovery Full Adder (SERF)**

As an initial step toward designing low power arithmetic circuit modules, we designed a Static Energy Recovery Full adder (SERF) cell module. The cell uses only 10 transistors and it does not need inverted inputs. The design was inspired by the XNOR gate full adder design [10]. In non-energy recovery design the charge applied to the load capacitance during logic level high is drained to ground during the logic level low. It should be noted that the new SERF adder has no direct path to the ground. The elimination of a path to the ground reduces power consumption, removing the $P_{sc}$ variable (product of $I_{sc}$ and voltage) from the total power equation. The charge stored at the load capacitance is reapplied to the control gates [11]. The combination of not having a direct path to ground and the re-application of the load charge to the control gate makes the energy recovering full adder an energy efficient design. To the best of our knowledge this new design has the lowest transistor count for the complete realization of a full adder.

![Fig.3. Schematic of SERF Full Adder](image)

**C. 8 T Full Adder Circuit**

The basic of 8T full adder consists of 3 modules: 2 XOR elements and a Carry. The Sum output is obtained by two XOR blocks in succession. For the carry section GDI based 2TMUX is used and $(A \ XOR \ B)$ as the selection signal. The Sum and the $C_{out}$ module need 6 and 2 transistors respectively [11]. The transistor level implementation of the eight transistor full adder. It is obvious from the figure that both SUM and $C_{out}$ has a maximum delay of 2T. It doesn’t suffer from threshold voltage loss problem. Also the noise margin has been substantially increased by proper sizing of transistors in 3T XOR. The power delay product (PDP), and the area of the proposed adder are also found better than that of the existing.

**III. PROBLEM FORMULATION**

Adder is the basic building block for the arithmetic operation done in sequential circuit; thousand of operation is done in microseconds, So over main aim is to develop adder circuit which take less time for extraction of the bit. So to enhance the speed of the microprocessors we develop fast adder which occupy lesser area, so more No of Adder circuit can be fabricated on single chip. Area, Power and Delay are the Main problem Consent to the adder circuit to enhance the speed and performance of the adder circuit. We mainly focus on the area of power, delay and Area of the circuit should be mitigate to enhance the speed of the processor.

**IV. PROPOSED METHODOLOGY**

In this section we introduce a novel Low-Power Full Adder, which has good characteristic in term of speed and power. The circuit of 11T adder is a one-bit full adder core has three inputs ($A, B, C_{in}$) and two outputs (Sum S and Carry $C_{out}$). The adder is made of three CMOS inverter. Input A is directly connected to first inverter & Input B is connected to parallel PMOS network. The output of the first inverter generate compliment of $C_{out}$ and SUM Compliment is generated with the help of $C_{out}$ which is feed to the second inverter, $C_{in}$ is feed to the third inverter so as to generate the SUM.

**V. SIMULATION ANALYSIS**

The Power Consumption of proposed circuit is remarkable reduced than the other Approach at 180nm technology with supply voltage of 1.8v. The circuit is simulated at the temperature of 27ºC. All transistor have minimum length ($L_{min}$=180nm according to used technology), while their width are typically design parameters. In order to prove that which designs consume less power and have high performance, Simulation is carried out for Power, delay and PDP.
VI. CONCLUSION

Adder circuits are basically used to implement wide Arithmetic circuits. Adder are used in Dynamic RAMs, Static RAMs, high speed processors and other high speed circuits and GDI reduces the area of the Arithmetic circuits. For low-leakage and high-speed circuit concern should be on both the factor speed and power this paper concluded with the efficient approach of Adder Circuit at 180nm technology. A novel low-power 1-bit full-adder cell can be further implemented. Low power consumption is target at the circuit-design level in this paper first we have determined Average Power with respect 28T 93.25%, GDI 59.16%, SERF 64.09%, & 8T 85.28 % of Average Power is Saved. From proposed circuit we can implement 8-Bit & 16-Bit full adder and Mitigate the average Power consumption and enhance the speed of the circuit.

REFERENCES


