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Radiation Effect on MOSFET at Deep Submicron Technology

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Abstract: ***MOSFET is the basic component of VLSI and ULSI circuits. In fact, MOSFET finds application in the instrumentation part of any electronic system. Large packing density, low noise and low power requirement make MOS transistors superior to bipolar junction transistors. Unfortunately, MOS devices are susceptible to degradation in presence of ionizing radiation. Exposure to high radiation dose may lead to permanent failure of these devices. Conventional MOSFET can survive 3-10 krad (Si) of total dose without much parametric degradation. However, ionizing radiation dose in excess of 50 krad (Si) may turn out to be detrimental to proper functioning of the device. The space environment is hostile to most integrated electronic components such as those for navigation, communication, data processing function in satellites and various space missions. The radiations generally encountered in space are α-, β-, γ- , x-ray, energetic electrons, protons, neutrons and ions of various kinds are prevalent in space and have potential to cause various transient or fatal device damages. It is therefore necessary to study the performance of MOSFET in presence of nuclear radiation to devise ways and means for developing radiation hardened devices. Earlier the size of MOSFET was very large, but due the advancement in technology the size of MOSFET is reducing. The size of MOSFET is measured by its channel length. In deep sub micron technology, the channel length of MOSFET reduces from .35 micrometer to .25 micro meters. In this paper, a semiemperical analytical model of MOSFET is developed and implemented in MATLAB at deep sub micron technology. Various short channel effects are studied at deep submicron technology and various radiation effects on MOSFET are analyzed which degrades the electrical parameters of the MOSFET.***

Keywords: MOS, ULSI, VLSI, radiation effect.

I. INTRODUCTION : MOSFET and ITS PARAMETERS

A. METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET)

The metal–oxide–semiconductor field effect transistor (MOSFET) or insulated–gate field effect transistor (IGFET) is the main subject of interest, since it is acting as a prevailing device in microprocessors and memory circuits, and has been the prominent device for ICs over the past four decades. In addition, the MOSFET is increasingly used in areas as diverse as mainframe computers and power electronics mainframe computers and power electronics. The MOSFET shown in Fig.1 is an n-channel device, which uses contacts to the substrate. The MOS transistor consists of a semiconductor substrate (usually silicon) on which is grown a thin layer of insulating oxide (Sio_2,) of thickness t_{ox}, (80-l000A). On the top of the oxide, a conducting layer (a metal or heavily doped polysilicon) called the gate electrode is deposited. Two heavily doped regions of depth X_j (0.l - l.0μm), called the source and the drain are formed in the substrate on either side of the gate. The source and the drain regions are overlapped slightly with the gate (see Figure1). The distance L between the n^+ source-drain edges is called channel length [1]. The distance W to which the device is extended in the lateral direction (i.e. into and out of the page) is called channel width. The device width to length ratio (W/L) is known as the aspect ratio which is normally used as a design parameter that can be varied to set the desired drain-source conduction properties of the MOSFET. The region between the source and drain junctions is called the channel region.

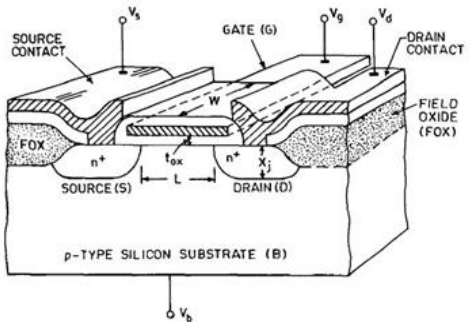

Fig.1 Schematic diagram of a MOSFET [2]

Thus a MOS transistor is essentially a MOS structure, called the MOS capacitor, with two pn junctions on either side of the gate**.** Under normal operating conditions, a voltage V, applied to the gate terminal creates an electric field that controls the flow of the charge carriers in the channel region between the source and the drain. The device is known as a MOS Field-Effect-Transistor (MOSFET) device because the current is controlled by the electric field (vertical field due to the gate voltage and lateral field due to the source to drain voltage). The gate is electrically isolated from the other electrodes, so this device is also called an Insulated-Gate Field-Effect Transistor (IGFET). Another short form sometime used is MOST for the MOS Transistor.

Earlier the size of MOSFET was very large but as technology advances, the feature sizes of MOS transistors are reduced continuously to increase the packaging density of VLSI circuits [3]. CMOS processes are characterized by the minimum allowed channel length (e.g.in a 0.13 μm technology, L min = 0.13 μm). The trend is to reduce L min in order to increase the transistor density, as well as to operate at higher speeds or, in analogue terms, over a wider bandwidth. The gate oxide thickness decreases and, as a consequence, the oxide capacitance (C_{ox}) increases as an effect of scaling. De-spite the variation of the surface mobility, the current parameter, and $k = \mu C_{ox}$, has been steadily increasing because of scaling. Hence, modern submicron devices achieve higher transconductance at the same overdrive voltage. The threshold voltage (V_T) decreases with L min, but the reduction has not been as large as that of the power supply (which was reduced dramatically from 5 V, for the 1 μm CMOS technology, to about 1.8 V, for the 0.35 μm process).

B. MOSFET PARAMETERS:

Although continuous technology improvements and shrinking of MOSFET size have resulted in a more complicated structure, which has its effect on modeling, the essential structure remains the same. Some of the important parameters are as follows:

Mobility: The carrier mobility of electrons and holes, u_n and u_p is a measure of the ease of motion of the electrons and holes within the semiconductor crystal.

Threshold voltage: One of the important parameter of the MOSFET is the threshold voltage. It is a measure of device performance in switching applications. Threshold voltage also called turn–ON or switching voltage is the bias voltage necessary on the gate to form the inversion layer at the silicon surface beneath the gate, which constitute the conducting path between the source and the drain.

Drain current: The drain current is most important device parameter of the field effect device MOSFET to evaluate the current performance of driver circuitry. When the inversion region is formed under the gate, current can flow from drain to source (for an n-channel device) on application of drain voltage.

Transconductance: Under normal operation, a voltage applied to gate , drain or substrate result in a change in the drain current .The ratio of change in the drain current to the change in the gate voltage while keeping drain and substrate voltages constant is called gate transconductance or simple transconductance $g_{m\ i.e.}$

for

$V_{D,}$ linear region

for

, Saturation region

II. INTRODUCTION of RADIATION ENVIRONMENTS

For military applications and space missions it is obvious that there is a radiation-harsh environment. The amount of radiation that the semiconductor devices and materials encounter during their lifecycle strongly depends on the radiation environment and their operating conditions. However, also during their fabrication process and even for standard terrestrial operation the devices may suffer from ionizing radiation.

In general, one can differentiate between the following different environments [4]

a) Space environments
b) High-energy physics experiments
c) Nuclear environments
d) Processing-induced radiation

In predicting the response of a MOS device to ionizing radiation, it is necessary to determine the amount of energy deposited by the radiation in the material. Ausman and McLean [5] followed by Benedetto and Boesh [6] determined that, on the

average, each 18 eV of energy deposited in the oxide by the ionizing radiation would result in the formation of an electron–hole pair. These radiation-induced electrons are much more mobile than the holes and are swept out of the oxide layer. The holes which are relatively immobile cause a negative shift of the flat-band voltage on the electrical characteristics of MOS devices. Fig.2 shows that the part of the MOS structure which is sensitive to ionizing radiation is the silicon dioxide.

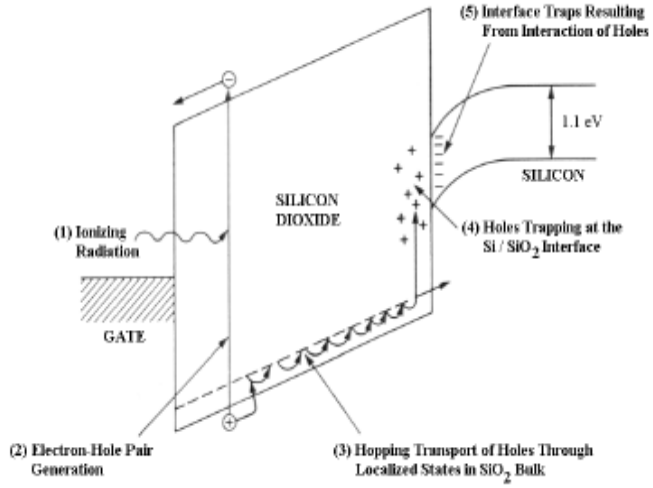

Fig.2: Schematic illustration of the effects induced by ionizing radiation in an MOS device [7]

In the gate (metal or polysilicon) and in the substrate the electron-hole pairs quickly disappear, since these are materials of little resistance. On the contrary in the oxide, which is an insulator, electrons and holes have different behaviors, as their nobilities differ by five to twelve orders of magnitude. A fraction of the radiation-induced electron-hole pairs will recombine immediately after being created. The electron-hole pairs which do not recombine are separated in the oxide by the electric field and, for example in the case of a positive bias applied to the gate, the electrons drift to the gate in a very short time (order of picoseconds) whereas the holes move towards the SiO_2-Si interface with a very different characteristic transport phenomenon. Close to the interface, but still in the oxide, some of the holes may be trapped, giving origin to a fixed positive charge in the oxide. The generation, transport and trapping of holes in the oxide will be treated in more detail. Ionizing radiation also induces the creation of traps at the SiO2-Si interface when the gate is positively biased.

III. CONSEQUENCES of RADIATIONS on the ELECTRICAL PARAMETERS of MOSFET:

Following are the effects of radiations on the MOSFET parameters:

a) **Threshold Voltage Shift**

The threshold voltage of a MOS transistor changes when the device is irradiated. The change ΔV_T is given by the sum of two contributions, ΔVox and ΔNit, which are related to the hole trapping in the silicon dioxide and to the charge state of the interface traps. Charges trapped in the oxide give origin to a shift in the flat-band voltage, and therefore in the threshold voltage, which can be expressed as

$$= (X)\, dx$$

Where t_{ox} is the gate oxide thickness, C_{ox} is the capacitance per unit area and (x) is the charge distribution in the oxide per unit volume as a function of the distance from the gate oxide interface x. The first observation one can make from this expression is that the voltage shift due to this contribution is negative when the charge is positive (as it is in the reality).

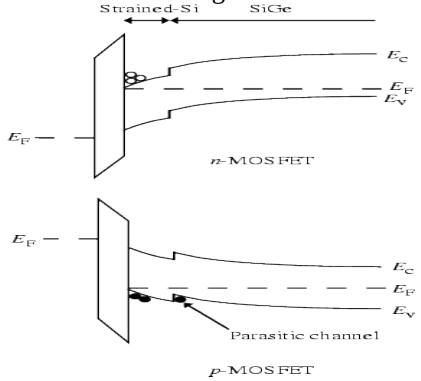

Fig.3 Energy bands diagrams in the silicon for an n-channel and a p-channel transistors [7]

The threshold voltage shift component associated with the radiation induced interface states ΔN_{it} can be treated as before.
Where kg is the number of electron-hole pairs produced per unit dose, f_y is the probability that an electron-hole pair escapes recombination, D (E) is the incident radiation dose shown as a function of energy (E) and fit is the number of interface-trapped charges created per radiation-induced electron –hole pair.
We assume that the traps above mid-gap are acceptor-like and those below are donor-like. This means that for an n-channel transistor (for example), where the Fermi level in the silicon close to the silicon-oxide interface lies between E_i and E_c, the acceptor-like traps which are below the Fermi level will be negatively charged, and then the threshold voltage shift will be positive. Similarly for a p-channel the threshold voltage shift will be negative. Fig.3 shows the behavior of the interface traps in two typical cases (gate bias, referred to the substrate, positive for the n-channel transistor and negative for the p-channel).

b) **Increase of Sub-threshold Currents**

The "off-state" current is the current which flows from drain to source when $V_{GS} = 0$, and is sometimes referred to as "leakage current" in a MOS transistor. In an irradiated n-channel transistor two effects lead to an increase in the "off-state" current: the increase of the sub-threshold current and the generation of parasitic currents.

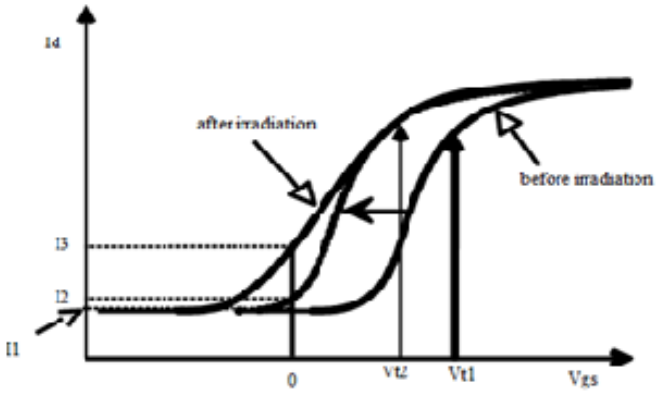

Fig.4: Increase of the sub-threshold current in a n-channel transistor given by a decrease in the threshold voltage and in the sub -threshold slope [3].

These phenomena can be critical for many applications, as for example when the transistor is used as a switch. The increase in the sub-threshold current is related to two factors, illustrated in figure4. The first is the decrease of the threshold voltage. The pre-irradiation solid line in fig.4 shifts towards the y axis (V_T goes from V_{T1} to V_{T2}) and becomes the dotted line after irradiation. The second is the radiation-induced decrease of the sub-threshold slope; due to this effect the dotted line becomes the solid one after irradiation in Figure4.The sub-threshold current which before irradiation was I_1 becomes therefore I_2 due to the threshold voltage shift and then I_3 due to the sub-threshold slope decrease.

IV. DEVICE MINIATURIZATION

In the past 40 years with the success story of downscaling, silicon transistors have became smaller and smaller in accordance to Moore's law [8], which predicted a decrease in feature size by a factor of 0.7 every years. This made the chips faster by 15-30% per year, reduced power consumption and allowed the increase of DRAM (Dynamic Random Access Memory) integration by 4 times at reduced cost today, the minimum gate length of the most advanced transistor in production is about 28nm, and it is projected to be 5nm by 2020[9], thus allowing more devices per unit area on a single chip. Why is device miniaturization necessary? Obviously, the objective is to deliver high performance at low cost as shown in the fig.5:

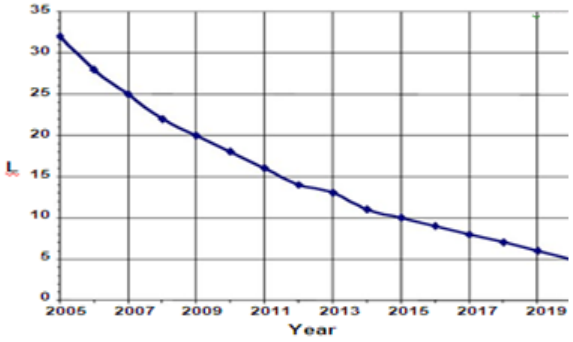

Fig.5 Gate length (in micron) scaling [1]

It results in reduced unit cost per function and in enhanced performance. Smaller circuit dimensions reduce the overall chip area thereby allowing more transistors to be fabricated on a single chip without imparting the chip manufacturing cost. On decreasing, the MOSFET dimension the MOSFET dimensions, the intrinsic switching time of devices decrease linearly. This is because the intrinsic delay time=channel length /carrier velocity. Thus, performance measured as speed of operation is improved. Another advantage is the reduction of power consumption which is not only useful for mobile systems (such as mobile handsets, notebook computers implantable medical devices and other portable devices) to lengthen battery life, but also for improving reliability of high performance systems.

A. **Scaling**

During the last two decades, MOS transistors have been systematically scaled down in dimensions in order to achieve increased circuit density (more circuit functions in a given silicon area) and higher performance (higher switching speed, lower power dissipation, etc).

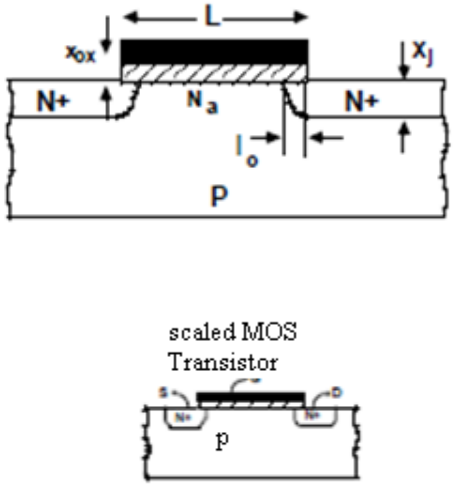

Fig.6 Shows MOSFET Device Scaling [1]

Rules of scaling were first proposed by Dennard et al [10-11]. With the idea of reducing the device dimensions while still maintaining the current-voltage behavior of a large device. According to this rule, all horizontal and vertical device dimensions (i.e., device length L, width W, gate-oxide thickness t_{ox}, and source drain junction depth X j*)* as well as voltages are scaled down by a factor X > 1, called the scaling factor**,** while the doping concentration *N***,** and is increased by the same factor. This scaling rule, often known as classical or constant field scaling**,** results in electric fields inside the device that are unchanged compared to the un-scaled or original device. The effect of keeping the electric field unchanged in the scaled device is to avoid undesirable high field effects such as mobility degradation, impact ionization, hot-carrier effect etc.

B. **Effect of Device downscaling:**

Downscaling has been manifested by the four main IC technology-generations that formed up: micron, submicron, deep submicron and very deep submicron. At the same time plenty of limiting factors, as short-channel and quantum effects, accompany this technology evolution and strongly affect the device operation since numerous characteristics and measurable parameters of the MOSFET (such as the surface potential, the drain current, the trans-conductance and the trans-capacitance, etc.) change. All these effects directly reflect the complexity of device models causing numbers of physical, mathematical and computational problems. Lithography is one of the key technologies that enable Moore‘s law. Continued improvements in optical projection lithography have enabled the printing of ever finer features, the smallest feature size decreasing by about 30% every two years. The deep submicron technology started in 1995 with the introduction of lithography better than 0.35 µm. There are various types of effects studied during down scaling the device which are as follows:

a) **Short Channel Effects**

A MOSFET device is considered to be short when the channel length is the same order of magnitude as the depletion-layer widths (xd_D, xd_S) of the source and drain junction. As the channel length *L* is reduced to increase both the operation speed and the number of components per chip, the so-called short-channel effects arise. The short-channel effects are attributed to two physical phenomena: the limitation imposed on electron drift characteristics in the channel and the modification of the threshold voltage due to the shortening channel length Thus, in order for the MOSFET to work as a component of

VLSI/ULSI, the suppression of short-channel effects is the first priority in the designing of the MOSFET, which can be done by proper scaling of device dimensions MOSFET.

b) **Punch through effect:**

If the channel length becomes too short, the depletion region from the drain can reach the source side and reduces the barrier for electron injection. This is known as punch through effect.

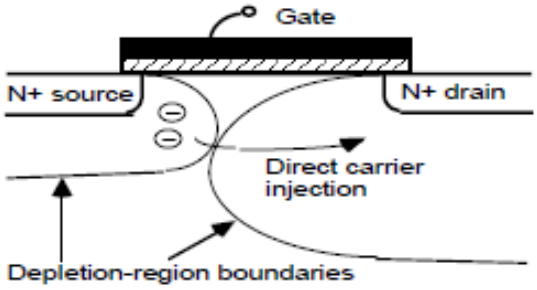

Fig.7 Shows a punch through phenomena [3]

c) **Mobility reduction**

As the channel length becomes smaller due to the lateral extension of the depletion layer into the channel region, the longitudinal electric field component Ey increases, and the surface mobility becomes field-dependent. Since the carrier transport in a MOSFET is confined within the n inversion layer, and the surface scattering (that is the collisions suffered by the electrons that are accelerated toward the interface by ex) causes reduction of the mobility, the electrons move with great difficulty parallel to the interface, so that the average surface mobility, even for small values of E_y, is about half as much as that of the bulk mobility.

d) **Threshold rolls off**

The equation giving the threshold voltage at zero-bias is accurate in describing large MOS transistors, but it collapses when applied to small-geometry MOSFETs. In fact that equation assumes that the bulk depletion charge is only due to the electric field created by the gate voltage, while the depletion charge near n+ source and drain region is actually induced by pn junction band bending.

Therefore, the amount of bulk charge the gate voltage supports is overestimated, leading to a larger V_T than the actual value. The electric flux lines generated by the charge on the MOS capacitor gate electrode terminate on the induced mobile carriers in the depletion region just under the gate. For short-channel MOSFETs, on the other hand, some of the field lines originating from the source and the drain electrodes terminate on charges in the channel region. Thus, less gate voltage is required to cause inversion. This implies that the fraction of the bulk depletion charge originating from the pn junction depletion and hence requiring no gate voltage must be subtracted from the V_T expression.

e) **Channel length modulation**

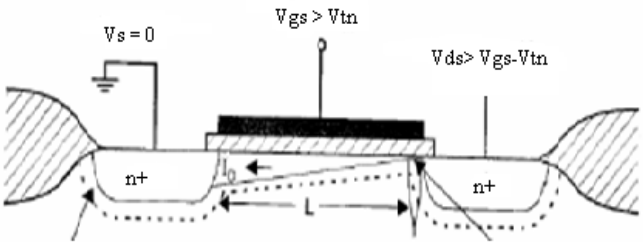

Fig.8 Channel length modulation

It is a shortening of the length of the inverted channel region with increase in drain bias for large drain. In short channel the current does not stay constant but rather increases significantly when drain voltage exceeds $V_{D\,sat}$. This behavior results from channel length modulation

V. Methodology Used

In the beginning of the compact modeling era, there were four long-channel CMOS transistor models proposed for DC circuit simulation (or calculation). All the four models are based on the long-channel Gradual Channel Approximation (GCA). The four models are Bulk-Charge model, Square-Law model, Pao-Sah model and Charge-Sheet model.

Bulk-Charge model (Ihantola and Moll, 1964) and Square-Law model (simplified version of Bulk-Charge model) are only valid if the CMOS transistor is operated in strong inversion. This has limited the usage of these models. These two models do not yield a good MOSFET characteristics prediction with radiation effect at deep submicron technology and can have several disadvantages.

Pao-Sah model (Pao and Sah, 1966) is the first model that able to cover the entire range of CMOS transistor operation. This model retains the GCA but the drain current, Id equation requires numerical integration in two dimensions. Such numerical complexity has limited the role of this model for theoretical analysis of the CMOS transistor.

But we are trying to find the best method to analyze the modeling approaches that consider both radiation effect & short channel effect parameter. So, here a model is being presented that collectively combines both radiation effects & short channel effect at deep sub micron technology.

Charge-Sheet model (Brews, 1978) has become the most widely adopted long-channel CMOS model that is accurate in the inversion range [12]. Although the Charge-Sheet model allows Id to be calculated with much less computational effort than that of the Pao-Sah model, the computational effort for determining Id is still too great for most circuit simulation applications, and thus the Charge-Sheet model has not been incorporated into the popular circuit simulation engine, which is known as the SPICE simulator. Since the Charge-Sheet model is too complex to be used in most circuit simulation applications, an alternate analytical expression (simplified from the Charge- Sheet model) is implemented to be used in sub threshold region. Practically all the models used in today's circuit simulators fall into this category, and range from simple to more complex models. The advantage of these models is that they do describe the relationship between the physical process and geometry structure on the one hand and electrical behavior on the other, so that with some minor changes in the process, electrical behavior can still be predicted. However, the disadvantage is that they are technology dependent and takes considerable time to develop the model.

The current has two components: Drift and Diffusion

After integration, each of these components is given by:

We can complete the integration by using

After integration, we have

Where and can be numerically found from

Previous equations can be simplified if we approximate the depletion charge. Linear dependence on surface potential using a Taylor expansion around a choice of surface potential, e.g. ,

Strong inversion, (surface potential at source side)

Weak inversion, (surface potential when depletion charge is dominant)

Equations can be simplified if we approximate the charge linear sheet model on using Taylor expansion.

The current is given by:

Where V_P is the Pinch off voltage given by:

VI. Simulation Result

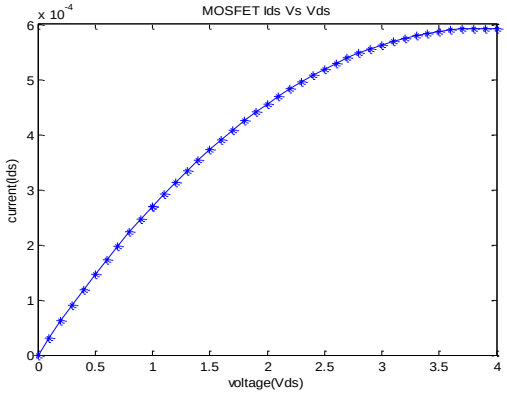

Fig.9 this waveform shows variation in Ids vs. V_{ds} at constant V_{gs}=4.0 V

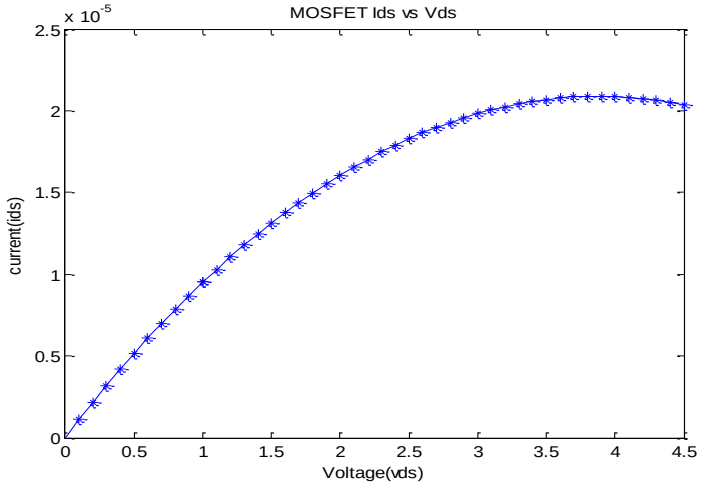

Fig.10 Varation of Ids and Vds at Constat Vgs=4.0V including mobility degradtion.This graph shows Ids reduction due to mobility degration.

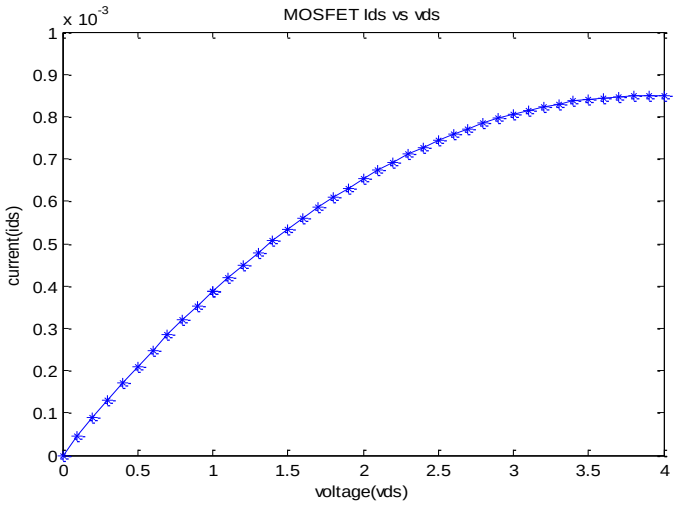

Fig.11 Varation in Ids and Vds at Constat Vgs=4.0 V including channel length modulation.This graph shows that Ids increases due to channel length modulation.

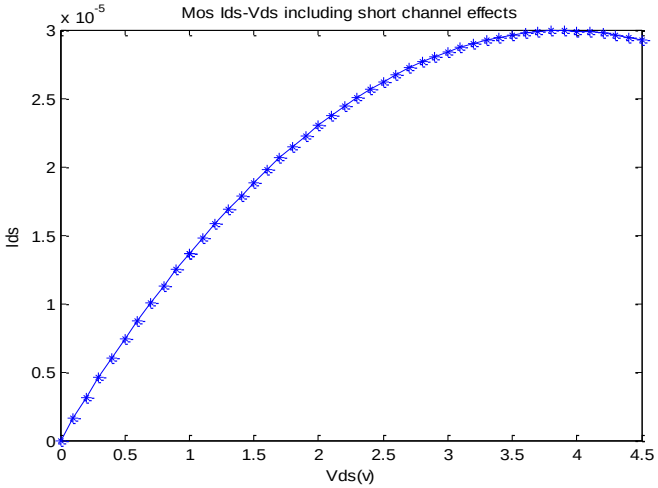

Fig.12 Shows Ids vs. Vds curve including short channel effects. This curve depicts that by including short channel effects drain current decreases.

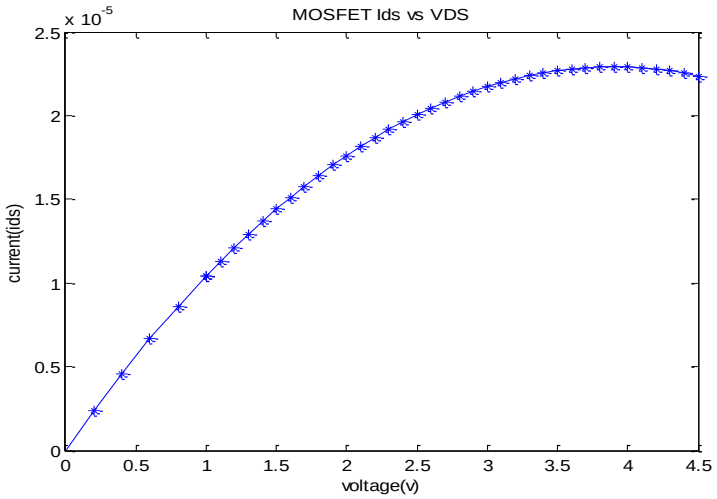

Fig.13 Shows I_{ds} vs. V_{ds} MOSFET characteristics with short channel effects and radiation effects.

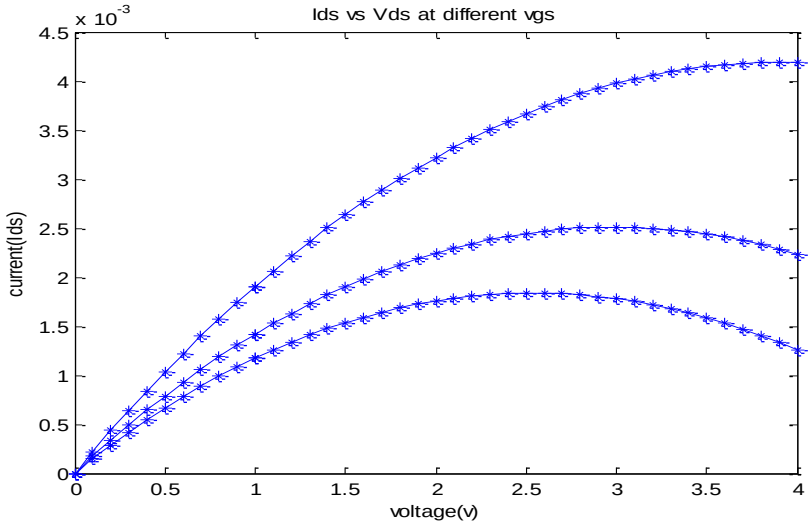

Fig.14 shows Drain-Current voltage characteristics at different V_{gs} 4V, 3V, 2.5V at 1 um technology including short channel effects

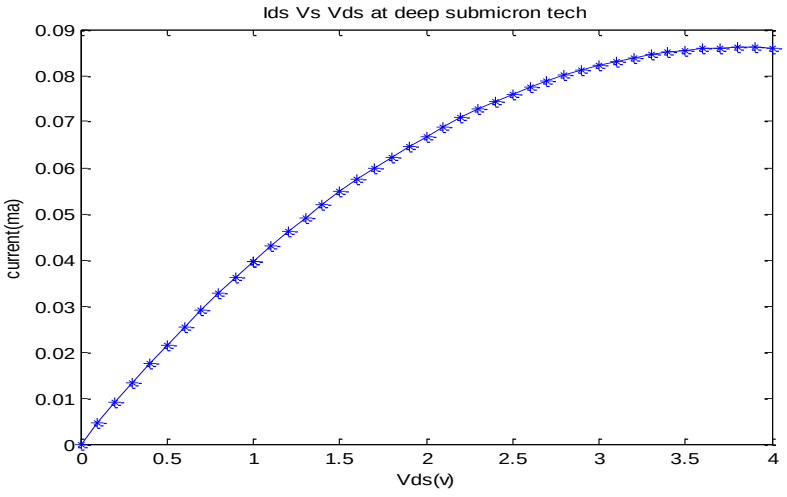

Fig.15 shows drain-current voltage characteristics at deep submicron technology. The value of current increases in deep submicron technology.

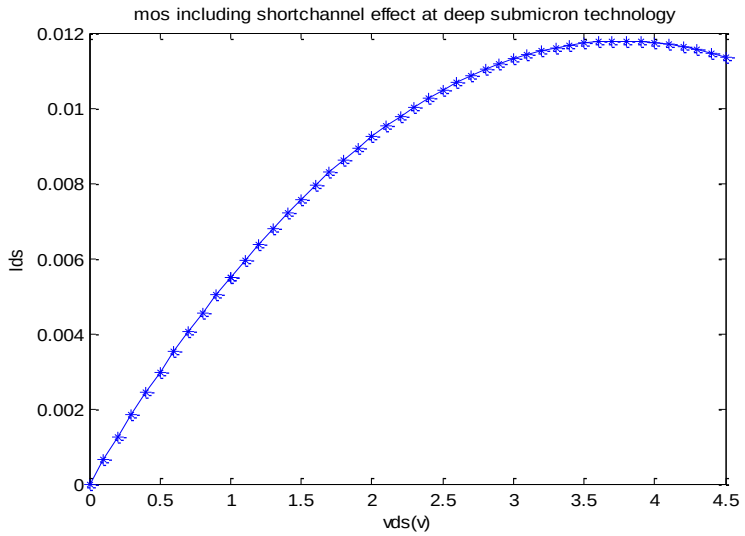

Fig.17 Shows drain-current voltage characteristics at deep submicron technology (.35 um) including short channel effect. The value of current decrease due to short channel effect.

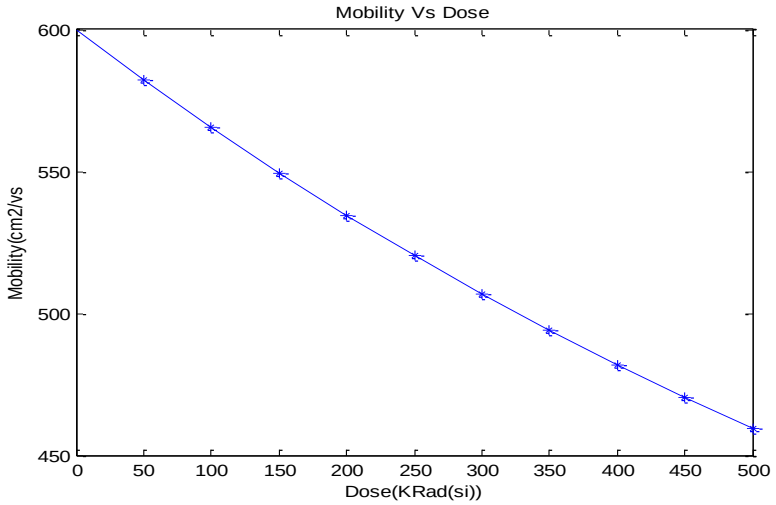

Fig.17 MOSFET mobility reduces with the increase in dose (Krad).

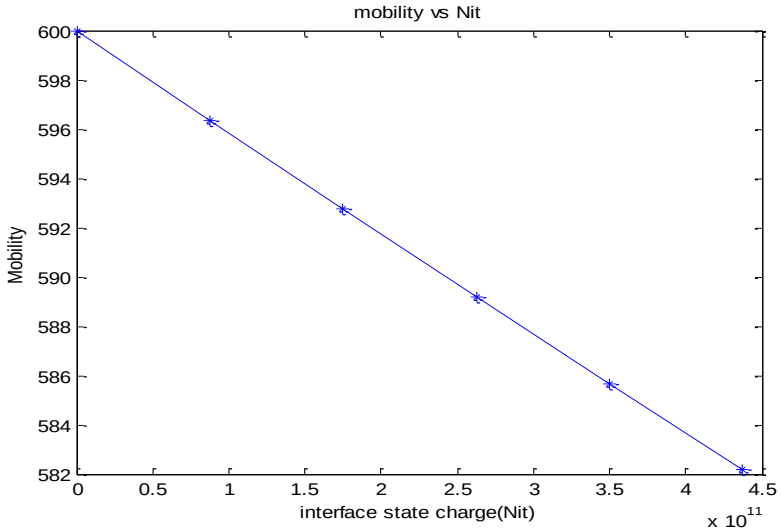

Fig.18 Show mobility vs interface trapped charges.

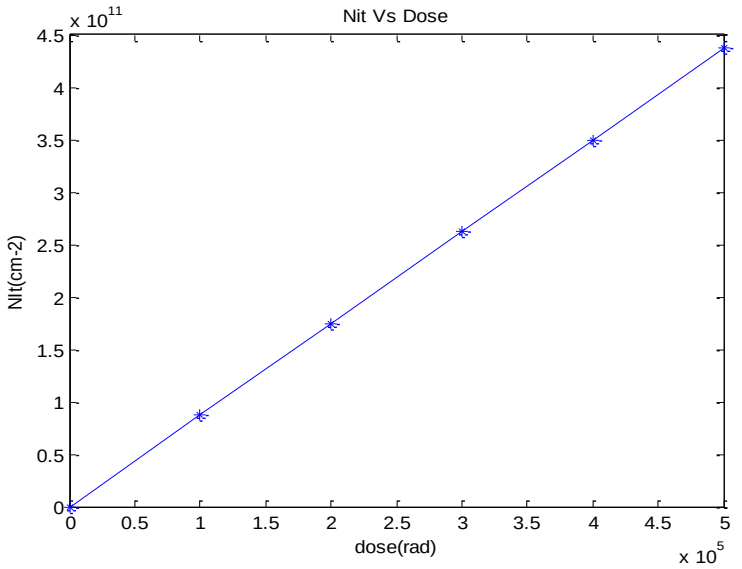

Fig.19 n-MOSFT Transistor variations in interface trap charge with mobility.

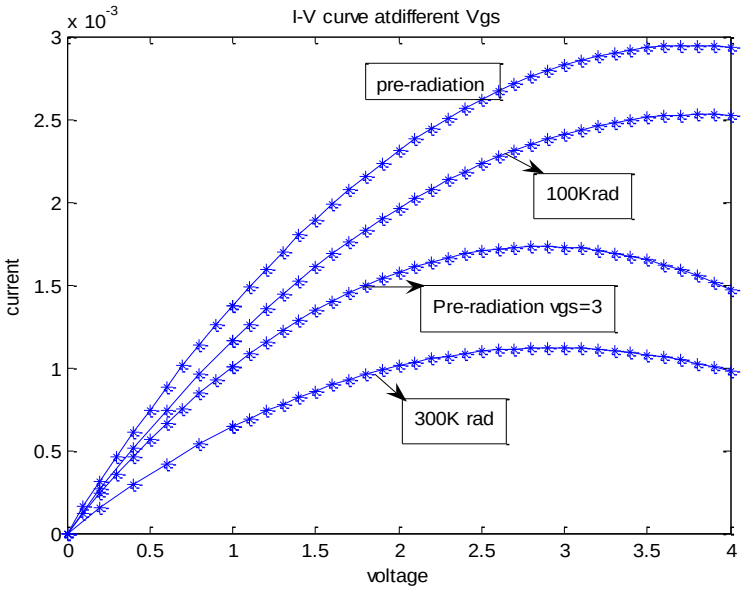

Fig.20 Shows effect of radiation on I_{ds}-V_{ds} curve. Current decreases with increasing dose.

VII. Discussions

1. Nit, Not: In the radiation prone environment, oxide charge and interface trapped charge both increase uniformly with dose.
2. Mobility: The dose dependence of the oxide fixed charge is shown. The resulting increase in interface charge causes a decrease in channel mobility.
3. Threshold voltage: These charges Nit and Not cancel to produce a total threshold shift of 20V at 500 Krad (si). At higher doses the interface trap charges dominate and there is a "rebound effect" in the nMOSFET threshold voltage.
4. Drain Current: simple uniformly increasing relationship between dose and both oxide charge and interface charge are sufficient for all these device characteristics the drain current decrease with increase in dose krad (si).

VIII. Conclusion

MOSFET is the basic component of VLSI and ULSI circuits but MOS devices are highly affected by ionization radiations. With feature sizes ranging from 180 to 90 nm, today's very deep submicron technologies pose new modeling challenges including power dissipation, leakage management, and short channel effects in deep submicron transistors, increasing capacitive and inductive noise in interconnect and platform integration issues. With this regard device models are constantly developed, elaborated and refined to achieve best description and prediction of the downscaling devices. Deep understanding

of the underlying physical phenomena is required as well as competent use of mathematical techniques to settle efficient and accurate modeling methodologies that encompass constantly downscaling technologies. Now a huge emphasis is placed on obtaining physics-based, simple and highly accurate analytical device models. MOSFET characteristics cannot be accurately predicted using classical modeling methods currently used in the most common MOSFET models such as BSIM, MM9 etc, without introducing large number of empirical parameters.

In this paper we have studied the basic of MOSFET and its parameters like mobility, transconductance, drain current and threshold voltage and also the consequences of ionization radiations on MOSFET parameters. We have also studied the different radiation environments which affects the MOSFET parameters. The threshold voltage changes when the device is irradiated, off-state current or leakage current increases and mobility and transconductance decreases when MOS transistors are exposed to ionization radiations. In this paper, we have developed an analytical model of MOSFET at deep submicron technology and parameters are extracted at deep submicron technology and also included radiation effects on MOS at deep submicron technology. Compare results of pre radiation and post radiation condition. The drain current increases in deep submicron technology manifold as compared to long channel MOSFET. But due to exposure to ionization radiations and short channel effects, MOSFET characteristics changes which degrades the electrical parameters of the device.

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